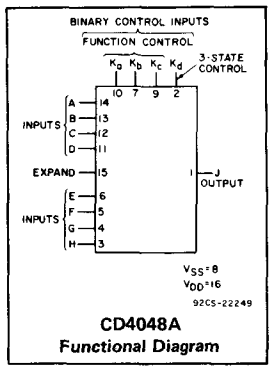
# CMOS Multi-Function Expandable 8-Input Gate

The RCA-CD4048A is an 8-input gate having four control inputs. Three binary control inputs – Ka, Kb, and Kc – provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

A fourth control input –Kd – provides the user with 3-state outputs. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the input states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 6). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to $V_{SS}$.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).




**CD4048A**
**Functional Diagram**

## MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE ($T_{stg}$) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
*DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)*
(Voltages referenced to $V_{SS}$ Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE ($P_D$)
FOR $T_A$ = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR $T_A$ = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A$ = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR $T_A$ = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to $V_{DD}$ +0.5 V
*LEAD TEMPERATURE (DURING SOLDERING):*
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

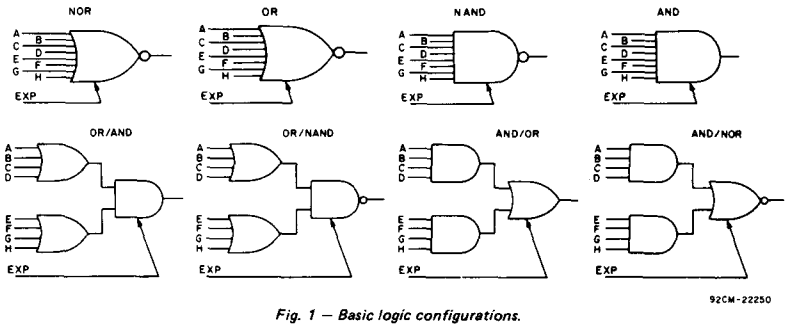



*Fig. 1 – Basic logic configurations.*

## RECOMMENDED OPERATING CONDITIONS

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | $V_{DD}$ (V) | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|
| | | D, F, K, H Packages | | E Package | | |
| | | Min. | Max. | Min. | Max. | |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | | 3 | 12 | 3 | 12 | V |

## *Features:*

- **Medium-power TTL drive capability**
- **Three-state output**
- **High current source and sink capability 9 mA (typ.) @ $V_{DS}$ = 0.5 V, $V_{DD}$ = 10 V**
- ***Many logic functions available in one package***
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

## *Applications:*

- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - ***Decoding***
  - **Encoding**

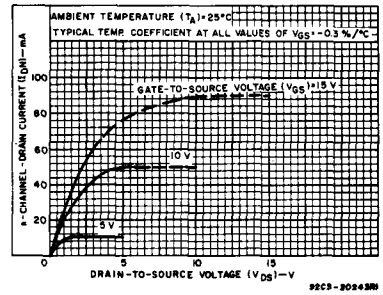



*Fig. 2– Typical output n-channel drain characteristics.*

## STATIC ELECTRICAL CHARACTERISTICS

| Characteristic | Conditions | | | Limits at Indicated Temperatures (°C) | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | D, F, K, H Packages | | | | E Package | | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | +25 Typ. | +25 Limit | +125 | −40 | +25 Typ. | +25 Limit | +85 | |
| Quiescent Device Current $I_L$ Max. | – | – | 5 | 1 | 0.005 | 1 | 60 | 10 | 0.01 | 10 | 140 | μA |
| | – | – | 10 | 2 | 0.01 | 2 | 120 | 20 | 0.02 | 20 | 280 | |
| | – | – | 15 | 25 | 0.5 | 25 | 1000 | 250 | 2.5 | 250 | 2500 | |
| Output Voltage: Low Level, $V_{OL}$ | – | 5 | 5 | 0 Typ.; 0.05 Max. | | | | | | | | V |
| | – | 10 | 10 | 0 Typ.; 0.05 Max. | | | | | | | | |
| High Level $V_{OH}$ | – | 0 | 5 | 4.95 Min.; 5 Typ. | | | | | | | | |
| | – | 0 | 10 | 9.95 Min.; 10 Typ. | | | | | | | | |
| Noise Immunity: Inputs Low, $V_{NL}$ | 4.2 | – | 5 | 1.5 Min.; 2.25 Typ. | | | | | | | | V |
| | 9 | – | 10 | 3 Min.; 4.5 Typ. | | | | | | | | |
| Inputs High $V_{NH}$ | 0.8 | – | 5 | 1.5 Min.; 2.25 Typ. | | | | | | | | |
| | 1 | – | 10 | 3 Min.; 4.5 Typ. | | | | | | | | |
| Noise Margin: Inputs Low, $V_{NML}$ | 4.5 | – | 5 | 1 Min. | | | | | | | | V |
| | 9 | – | 10 | 1 Min. | | | | | | | | |
| Inputs High, $V_{NMH}$ | 0.5 | – | 5 | 1 Min. | | | | | | | | |
| | 1 | – | 10 | 1 Min. | | | | | | | | |
| Output Drive Current: n-Channel (Sink) $I_DN$ Min. | 0.4 | – | 4.5 | 2 | 3.2 | 1.6 | 1.1 | 1.9 | 3.2 | 1.6 | 1.3 | mA |
| | 0.5 | – | 10 | 5.6 | 9 | 4.5 | 3.1 | 5.4 | 9 | 4.5 | 3.7 | |
| p-channel (Source), $I_DP$ Min. | 4.6 | – | 5 | −2 | −3.2 | −1.6 | −1.1 | −1.9 | −3.2 | −1.6 | −1.3 | |
| | 9.5 | – | 10 | −5.6 | −9 | −4.5 | −3.1 | −3.8 | −9 | −3.15 | −2.6 | |
| Input Leakage Current, $I_{IL}$, $I_{IH}$ | Any Input | | | | | | | | | | | μA |
| | – | – | 15 | $\pm 10^{-5}$ Typ., ± 1 Max. | | | | | | | | |
| 3-State Output Leakage Current $I_{OL}$, $I_{OH}$ | Forced (Output Disabled) | | | | | | | | | | | μA |
| | – | – | 15 | $\pm 10^{-4}$ Typ., ±2 Max. | | | | | | | | |

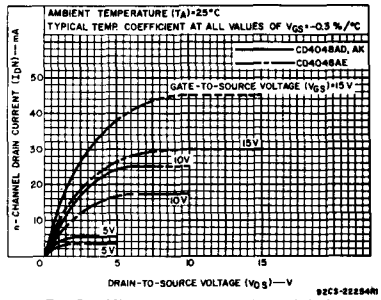



*Fig. 3— Minimum output n-channel drain characteristics*

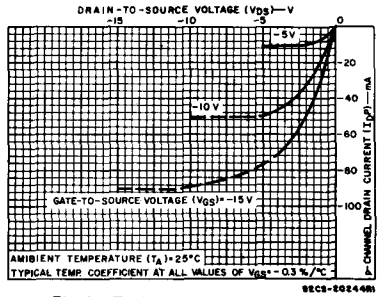



*Fig. 4— Typical output p-channel drain characteristics.*

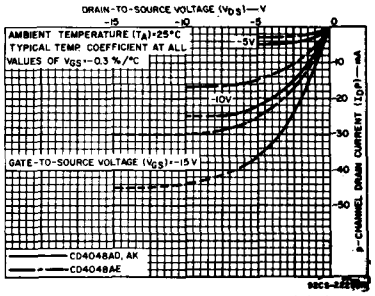



*Fig. 5— Minimum output p-channel drain characteristics.*

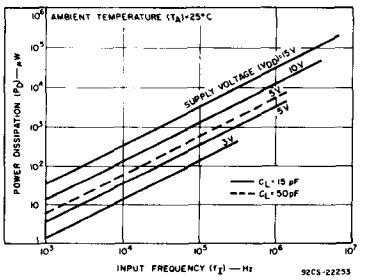



*Fig. 6— Typical power dissipation as a function of input frequency.*

**DYNAMIC ELECTRICAL CHARACTERISTCS** at $T_A$ = 25°C and $C_L$ = 15 pF and 50 pF,
Typical Temperature Coefficient for all values of $V_{DD}$ = 0.3%/°C $R_L$ = 200 kΩ

$C_L$ = 15 pF

| CHARACTERISTIC | TEST CONDITIONS | | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | *D, F, K, H Packages* | | *E Package* | | |
| | | $V_{DD}$ (Volts) | TYP. | MAX.* | TYP. | MAX.* | |
| Propagation Delay Time $t_{PHL}$ | | 5 | 750 | 1300 | 750 | 1600 | ns |
| | | 10 | 225 | 400 | 225 | 500 | |
| Transition Time: High-to-Low Level $t_{THL}$ | | 5 | 90 | 140 | 90 | 170 | ns |
| | | 10 | 30 | 50 | 30 | 65 | |
| Low-to-High Level $t_{TLH}$ | | 5 | 130 | 250 | 130 | 300 | ns |
| | | 10 | 40 | 60 | 40 | 75 | |
| Input Capacitance $C_I$ | Any Input | | 5 | – | 5 | – | pF |
| $C_L$ = 50 pF | | | | | | | |
| Propagation Delay Time $t_{PLH}, t_{PHL}$ | | 5 | 775 | 1350 | 775 | 1650 | ns |
| | | 10 | 240 | 430 | 240 | 530 | |
| Transition Time: High-to-Low Level $t_{THL}$ | | 5 | 105 | 170 | 105 | 200 | ns |
| | | 10 | 40 | 70 | 40 | 85 | |
| Low-to-High Level $t_{TLH}$ | | 5 | 145 | 280 | 145 | 330 | ns |
| | | 10 | 50 | 80 | 50 | 95 | |
| Input Capacitance $C_I$ | Any Input | | 5 | – | 5 | – | pF |

* Max. Limits represent worst-case limits for worst-case modes of operation shown in Figs. 15, 16, and 17.

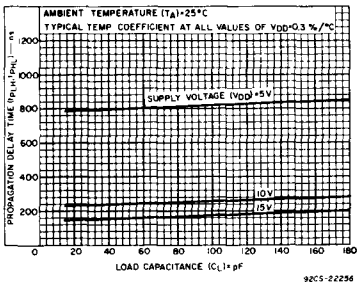



*Fig. 7— Typical propagation delay time as a function of load capacitance.*

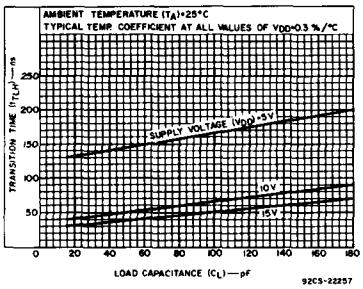



*Fig. 8— Typical low-to-high level transition time as a function of load capacitance.*

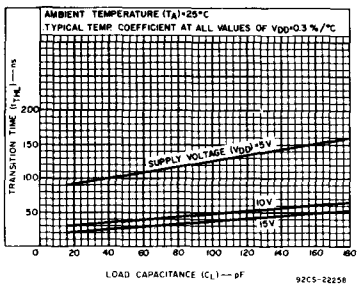



*Fig. 9— Typical high-to-low level transition time as a function of load capacitance.*

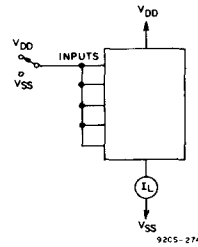



*Fig. 10— Quiescent-device-current test circuit.*

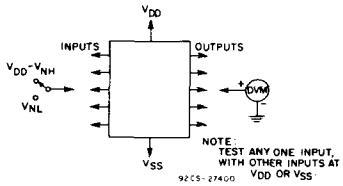



*Fig. 11— Noise-immunity test circuit.*

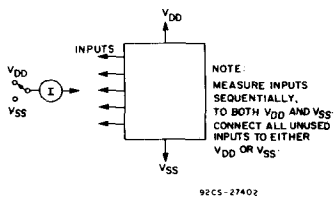
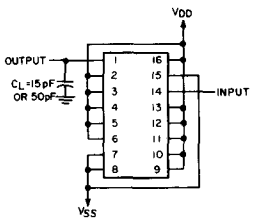



*Fig. 12— Input-leakage-current test circuit.*



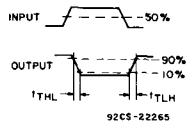
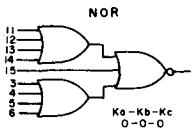




*Fig. 13— $t_{THL}$, $t_{TLH}$ — AND/NOR.*



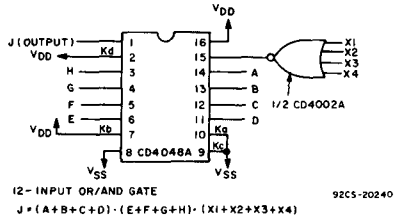
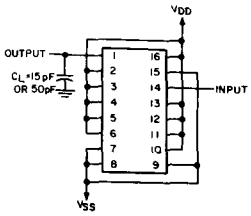




Fig. 14(a) - 12-input OR/AND gate.



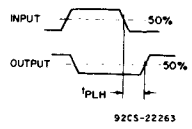
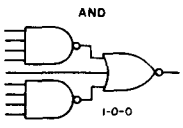
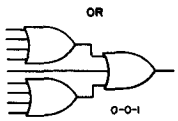




Fig. 15- $t_{PLH}$ - NAND.



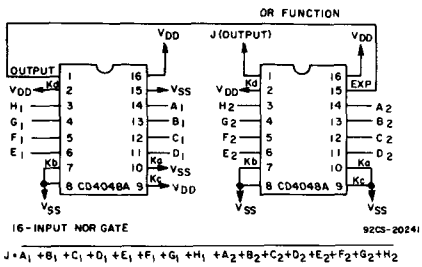
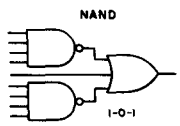



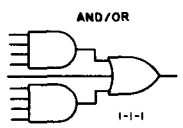

Fig. 14(b) 16-input NOR gate.
Applications of Expand Input

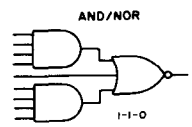


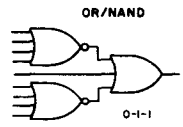

**IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS**

| OUTPUT FUNCTION | FUNCTION NEEDED AT EXPAND INPUT | OUTPUT BOOLEAN EXPRESSION |
|---|---|---|
| NOR | OR | $J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$ |
| OR | OR | $J=(A+B+C+D+E+F+G+H)+(EXP)$ |
| AND | NAND | $J=(ABCDEFGH)\cdot\overline{(EXP)}$ |
| NAND | NAND | $J=\overline{(ABCDEFGH)\cdot\overline{(EXP)}}$ |
| OR/AND | NOR | $J=(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}$ |
| OR/NAND | NOR | $J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}}$ |
| AND/NOR | AND | $J=\overline{(ABCD)+(EFGH)+(EXP)}$ |
| AND/OR | AND | $J=(ABCD)+(EFGH)+(EXP)$ |

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).



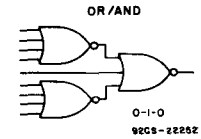
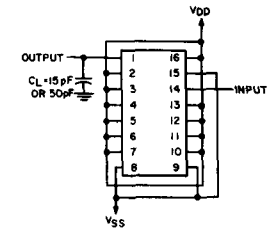




Fig. 14(c) Actual-circuit logic configurations.

Fig. 14- Expansion logic and truth table.



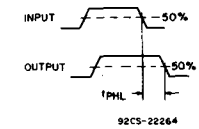
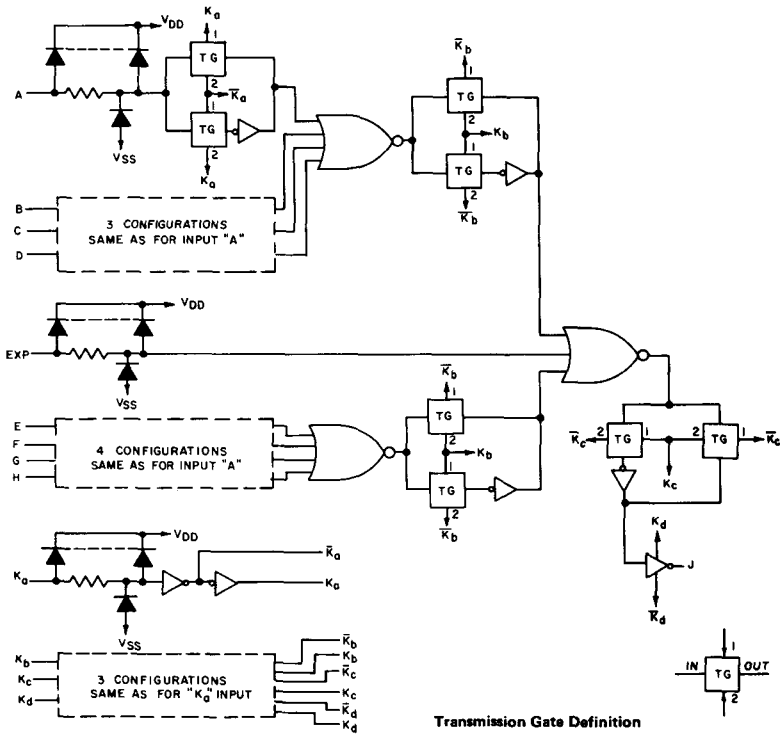




Fig. 16- $t_{PHL}$ - AND.




**Transmission Gate Definition**

TG = Transmission Gate
Input to Output is:

a) A bidirectional low impedance when control input 1 is low and control 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

92CM-22251RI

**FUNCTION TRUTH TABLE**

| OUTPUT FUNCTION | BOOLEAN EXPRESSION | $K_a$ | $K_b$ | $K_c$ | UNUSED INPUT* |
|---|---|---|---|---|---|
| NOR | $J=\overline{A+B+C+D+E+F+G+H}$ | 0 | 0 | 0 | $V_{SS}$ |
| OR | $J=A+B+C+D+E+F+G+H$ | 0 | 0 | 1 | $V_{SS}$ |
| OR/AND | $J=(A+B+C+D)\cdot(E+F+G+H)$ | 0 | 1 | 0 | $V_{SS}$ |
| OR/NAND | $J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$ | 0 | 1 | 1 | $V_{SS}$ |
| AND | $J=ABCDEFGH$ | 1 | 0 | 0 | $V_{DD}$ |
| NAND | $J=\overline{ABCDEFGH}$ | 1 | 0 | 1 | $V_{DD}$ |
| AND/NOR | $J=\overline{ABCD+EFGH}$ | 1 | 1 | 0 | $V_{DD}$ |
| AND/OR | $J=ABCD+EFGH$ | 1 | 1 | 1 | $V_{DD}$ |
| $K_d$=1 Normal Inverter Action | | | | | |
| $K_d$=0 High Impedance Output | | | | | |

EXPAND Input=0

*See Figs. 1 and 7.

*Fig. 17– Logic diagram and truth table.*