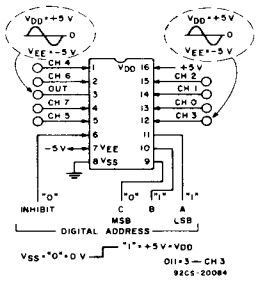
RCA
Solid State
Division

Digital Integrated Circuits

Monolithic Silicon

Preliminary CD4051AD, CD4051AE, CD 4051AK
Preliminary CD4052AD, CD4052AE, CD4052AK
Preliminary CD4053AD, CD4053AE, CD4053AK

Preliminary Data



Typical Connection For CD4051A.

COS/MOS Analog Multiplexers

With Logic—Level Conversion

CD4051AD, CD4051AE, CD4051AK — Single 8—Channel Multiplexer

CD4052AD, CD4052AE, CD4052AK — Differential 4—Channel Multiplexer

CD4053AD, CD4053AE, CD4053AK — Triple 2—Channel Multiplexer

RCA COS/MOS Analog Multiplexers CD4051A, CD4052A, and CD4053A are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage current. Control of analog signals up to 15 V p-p can be achieved by digital signal amplitudes of 3 to 15 V. For example, if V_{DD} = +5 V, V_{SS} = 0 V, and V_{EE} = −5 V, analog signals from −5 V to +5 V can be controlled by digital inputs of 0 to 5 V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are "OFF".

CD4051A is a single 8-channel multiplexer having three binary control inputs, A(LSB),B, and C(MSB) and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output. The terminals marked "CHANNEL IN/OUT" and "COMMON OUT/IN" can be used as input or output terminals. For example, when the CD4051A is being used as a Multiplexer, the "CHANNEL IN/OUT" terminals are the inputs, and the "COMMON OUT/IN" terminal is the output; when the CD4051A is being used as a Demultiplexer, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminal is the input.

CD4052A is a differential 4-channel multiplexer having two binary control inputs, A(LSB) and B(MSB), and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

Features:

- **Wide range of digital and analog signal levels: Digital 3 to 15 V p-p analog to 15 V p-p**
- **Low "ON" resistance — 50 Ω (typ) over entire 15-V p-p signal-input range for $V_{DD} - V_{EE}$ = 15 V**
- **High "OFF" resistance — input leakage ± 10 pA (typ) @ $V_{DD} - V_{EE}$ = 15 V**
- **Logic-level conversion for digital addressing signals of 3 to 15 V ($V_{DD} - V_{SS}$ = 3 V to 15 V) to switch analog signals to 15 V p-p ($V_{DD} - V_{EE}$ = 15 V)**
- **Matched switch characteristics ΔR_{ON} - 5 Ω (typ) for $V_{DD} - V_{EE}$ = 15 V**
- **Very low quiescent power dissipation under all digital-control input and supply conditions — 0.1 μW typ @ $V_{DD} - V_{SS} = V_{DD} - V_{EE}$ = 10 V**
- **Binary address decoding on chip**

Applications:

- **Analog and digital multiplexing and demultiplexing.**
- **A/D and D/A conversion.**
- **Signal gating.**

CD4053A is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C and an inhibit input. Each control input selects one pair of channels which

are connected in a single-pole double-throw configuration. All six channels are "OFF" when a logic 1 is present at the inhibit input.

These devices are supplied in a 16-lead dual-in-line ceramic package (CD4051AD, CD4052AD, and CD4053AD), a 16-lead dual-in-line plastic package (CD4051AE, CD4052AE, and CD4053AE), or a 16-lead flat pack (CD4051AK, CD4052AK, and CD4053AK).

Maximum Ratings, *Absolute Maximum Values*

Storage-Temperature Range ..... −65°C to +150°C
Operating-Temperature Range
  Ceramic Packages ..... −55°C to +125°C
  Plastic Packages ..... −40°C to +85°C
Dissipation Per Package ..... 200 mW
DC Supply Voltages
  $V_{DD} - V_{SS}$ ..... −0.5 to +15 V
  $V_{DD} - V_{EE}$ ..... −0.5 to +15 V
Channel Current ..... ±50 mA

Maximum Ratings, (cont'd)

Digital Control Inputs ..... $V_{SS} \leq V_I \leq V_{DD}$
Analog Inputs ..... $V_{EE} \leq V_I \leq V_{DD}$
Minimum Recommended Power Supply Voltages
  $V_{DD} - V_{SS}$ ..... 3 V
  $V_{DD} - V_{EE}$ ..... 3 V
Lead Temperature (During soldering)
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
  from case for 10 seconds max. ..... 265°C

ELECTRICAL CHARACTERISTICS @ $T_A = 25°C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
Quiescent Device Dissipation Per Package	P_D	V_{DD} = +10 V, V_{SS} = 0 V, V_{EE} = 0 V or V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V All Digital Combinations On The Address Inputs (Note 1), All Analog Inputs $V_{EE} \leq V_I \leq V_{DD}$		0.1	μW
Channel "ON"-Resistance	R_{ON}	$V_{DD} - V_{EE}$ = 15 V (i.e., V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −10 V) Channel Selection see Note 1; $V_{EE} \leq V_I \leq V_{DD}$		50	Ω
		$V_{DD} - V_{EE}$ = 10 V (i.e., V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V)		120	
Channel Δ "ON"−Resistance Between Any 2 Channels	ΔR_{ON}	$V_{DD} - V_{EE}$ = 15 V (i.e., V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −10 V)		5	Ω
		$V_{DD} - V_{EE}$ = 10 V (i.e., V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V)		10	
Leakage Current: Any Channel (Channel OFF)		V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V, $V_{EE} \leq V_I \leq V_{DD}$		±10	pA
Leakage Current: Common (All Channels OFF)		V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V Inhibit = +5 V	CD4051A	±80	pA
			CD4052A	±40	
			CD4053A	±20	
Average Input Capacitance	C_I	V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V Channel OFF		6	pF
Average Output Capacitance	C_O	V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V Inhibit = + 5 V	CD4051A	30	pF
			CD4052A	18	
			CD4053A	10	
Turn-on Propagation Delay	t_{pd}	V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −5 V		200	ns
Address Input Resistance	R_I			10^{11}	Ω

NOTE 1: Positive Address − Logic: "0" = V_{SS}, "1" = V_{DD}
i.e., for CD4051A: C = 1, B = 1, A = 0, Inhibit = 0, turns ON CHANNEL 6

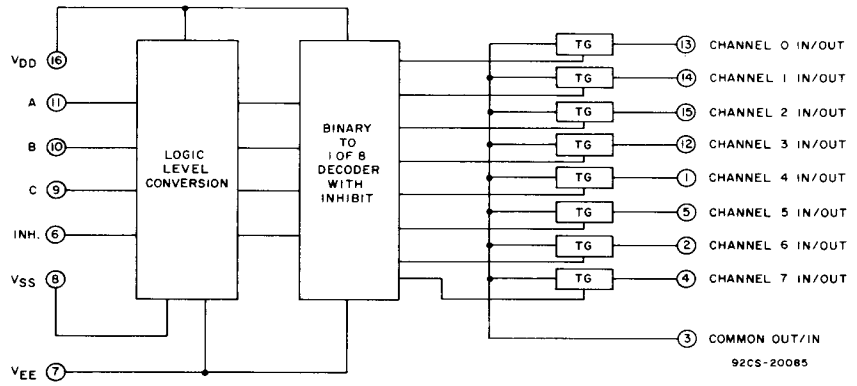


Fig.1—Functional diagram, CD4051A.

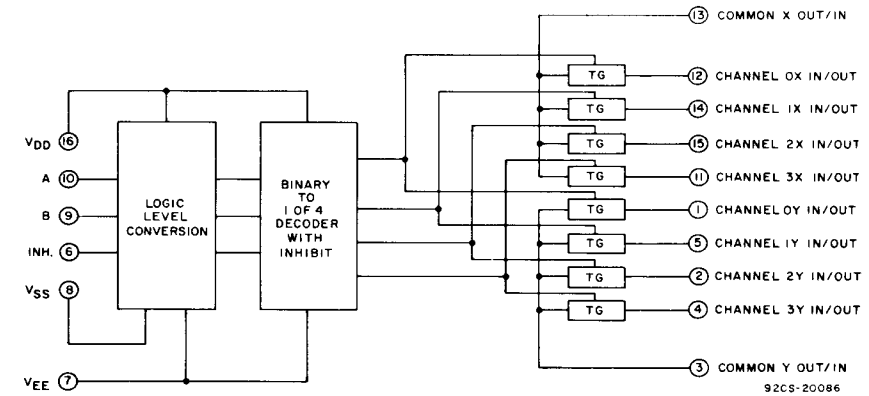


Fig.2—Functional diagram, CD4052A.

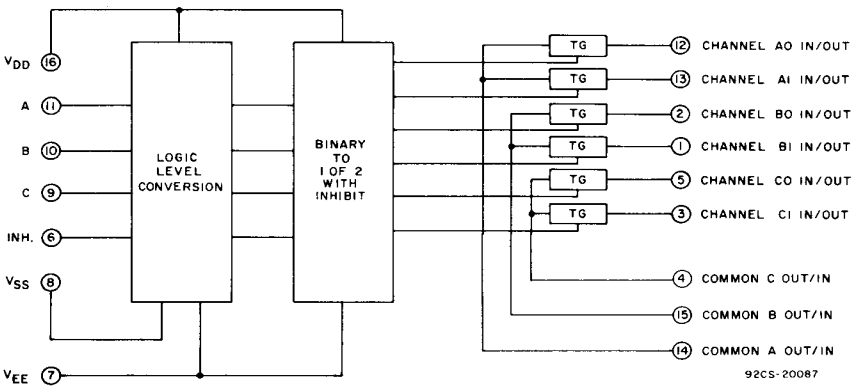


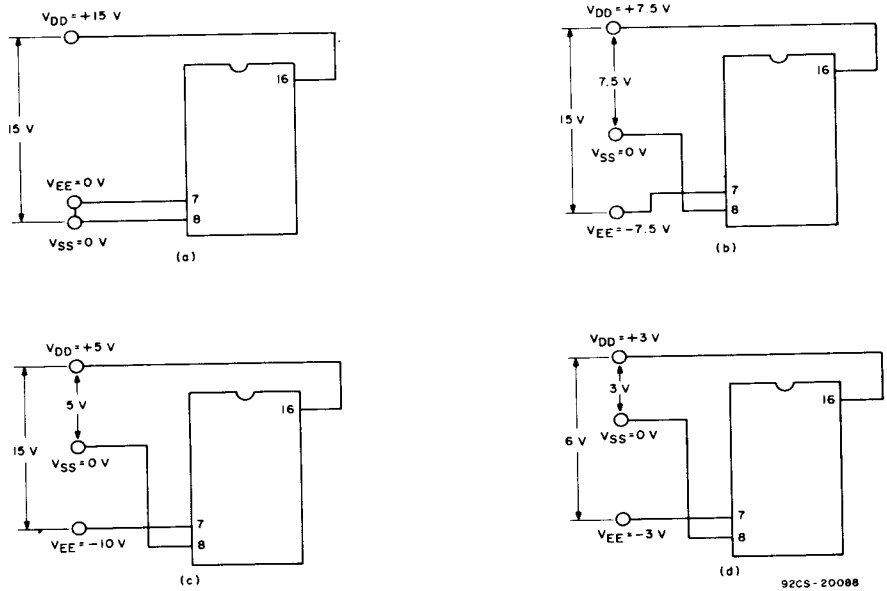
Fig.3—Functional diagram, CD4053A.

TRUTH TABLE

TABLE I

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051A	CD4052A	CD4053A
0	0	0	0	0	0x, 0y	A0, B0, C0
0	0	0	1	1	1x, 1y	A1, B0, C0
0	0	1	0	2	2x, 2y	A0, B1, C0
0	0	1	1	3	3x, 3y	A1, B1, C0
0	1	0	0	4		A0, B0, C1
0	1	0	1	5		A1, B0, C1
0	1	1	0	6		A0, B1, C1
0	1	1	1	7		A1, B1, C1
1	*	*	*	NONE	NONE	NONE

* = Don't care condition



The ADDRESS (digital-control inputs) and INHIBIT logic levels are "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

Fig.4—Typical bias voltages.

Type	Package	JEDEC Dimensional Outline
CD4051AD, CD4052AD, CD4053AD	16-Lead Dual-In-Line Ceramic	MO-001-AE
CD4051AE, CD4052AE, CD4053AE	16-Lead Dual-In-Line Plastic	MO-001-AC
CD4051AK, CD4052AK, CD4053AK	16-Lead Ceramic Flat Pack	MO-004-AG