CD4051M/CD4051C
Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052M/CD4052C
Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053M/CD4053C
Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to 15 Vp-p can be achieved by digital signal amplitudes of 3–15V. For example, if V_{DD} = 5V, V_{SS} = 0V and V_{EE} = −5V, analog signals from −5V–+5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate, extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF."

CD4051M/CD4051C is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

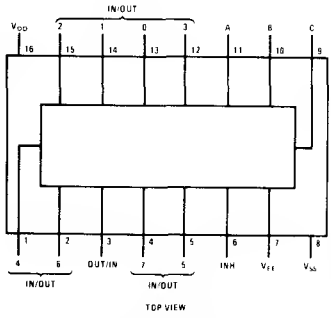
CD4052M/CD4052C is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053M/CD4053C is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

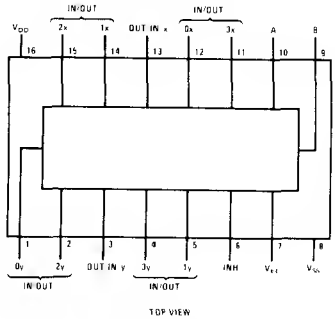
Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to 15 Vp-p
- Low "ON" resistance: 80Ω (typ) over entire 15 Vp-p signal-input range for $V_{DD} - V_{EE}$ = 15V
- High "OFF" resistance: input leakage ±10 pA (typ) at $V_{DD} - V_{EE}$ = 10V
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD} - V_{SS}$ = 3–15V) to switch analog signals to 15 Vp-p ($V_{DD} - V_{EE}$ = 15V)
- Matched switch characteristics: ΔR_{ON} = 5Ω (typ) for $V_{DD} - V_{EE}$ = 15V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1μW typ at $V_{DD} - V_{SS} = V_{DD} - V_{EE}$ = 10V
- Binary address decoding on chip

Connection Diagrams (Dual-In-Line and Flat Packages)



Order Number CD4051MD
See Package 15
Order Number CD4051MF
See Package 24
Order Number CD4051CJ or CD4051MJ
See Package 19
Order Number CD4051CN
See Package 22



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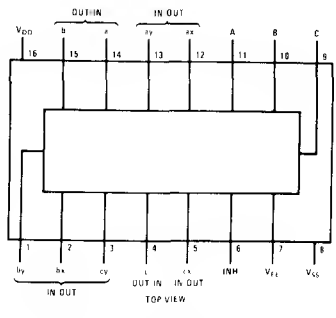


Order Number CD4053MD
See Package 15
Order Number CD4053MF
See Package 24
Order Number CD4053CJ or CE4053MJ
See Package 19
Order Number CD4053CN
See Package 22

Absolute Maximum Ratings

Voltage at Any Control Input	V_{SS} − 0.3V to V_{DD} + 0.3V
Voltage at Any Switch Input or Output	V_{EE} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD40XXM	−55°C to +125°C
CD40XXC	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{EE} + 3V to V_{EE} + 15V
	V_{SS} + 3V to V_{SS} + 15V

Electrical Characteristics CD4051M, CD4052M, CD4053M

	PARAMETER	CONDITIONS			−55°C MIN	−55°C TYP	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C TYP	125°C MAX	UNITS
P_D	Quiescent Dissipation Per Package	V_{DD} = 10V, V_{EE} = V_{SS} = 0V					100		1	100			6000	µW
R_{ON}	"ON" Resistance (Peak for $V_{SS} \leq V_{IS} \leq V_{DD}$)		V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V V_{EE} = 0V			60	220		80	280		145	320	Ω
		R_L = 10 kΩ V_{SS} = 0, (Any Channel Selected)	V_{DD} = 5V V_{EE} = 5V or V_{DD} = 10V V_{EE} = 0V			85	400		120	400		190	550	Ω
			V_{DD} = 2.5V V_{EE} = 2.5V or V_{DD} = 5V V_{EE} = 0V			210	3000		270	2500		360	5500	Ω
ΔR_{ON}	Δ "ON" Resistance Between Any Two Channels	R_L = 10 kΩ V_{SS} = 0 (Any Channel Selected)	V_{DD} = 7.5V, V_{EE} = 7.5V or V_{DD} = 15V V_{EE} = 0V						5					Ω
			V_{DD} = 5V V_{EE} = 5V or V_{DD} = 10V V_{EE} = 0V						10					Ω
	Sine Wave Response (Distortion)	R_L = 10 kΩ, V_{SS} = 0, f_{IS} = 1 kHz	V_{DD} = 7.5V V_{EE} = 7.5V						0.1					%
			V_{DD} = 5V V_{EE} = −5V						0.2					%
			V_{DD} = 2.5V V_{EE} = 2.5V						1					%
	"OFF" Channel Leakage Current Any Channel "OFF"	V_{SS} = 0V OUT IN = ±7.5V, IN OUT = 0V	V_{DD} = 7.5V V_{EE} = 7.5V				±50		±0.01	±50			±500	nA
	All Channels "OFF" (Common OUT/IN)	Inhibit = 5V V_{SS} = 0V OUT IN = 0V, IN OUT = ±7.5V	V_{DD} = 7.5V V_{EE} = 7.5V	CD4051M			±400		±0.08	±400			±4000	nA
				CD4052M			±200		±0.04	±200			±2000	nA
				CD4053M			±100		±0.02	±100			±1000	nA
	Frequency Response Channel "ON" (Sine Wave Input)	R_L = 1 kΩ, V_{IS} = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = 5V 20 $\log_{10} V_{OS}/V_{IS}$ = −3 dB						40					MHz
	Feedthrough Channel "OFF"	R_L = 1 kΩ V_{IS} = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V 20 $\log_{10} V_{OS}/V_{IS}$ = −40 dB						1					MHz
	Crosstalk Between Any Two Channels (Frequency at 40 dB)	R_L = 1 kΩ V_{IS}(A) = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V 20 $\log_{10} V_{OS}$(B)/V_{IS}(A) = −40 dB (Note 1)						1					MHz
C_{IS}	Capacitance Input (IN/OUT)	V_{DD} = V_{EE} = V_{SS} = 0V							10					pF
C_{OS}	Output (Common OUT/IN)			CD4051M					60					pF
				CD4052M					30					pF
				CD4053M					20					pF
C_{IOS}	Feedthrough								0.2					pF
t_{PLH}, t_{PHL}	Propagation Delay Signal Input to Signal Output	V_{DD} = 10V, V_{SS} = V_{EE} = Inhibit = 0V, C_L = 15 pF, V_{IS} = 10V (Square Wave), t_r, t_f = 20 ns (Input Signal)							10					ns

Electrical Characteristics (Continued) CD4051M, CD4052M, CD4053M

PARAMETER		CONDITIONS		55°C			25°C			125°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CONTROL INPUTS A, B, C AND INHIBIT													
	Noise Immunity (Any Control Input)												
V_{NL}		$V_{IS} = V_{DD}$ through 1 kΩ, $V_{EE} = V_{SS}$	$V_{DD} - V_{SS} = 10V$	3.0			3.0	4.5		2.9			V
			$V_{DD} - V_{SS} = 5V$	1.5			1.5	2.25		1.4			V
V_{NH}		$I_{IS} = 10\mu A$ $R_L = 1k\Omega$ to V_{EE}	$V_{DD} - V_{SS} = 10V$	2.9			3.0	4.5		3.0			V
			$V_{DD} - V_{SS} = 5V$	1.4			1.5	2.25		1.5			V
C_I	Average Input Capacitance							5					pF
t_{PHL}, t_{PLH}	Turn "ON" Propagation Delay Control Input to Signal Output	$C_L = 15$ pF, $R_L = 10$ kΩ, $V_{IS} \leq V_{DD}$ $t_r, t_f = 20$ ns V_{SS} = Inhibit = 0V, (Note 2)	$V_{DD} = 10V$, $V_{EE} = 0V$					150	300				ns
			$V_{DD} = 5V$, $V_{EE} = 0V$					400	800				ns
			$V_{DD} = 5V$, $V_{EE} = 5V$					200	400				ns
	Inhibit Input to Signal Output	$C_L = 15$ pF, $R_L = 10$ kΩ, $V_{IS} = V_{DD}$ $t_r, t_f = 20$ ns	$V_{DD} = 10V$ $V_{EE} = 0V$					200	400				ns
			$V_{DD} = 5V$ $V_{EE} = 0V$					550	1100				ns
	Inhibit Recovery Time	$V_{DD} = 10V$						200	400				ns

Electrical Characteristics CD4051C, CD4052C, CD4053C

PARAMETER		CONDITIONS			40°C			25°C			85°C			UNITS
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
P_D	Quiescent Dissipation Per Package	$V_{DD} = 10V$ $V_{EE} = V_{SS} = 0V$					1000		1	1000			6000	μW
R_{ON}	"ON" Resistance (Peak for $V_{SS} \leq V_{IS} \leq V_{DD}$)	$R_L = 10$ kΩ, $V_{SS} = 0$, (Any Channel Selected)	$V_{DD} = 7.5V$, $V_{EE} = 7.5V$, or $V_{DD} = 15V$, $V_{EE} = 0V$		80	250		80	280		130	300	Ω
			$V_{DD} = 5V$, $V_{EE} = 5V$, or $V_{DD} = 10V$, $V_{EE} = 0V$		100	450		120	400		170	520	Ω
			$V_{DD} = 2.5V$ $V_{EE} = 2.5V$, or $V_{DD} = 5V$, $V_{EE} = 0V$		230	3500		270	2500		330	5200	Ω
ΔR_{ON}	Δ "ON" Resistance Between Any Two Channels	$R_L = 10$ kΩ, $V_{SS} = 0$, (Any Channel Selected)	$V_{DD} = 7.5V$, $V_{EE} = 7.5V$, or $V_{DD} = 15V$, $V_{EE} = 0V$					5					Ω
			$V_{DD} = 5V$, $V_{EE} = 5V$ or $V_{DD} = 10V$ $V_{EE} = 0V$					10					Ω
	Sine Wave Response (Distortion)	$R_L = 10$ kΩ, $V_{SS} = 0$, $f_{IS} = 1$ kHz	$V_{DD} = 7.5V$, $V_{EE} = 7.5V$					0.1					%
			$V_{DD} = 5V$, $V_{EE} = -5V$					0.2					%
			$V_{DD} = 2.5V$, $V_{EE} = 2.5V$					1					%
	"OFF" Channel Leakage Current Any Channel "OFF"	$V_{SS} = 0V$ OUT IN = +7.5V IN OUT = 0V	$V_{DD} = 7.5V$ $V_{EE} = 7.5V$			±50		±0.01	±50			±200	nA
	All Channels "OFF" (Common OUT/IN)	Inhibit = 5V $V_{SS} = 0V$ OUT IN = 0V, IN OUT = 7.5V	$V_{DD} = 7.5V$ $V_{EE} = 7.5V$	CD4051C		±1600		±0.08	±400			±1600	nA
				CD4052C		±800		±0.04	±200			±800	nA
				CD4053C		±400		±0.02	±100			±400	nA
	Frequency Response Channel "ON" (Sine Wave Input)	$R_L = 1$ kΩ, $V_{IS} = 5V$ (p-p), $V_{SS} = 0V$	$V_{DD} = 5V$ $V_{EE} = 5V$, 20 $\log_{10} V_{OS}/V_{IS} = -3$ dB					40					MHz

Electrical Characteristics (Continued) CD4051C, CD4052C, CD4053C

PARAMETER	CONDITIONS		-40°C			25°C			85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Feedthrough Channel "OFF"	R_L = 1 kΩ, V_{IS} = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V, 20 $Log_{10} V_{OS}/V_{IS}$ = −40 dB					1					MHz
Crosstalk Between Any Two Channels (Frequency at 40 dB)	R_L = 1 kΩ, V_{IS}(A) = 5V (p-p), V_{SS} = 0V	V_{DD} = 5V, V_{EE} = −5V, 20 $Log_{10} V_{OS}$(B)/V_{IS}(A) = 40 dB (Note 1)					1					MHz
Capacitance												
C_{IS} Input (IN/OUT)							10					pF
C_{OS} Output (Common OUT/IN)	V_{DD} = V_{EE} = V_{SS} = 0V	CD4051C					60					pF
		CD4052C					30					pF
		CD4053C					20					pF
C_{IOS} Feedthrough							0.2					pF
t_{PLH}, t_{PHL} Propagation Delay Signal Input to Signal Output	V_{DD} = 10V, V_{SS} = V_{EE} = Inhibit = 0V, C_L = 15 pF, V_{IS} = 10V (Square Wave), t_r, t_f = 20 ns (Input Signal)						10					ns
CONTROL INPUTS A, B, C AND INHIBIT												
V_N Noise Immunity (Any Control Input)	V_{IS} = V_{DD} through 1 kΩ, V_{EE} = V_{SS}	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
		V_{DD} = 5V	1.5			1.5	2.25		1.4			V
V_{NH}	I_{IS} = 10μA, R_L = 1kΩ to V_{EE}	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
		V_{DD} = 5V	1.4			1.5	2.25		1.5			V
C Average Input Capacitance							5					pF
t_{PHL}, t_{PLH} Turn "ON" Propagation Delay Control Input to Signal Output	C_L = 15 pF, R_L = 10 kΩ, V_S = V_{DD}, t_r, t_f = 20 ns, V_{SS} = Inhibit = 0V (Note 2)	V_{DD} = 10V, V_{EE} = 0V					150	300				ns
		V_{DD} = 5V, V_{EE} = 0V					400	800				ns
		V_{DD} = 5V, V_{EE} = −5V					200	400				ns
Inhibit Input to Signal Output	C_L = 15 pF, R_L = 10 kΩ, V_S = V_{DD}, t_r, t_f = 20 ns	V_{DD} = 10V, V_{EE} = 0V					200	400				ns
		V_{DD} = 5V, V_{EE} = 0V					550	1100				ns
Inhibit Recovery Time	V_{DD} = 10V						200	400				ns

Note 1: A,B are two arbitrary channels with A turned "ON" and B "OFF."

Note 2: Channel Overlap = Turn "ON" delay, where channel overlap is defined as the duration after control signal change during which two channels may be "ON" together.

Note 3: V_{IS} = input signal voltage, V_{OS} = output signal voltage, f_{IS} = input signal frequency.

Special Considerations

In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into "In/Out" pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into "Out/In" pin.

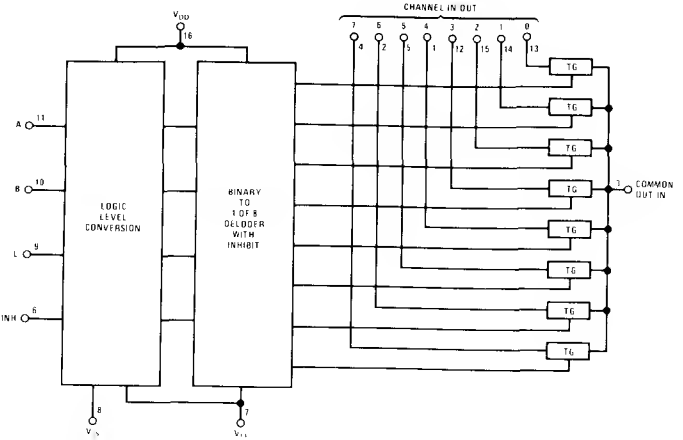
Truth Table

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051A	CD4052A	CD4053A
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

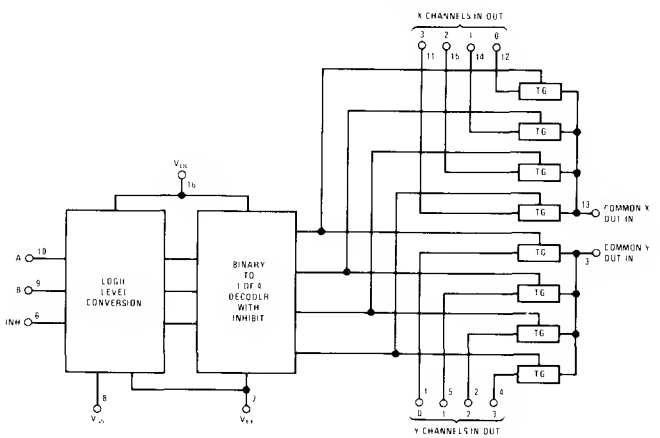
*Don't Care condition

Schematic Diagrams

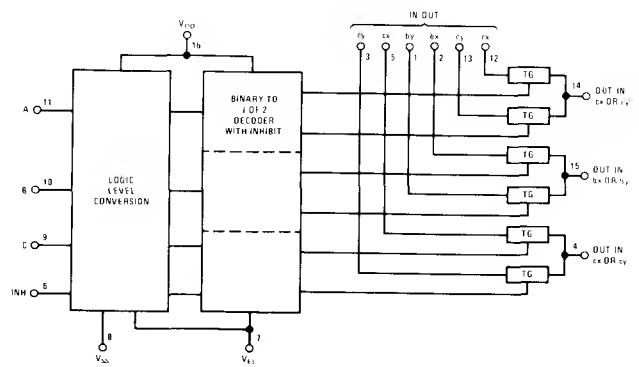
CD4051M/CD4051C



CD4052M/CD4052C

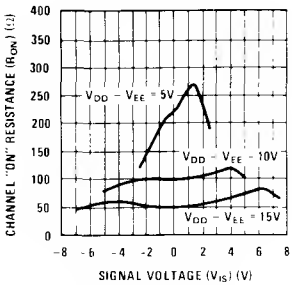


CD4053M/CD4053C

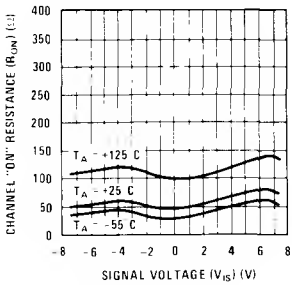


Typical Performance Characteristics

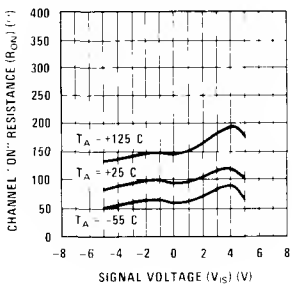
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$