

CD4054B, CD4055B, CD4056B Types

CMOS Liquid-Crystal Display Drivers

High-Voltage Types (20-Volt Rating)

CD4054B – 4-Segment Display Driver

CD4055B – BCD to 7-Segment Decoder/Driver with "Display-Frequency" Output

CD4056B – BCD to 7-Segment Decoder/Driver with Strobed-Latch Function

The RCA CD4055B and CD4056B types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signal swings (V_{DD} to V_{SS}) may be as small as 0 to -3 V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be as large as from 0 to -15 V. If V_{DD} to V_{EE} exceeds 15 V, V_{DD} to V_{SS} should be at least 4V (0 to -4 V).

The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055B provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056B provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the CD4055B and CD4056B provides displays of 0 to 9 as well as L, P, H, A, $-$, and a blank position.

The CD4054B provides level shifting similar to the CD4055B and CD4056B independently strobed latches, and common DF control on 4 signal lines. The CD4054B is intended to provide drive-signal compatibility with the CD4055B and CD4056B 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054B output line by connect-

Features:

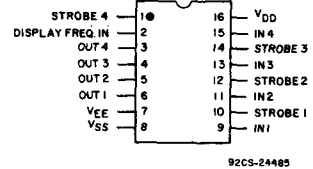
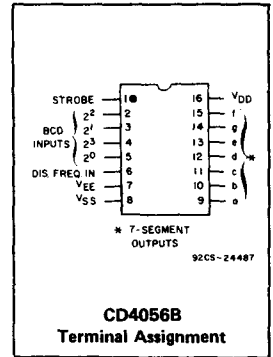
- Operation of liquid crystals with CMOS circuits provides ultra-low-power displays
- Equivalent ac output drive for liquid-crystal displays – no external capacitor required
- Voltage doubling across display, e.g. $V_{DD} - V_{EE} = 18$ V results in effective 36 V p-p drive across selected display segments
- Low- or high-output level dc drive for other types of displays
- On-chip logic-level conversion for different input- and output-level swings
- Full decoding of all input combinations: 0-9, L, H, P, A, $-$, and blank positions
- Strobed-latch function—CD4054B Series and CD4056B Series
- DISPLAY-FREQUENCY (DF) output for liquid-crystal common-line drive signal—CD4055B Series (CD4054B Series also; see introductory text)
- 100% tested for quiescent current at 20 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings

Applications

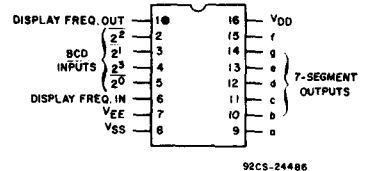
- General-purpose displays
- Calculators and meters
- Wall and table clocks
- Industrial control panels
- Portable lab instruments
- Panel meters
- Auto dashboard displays
- Appliance control panels

ing the corresponding input and strobe lines to a low and high level, respectively and applying a square wave to DF_{IN}. The CD4054B may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0 V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to -5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD} . Thus, the input and output swings can be selected independently of each other over a 3-to-18 V range. V_{SS} may be connected to V_{EE} when no level-shift function is required.

For the CD4054B and CD4056B, data are



CD4054B Terminal Assignment



CD4055B Terminal Assignment

transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low.

Whenever the level-shifting function is required, the CD4055B can be used by itself to drive a liquid-crystal display (Fig. 16 and Fig. 20). The CD4056B, however, must be used together with a CD4054B to provide the common DF output (Fig. 19). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig. 18. Fig. 17 is common to all three types.

The CD4054B-, CD4055B-, and CD4056B-series types are available in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

CD4054B, CD4055B, CD4056B Types

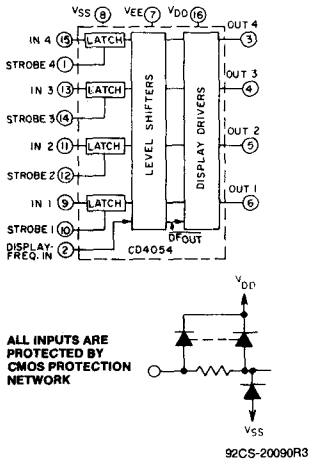


Fig. 1 - CD4054B functional diagram.

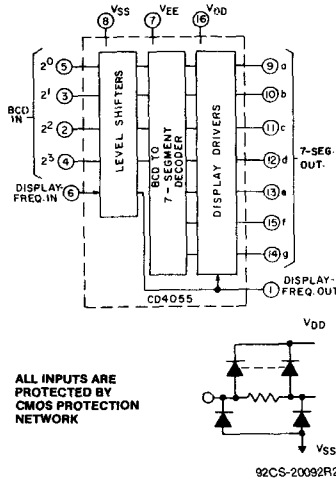


Fig. 2 - CD4055B functional diagram.

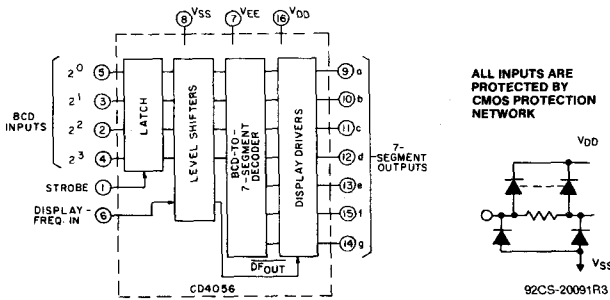


Fig. 3 - CD4056B functional diagram.

TRUTH TABLE FOR CD4055B and CD4056B

INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2 ³	2 ²	2 ¹	2 ⁰	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	□
0	0	0	1	0	1	1	0	0	0	0	□
0	0	1	0	1	1	0	1	1	0	1	□
0	0	1	1	1	1	1	1	0	0	1	□
0	1	0	0	0	1	1	0	0	1	1	□
0	1	0	1	1	0	1	1	0	1	1	□
0	1	1	0	1	0	1	1	1	1	1	□
0	1	1	1	1	1	1	1	0	0	0	□
1	0	0	0	1	1	1	1	1	1	1	□
1	0	0	1	1	1	1	1	0	1	1	□
1	0	1	0	0	0	0	1	1	1	0	□
1	0	1	1	0	1	1	0	1	1	1	□
1	1	0	0	1	1	0	0	1	1	1	□
1	1	0	1	1	1	1	0	1	1	1	□
1	1	1	0	0	0	0	0	0	0	1	□
1	1	1	1	0	0	0	0	0	0	0	BLANK

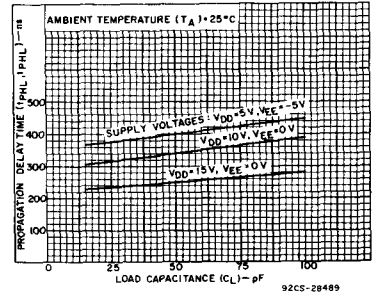


Fig. 4 - Typical propagation delay time vs. load capacitance for CD4054B.

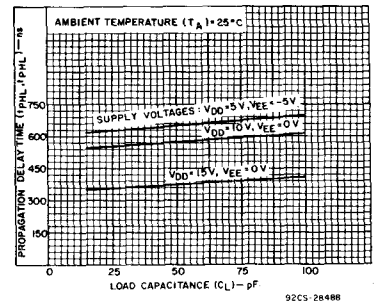


Fig. 5 - Typical propagation delay time vs. load capacitance for CD4055 and CD4056B.

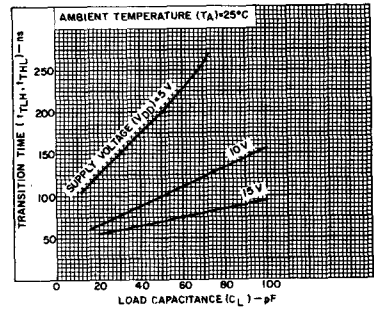


Fig. 6 - Typical transition time vs. load capacitance.

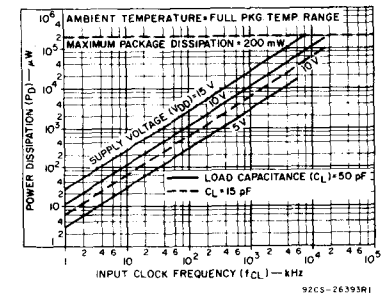


Fig. 7 - Typical input clock frequency vs. power dissipation.

CD4054B, CD4055B, CD4056B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	CONDITIONS					LIMITS							Units	
	V_{EE} (V)	V_{SS} (V)	V_O (V)	V_{IN} (V)	V_{DD} (V)	Values at $-55, +25, +125$ Apply to D, F, K, H, Packages Values at $-40^\circ, +25^\circ, +85^\circ\text{C}$ Apply to E Package								
						-55°	-40°	$+85^\circ$	$+125^\circ$	$+25^\circ\text{C}$				
											Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} MAX.	-5	0			5	5	150	150	-	0.04	5	μA		
	0	0			10	10	300	300	-	0.04	10			
	0	0			15	20	600	600	-	0.04	20			
	0	0			20	100	3000	3000	-	0.08	100			
Output Voltage: Low Level, V_{OL} MAX.	0	0		0.5	5		0.05		-	0	0.05	V		
	0	0		0.10	10		0.05		-	0	0.05			
	0	0		0.15	15		0.05		-	0	0.05			
	0	0		0.5	5		4.95		4.95	5	-			
High Level, V_{OH} MIN.	0	0		0.10	10		9.95		9.95	10	-	V		
	0	0		0.15	15		14.95		14.95	15	-			
	0	0	0.5											
	0	0	4.5		5		1.5		-	-	1.5			
Input Low Voltage, V_{IL} MAX.	0	0	1.9		10		3		-	-	3	V		
	0	0	1.5, 13.5		15		4		-	-	4			
	-5	0	0.5, 4.5		5		3.5		3.5	-	-			
	0	0	1.9		10		7		7	-	-			
Input High Voltage, V_{IH} MIN.	0	0	1.5, 13.5		15		11		11	-	-	V		
	-5	0	-4.5		5	0.98	0.92	0.67	0.55	0.8	1.6		mA	
	0	0	0.5		10	0.98	0.92	0.67	0.55	0.8	1.6			
	0	0	1.5		15	3.6	3.4	2.4	2	2.9	5.8			
Output Low (Sink) Current, I_{OL}	-5	0	4.5		5	-0.6	-0.55	-0.35	-0.3	-0.45	-0.9	mA		
	0	0	9.5		10	-0.6	-0.55	-0.35	-0.3	-0.45	-0.9			
	0	0	13.5		15	-1.9	-1.8	-1.2	-1.1	-1.5	-3			
	0	0			18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$		± 0.1	
Input Current, I_{IN}	0	0			0.18							μA		

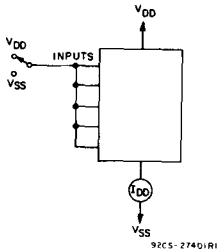


Fig. 11 - Quiescent-device-current test circuit.

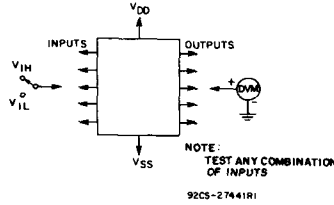


Fig. 12 - Input-voltage test circuit.

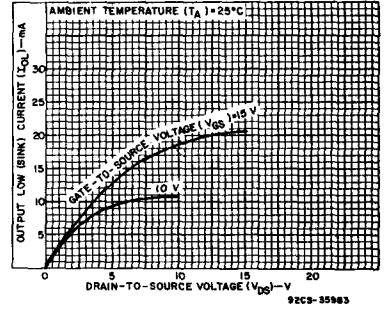


Fig. 8 - Typical n-channel output low (sink) current characteristics.

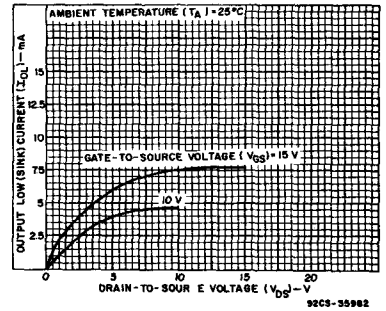


Fig. 9 - Minimum n-channel output low (sink) current characteristics.

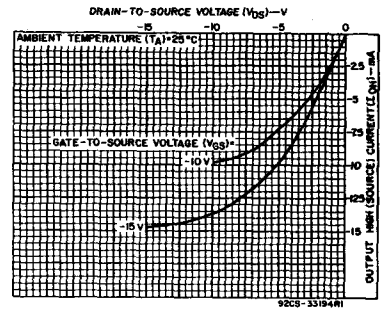


Fig. 10 - Typical p-channel output high (source) current characteristics.

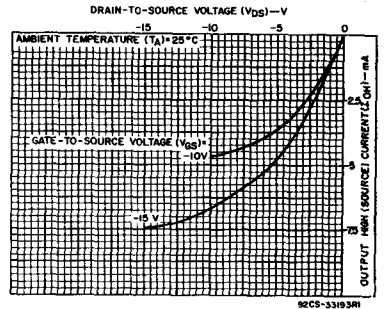


Fig. 13 - Minimum p-channel output high (source) current characteristics.

CD4054B, CD4055B, CD4056B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, Input $t_r, t_f = 20\text{ ns}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	CONDITIONS			LIMITS				UNITS
	VEE (V)	VSS (V)	VDD (V)	ALL PACKAGE TYPES				
				CD4054		CD4055, CD4056		
Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
Propagation Delay Time, t_{PHL}, t_{PLH} (Any Input to Any Output)	-5	0	5	400	800	650	1300	ns
	0	0	10	340	680	575	1150	
	0	0	15	250	500	375	750	
Transition Time, t_{THL}, t_{TLH} (Any Output)	-5	0	5	100	200	100	200	ns
	0	0	10	100	200	100	200	
	0	0	15	75	150	75	150	
Minimum Data Setup Time, t_S^*	-5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
			15	35	70	35	70	
Minimum Strobe Pulse Width, t_W^*	-5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
	0	0	15	35	70	35	70	
Input Capacitance, C_{IN} (Any Input)	-	-	-	5	7.5	5	7.5	pF

* CD4054 and CD4056 only.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$ (Unless otherwise specified)
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	VEE (V)	VSS (V)	VDD (V)	LIMITS		UNITS
				Min.	Max.	
Supply Voltage Range: (At $T_A = \text{Full Package Temperature Range}$)				3	18	V
Setup Time (t_S) [•]	-5	0	5	220	-	ns
	0	0	10	100	-	
	0	0	15	70	-	
Strobe Pulse Width (t_W) [•]	-5	0	5	220	-	ns
	0	0	10	100	-	
	0	0	15	70	-	

• For CD4054 and CD4056 only.

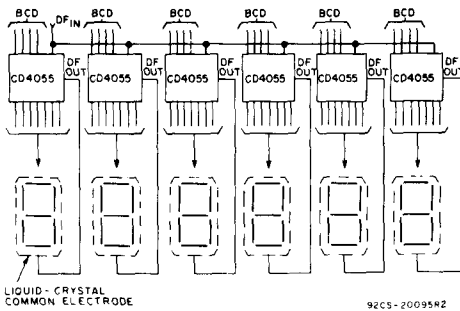


Fig. 16 - Clock display: $V_{DD} = 0\text{ V}$, $V_{SS} = -5\text{ V}$, $V_{EE} = -15\text{ V}$, $DF_{IN} = 30\text{ Hz}$ square wave.

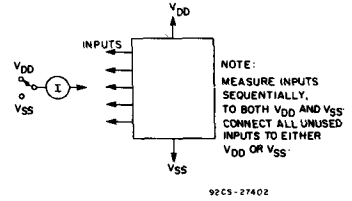


Fig. 14 - Input-current test circuit.

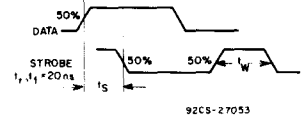


Fig. 15 - Data setup time and strobe pulse duration.

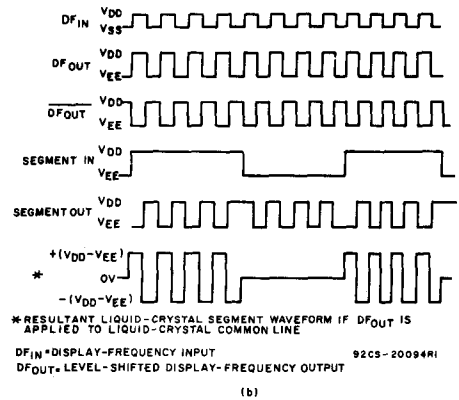
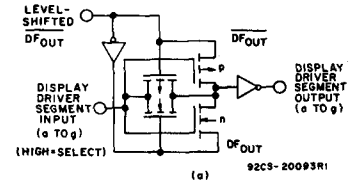


Fig. 17 - Display-driver circuit for one segment line and waveforms.

CD4054B, CD4055B, CD4056B Types

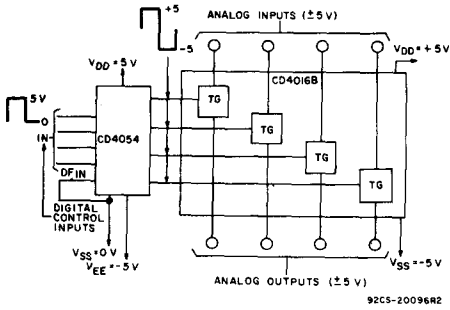


Fig. 18 — Digital (0 to +5 V) to bidirectional analog control (+5 to -5 V) level shifter.

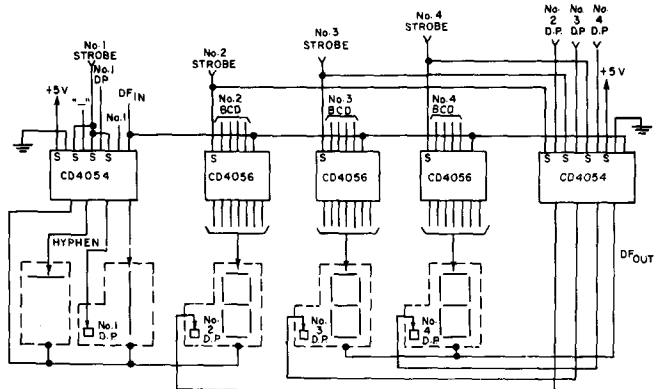


Fig. 19 — Typical 3 1/2-digit liquid-crystal display: $V_{DD} = +5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_{EE} = -10\text{ V}$, $DF_{IN} = 30\text{ Hz}$ square wave.

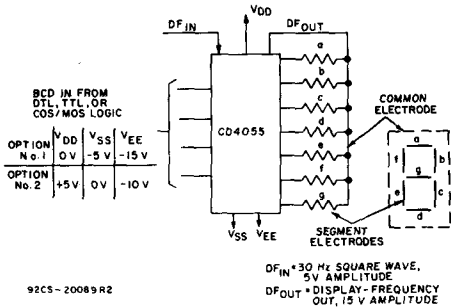


Fig. 20 — Single-digit liquid-crystal display.

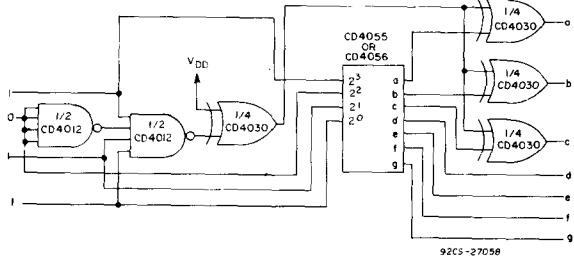
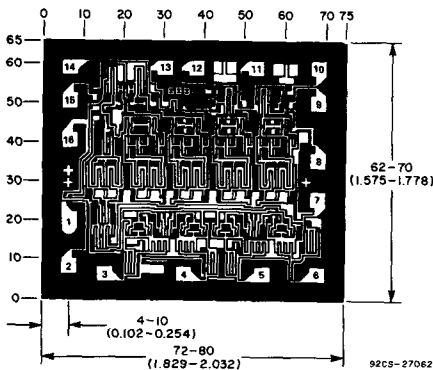


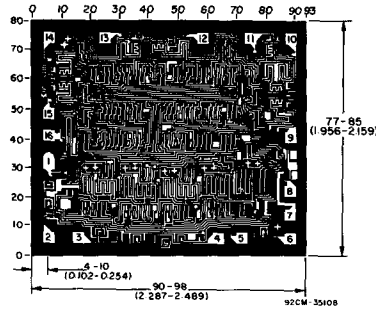
Fig. 21 — Conversion of "H" display to "F" display.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

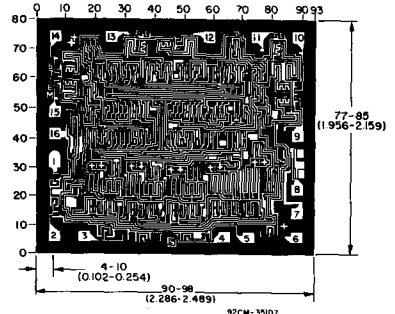
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Dimensions and pad layout for CD4054BH.



Dimensions and pad layout for CD4055BH



Dimensions and pad layout for CD4056BH

In addition to the letters L, H, P, and A (See the truth table), five other letters can be displayed through the use of simple logic circuits preceding and following the CD4055B or CD4056B devices. Fig. 21 is an example of a circuit that converts an "H" display (code 1011) to an "F" display. One condition that must be met is that $V_{EE} = V_{SS}$. If $V_{EE} \neq V_{SS}$, the CD4054B must be used to level shift in the appropriate places.

In a similar manner the letters C, E, J, and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive.

The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is pre-knowledge that only letters are to be displayed.