CD4062A Types

CMOS 200-Stage Dynamic Shift Register

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES K, T, H ..... -55 to +125°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55 to +100°C (PACKAGE TYPES K, T) ..... 500 mW

For T_A = +100 to +125°C (PACKAGE TYPES K, T) ..... Derate Linearly at 12 mW/°C to 200 mW

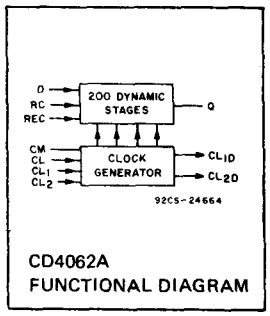
DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



CD4062A
FUNCTIONAL DIAGRAM

The RCA-CD4062A is a 200-stage dynamic shift register with provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended for low-power, low clock-line capacitance requirements. Single-phase clocking is specified for medium-speed operation (< 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (< 5 pF), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise and fall time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 pF/phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL_1 for two-phase operation.

The CD4062A-Series types are supplied in 12-lead hermetic TO-5 packages (T suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Minimum shift rates over full temperature range—**

  Single-phase clock: $3 V \leq V_{DD} \leq 10 V$; f_{min} = 10 kHz; $-55° C \leq T_A \leq +125° C$ (f_{min} = 1 kHz up to $T_A \leq 75° C$)

  Two-phase clock: $3 V \leq V_{DD} \leq 15 V$; f_{min} = 10 kHz; $-55° C \leq T_A \leq +125° C$ (f_{min} = 1 kHz up to $T_A \leq 75° C$)

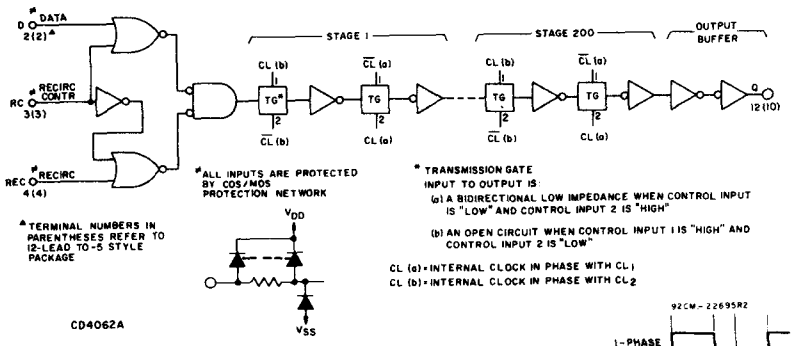


Fig. 1 – CD4062A logic block diagram.

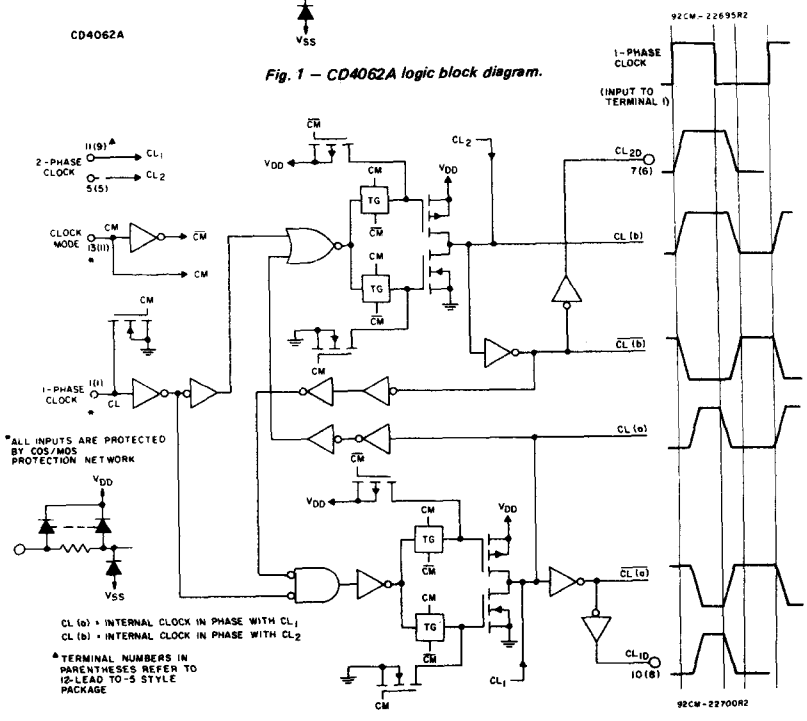


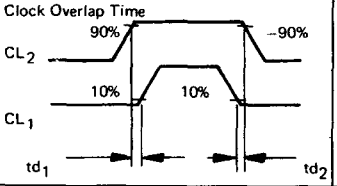
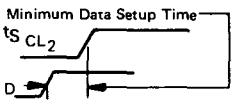
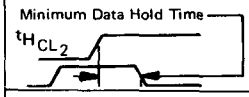
Fig. 2 – Clock circuit logic diagram.

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range):				
Single-Phase Clock		3	10	V
Two-Phase Clock		3	12	V
Clock Input Frequency, f_{CL}*	5	0.15	500	kHz
	10	0.15	1000	kHz
Clock Pulse Width, t_W*	5	250	66.7 X 10^6	ns
	10	500	66.7 X 10^6	ns
Clock Rise or Fall Times, t_rCL or t_fCL*	5	–	10	μs
	10	–	1	μs
Data Hold Time, t_H*	5	150	–	ns
	10	50	–	ns

* For single-phase clock, 50% duty cycle

Two-Phase Clock Operation (CL_1, CL_2); Clock Mode (CM) = High; 3 V ≤ V_{DD} ≤ 15 V. See Figure 4.

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL}	5	1.25	2.5	–	MHz
	10	2.5	5	–	MHz
Minimum Clock Input Frequency, f_{CL}	5	150	10	–	Hz
	10	150	10	–	Hz
Clock Overlap Time 		40	–	–	ns
Average Input Capacitance, C_I CL_1, CL_2		–	50	–	pF
Propagation Delays; t_{PHL}, t_{PLH} CL_1 to Q	5	–	250	500	ns
	10	–	100	200	ns
CL_1 to CL_{1D} CL_2 to CL_{2D}	5	–	250	500	ns
	10	–	100	200	ns
Minimum Data Setup Time 	5	–	150	300	ns
	10	–	50	100	ns
Minimum Data Hold Time 	5	–	–	0	ns
	10	–	–	0	ns
Clock Rise and Fall Times t_rCL_1, CL_2 t_fCL_1, CL_2		No Restrictions If Clock Overlap Requirement Is Met			

Features (Cont'd):

- Low power dissipation
  0.3 mW/bit at 1 MHz and 10 V
  0.04 mW/bit at 0.5 MHz and 5V
  (alternating 1-0 data pattern)
- Data output TTL-DTL compatible
- Recirculating capability
- Delayed two-phase clock outputs available for cascading registers
- Asynchronous ripple-type presettable to all 1's or 0's
- Ultra-low-power-dissipation standby operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Serial shift registers
- Time-delay circuits
- CRT refresh memory
- Long serial memory

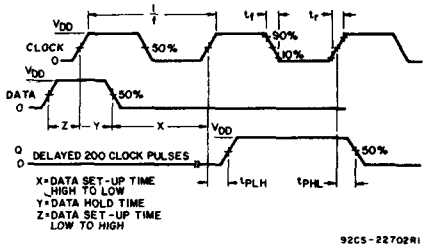


Fig. 3 – Timing diagram–single-phase clock.

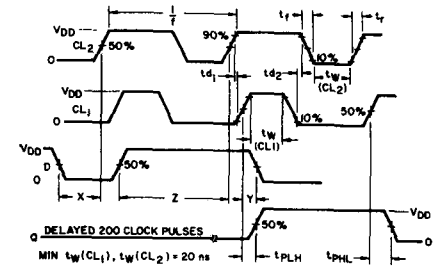


Fig. 4 – Timing diagram–two-phase clock.

CD4062A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) -55	+25 TYP.	+25 LIMIT	+125	UNITS
Quiescent Device Current, I_L Max.		–	–	5	12	0.5	12	720	μA
		–	–	10	25	1	25	1500	
CM=High, CL_1=High, CL_2=Low		–	–	15	50	1	50	2000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max				V
		–	10	10	0 Typ.; 0.05 Max				
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.				
		–	0	10	9.95 Min.; 10 Typ.				
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.				V
		9	–	10	3 Min.; 4.5 Typ.				
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.				
		1	–	10	3 Min.; 4.5 Typ.				
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.				V
		9	–	10	1 Min.				
Inputs High, V_{NMH}		0.5	–	5	1 Min.				
		1	–	10	1 Min.				
Output Drive Current: N-Channel (Sink), I_DN Min.	Q	0.4	–	4.5	1.6	2.6	1.3	0.91	mA
	Output	0.5	–	10	5	8*	4	3.2	
	CL_{1D},	0.5	–	5	0.87	1.4	0.7	0.49	
	CL_{2D}	0.5	–	10	2.2	3.6	1.8	1.26	
P-Channel (Source):		4.5	–	5	-0.31	-0.5	-0.25	-0.17	mA
I_DP Min.	Q	2.5	–	5	-0.93	-1.5	-0.75	-0.52	
	Output	9.5	–	10	-0.87	-1.4	-0.7	-0.49	
	CL_{1D},	4.5	–	5	-0.43	-0.7	-0.35	-0.24	
	CL_{2D}	9.5	–	10	-1.1	-1.8	-0.9	-0.63	
Input Leakage Current, I_{IL}, I_{IH}		Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.				μA

* Maximum power dissipation rating ⩽ 200 mW.

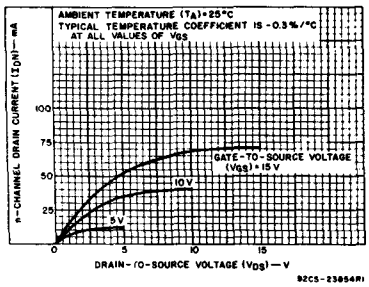


Fig. 5— Typical n-channel drain characterstics for Q output.

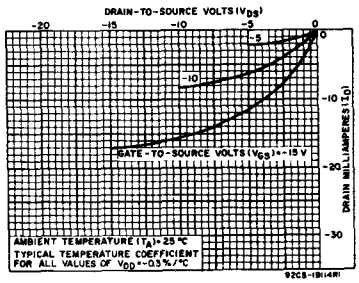


Fig. 6— Typical p-channel drain characteristics for Q output.

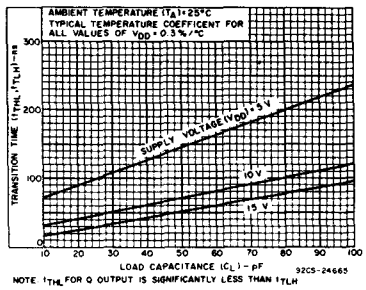


Fig. 7— Typical transition time vs. C_L for data outputs.

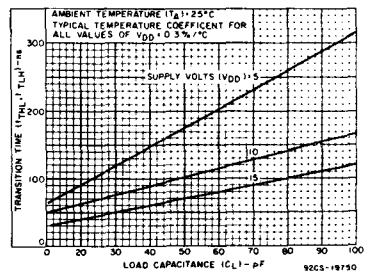
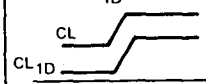
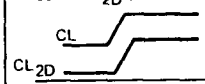
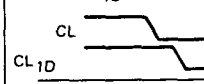
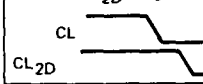
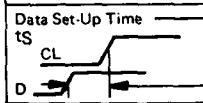
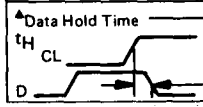


Fig. 8— Typical transition time vs. C_L for delayed clock output.

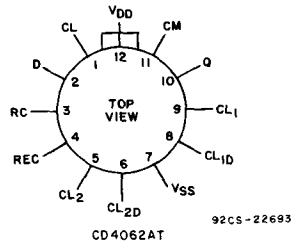
DYNAMIC CHARACTERISTICS AT T_A = 25°C, V_{SS} = 0 V, C_L = 50 pF, Input t_r, t_f = 20 ns, except t_rCL and t_fCL

Single-Phase-Clock Operation; Clock Mode (CM) = Low; 3 V ≤ V_{DD} ≤ 10 V (See Figure 3)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL} (50% Duty Cycle)	t_r, t_f=20 ns	5	0.5	1	–	MHz
		10	1	2	–	
Minimum Clock Input Frequency, f_{CL} (50% Duty Cycle)		5	150	10	–	Hz
		10	150	10	–	
Clock Rise and Fall Times** t_rCL, t_fCL		5	–	–	10	μs
		10	–	–	1	
Average Input Capacitance, C_I	All Inputs Except CL_1 and CL_2		–	5	–	pF
Propagation Delays: CL to Q		5	–	1000	2000	ns
		10	–	400	800	
CL to CL_{1D} (Positive Going) 	(50% Points)	5	–	750	1500	ns
		10	–	300	600	
CL to CL_{2D} (Positive Going) 	(50% Points)	5	–	500	1000	
		10	–	200	400	
CL to CL_{1D} (Negative Going) 	(50% Points)	5	–	450	900	
		10	–	175	350	
CL to CL_{2D} (Negative Going) 	(50% Points)	5	–	750	1500	
		10	–	300	600	
Transition Time: t_{TLH}, t_{THL} Q Output		5	–	100	200	ns
		10	–	50	100	
CL_{1D}, CL_{2D}		5	–	200	400	
		10	–	100	200	
Data Set-Up Time t_S 		5	–	–	0	ns
		10	–	–	0	
▲Data Hold Time t_H 		5	–	–	150	ns
		10	–	–	150	

** If more than one unit is cascaded in single-phase parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF, and the transition time of the output driving stage. (See Figs. 5 and 7 for cascading options.)

▲ Use of delayed clock permits high-speed logic to precede CD4062A register (see cascade register operation).



CD4062AT

TERMINAL DIAGRAM

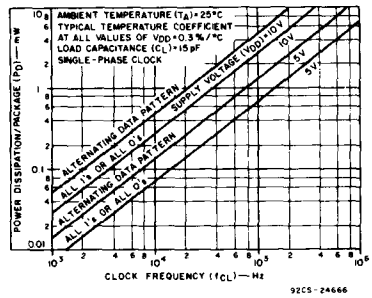


Fig. 9— Typical power dissipation vs. frequency.

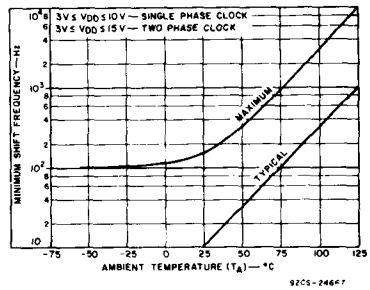


Fig. 10— Minimum shift frequency vs. ambient temperature.

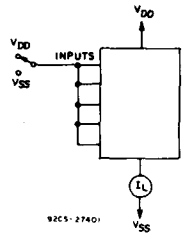


Fig. 11— Quiescent-device-current test circuit.

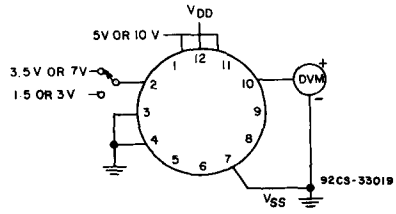


Fig. 12— Noise-immunity test circuit.

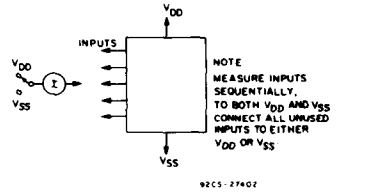


Fig. 13—Input-leakage-current test circuit.