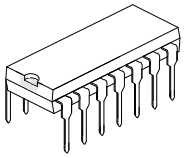
CD4066

CMOS IC

QUAD BILATERAL SWITCH



DIP-14

■ DESCRIPTION

The UTC **CD4066** is a quad bilateral switch which can be applied for switching of analog signals and digital signals. When control input CONT is set to “H” level, the impedance between input and output of the switch becomes low and when it is set to “L” level, the impedance becomes high. It has a much lower “ON” resistance, and “ON” resistance is relatively constant over the input-signal range.

■ FEATURES

* 15V Digital or ±7.5V Peak-to-Peak Switching
* 85-Ω Typical On-State Resistance for 15V Operation
* High noise immunity 0.45 V_{DD} (typ.)
* Matched “ON” resistance ΔR_{ON}=5Ω (typ.) over 15V signal input
* High degree linearity 0.1% distortion (typ.)
  @ f_{IS}=1kHz, V_{IS}=5V_{P-P}, V_{DD}-V_{SS}=5V, R_L=10kΩ
* Extremely low “OFF” 0.1nA (typ.)
  switch leakage: @ V_{DD}-V_{SS}=10V, T_A=25°C
* Extremely high control input impedance 10^{12}Ω (typ.)
* Frequency response, switch “ON” 40 MHz (typ.)

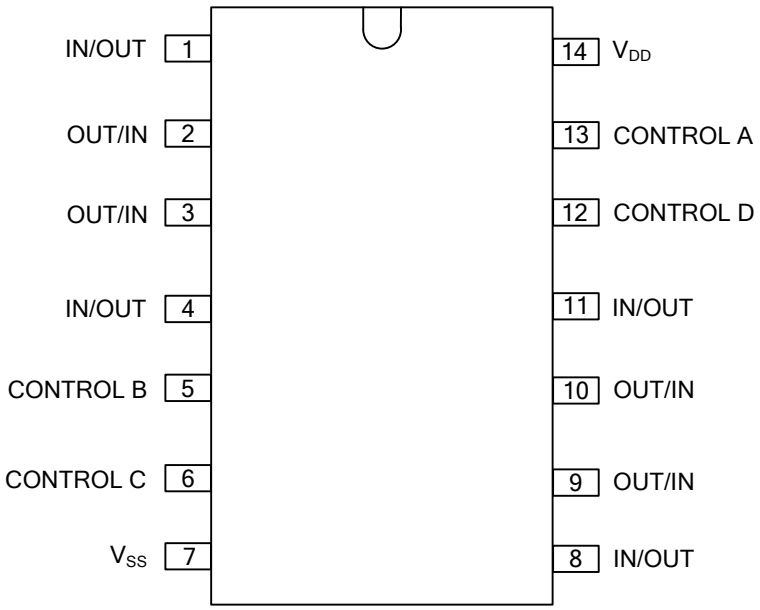
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
CD4066L-D14-T	CD4066G-D14-T	DIP-14	Tube

CD4066L-D14-T
- (1)Packing Type
- (2)Package Type
- (3)Lead Free

(1) T: Tube
(2) D14: DIP-14
(3) G: Halogen Free, L: Lead Free

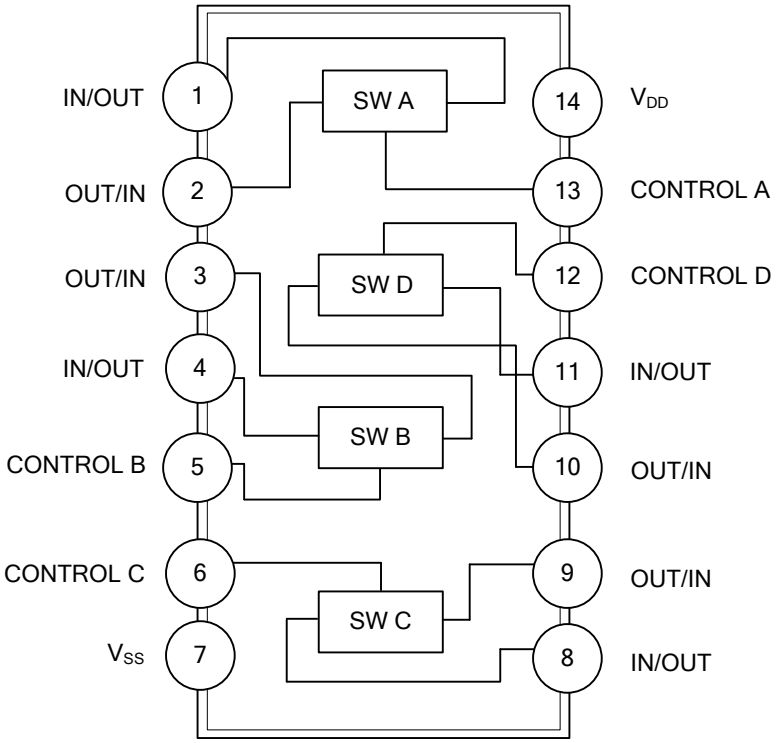
■ PIN CONFIGURATION



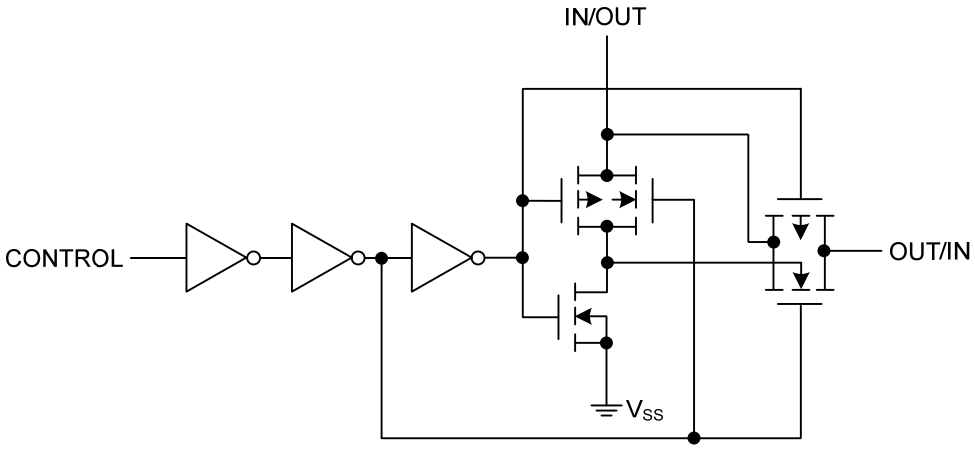
■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	IN/OUT	Signal IN/OUT A
2	OUT/IN	Signal OUT/IN A
3	OUT/IN	Signal OUT/IN B
4	IN/OUT	Signal IN/OUT B
5	CONTROL B	CONTROL B
6	CONTROL C	CONTROL C
7	V_{SS}	Ground
8	IN/OUT	Signal IN/OUT C
9	OUT/IN	Signal OUT/IN C
10	OUT/IN	Signal OUT/IN D
11	IN/OUT	Signal IN/OUT D
12	CONTROL D	CONTROL D
13	CONTROL A	CONTROL A
14	V_{DD}	Power supply

■ BLOCK DIAGRAM



■ SCHEMATIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (V_{SS}=0V unless otherwise specified.)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5~+18	V
Input Voltage	V_{IN}	-0.5~ V_{CC}+0.5	V
Power Dissipation	P_D	700	mW
Storage Temperature	T_{STG}	-65~+150	°C

■ RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V unless otherwise specified.)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	3~15	V
Input Voltage	V_{IN}	0~V_{DD}	V
Operating Temperature	T_A	-40~+85	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ DC ELECTRICAL CHARACTERISTICS (T_A=+25°C, V_{SS}=0V unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Quiescent Device Current	I_{DD}	V_{IN}=V_{DD}	V_{DD}=5V		0.01	1.0	μA
			V_{DD}=10V		0.01	2.0	
			V_{DD}=15V		0.01	4.0	
SINGAL INPUTS AND OUTPUTS							
"ON" Resistance	R_{ON}	R_L=10kΩ~(V_{DD}-V_{SS}/2), V_{CON}=V_{DD},V_{SS}~V_{DD}	V_{DD}=5V		240	1050	Ω
			V_{DD}=10V		120	400	
			V_{DD}=15V		80	240	
Δ"ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	R_L=10kΩ~(V_{DD}-V_{SS}/2), V_{CC}=V_{DD}, V_{IS}=V_{SS}~V_{DD}	V_{DD}=10V		10		Ω
			V_{DD}=15V		5		
Input or Output Leakage Switch "OFF"	I_{IS}	V_{CON}=0			±0.1	±50	nA
CONTROL INPUTS							
LOW Level Input Voltage	V_{ILC}	V_{IS}=V_{SS} and V_{DD}, V_{OS}=V_{DD} and V_{SS}, I_{IS}=±10μA	V_{DD}=5V		2.25	1.5	V
			V_{DD}=10V		4.5	3.0	
			V_{DD}=15V		6.75	4.0	
HIGH Level Input Voltage	V_{IHC}	V_{DD}=5V		3.5	2.75		V
		V_{DD}=10V (Note 5)		7.0	5.5		
		V_{DD}=15V		11.0	8.25		
Input Current	I_{IN}	V_{DD}-V_{SS}=15V, V_{DD}≥V_{IS}≥V_{SS}, V_{DD}≥V_{CON}≥V_{SS}			±10^{-5}	±0.3	μA

■ AC ELECTRICAL CHARACTERISTICS

(T_A=25°C, t_R=t_F=20nS and V_{SS}=0V, unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay Time Signal	t_{PHL}, t_{PLH}	V_{CON}=V_{DD}, C_L=5pF, R_L=200kΩ (Fig. 1)	V_{DD}=5V		25	55	ns
			V_{DD}=10V		15	35	ns
			V_{DD}=15V		10	25	ns
Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	t_{PZH}, t_{PZL}	R_L=1kΩ, C_L=50pF, (Fig. 2, 3)	V_{DD}=5V			125	ns
			V_{DD}=10V			60	ns
			V_{DD}=15V			50	ns
Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	t_{PHZ}, t_{PLZ}	R_L=1kΩ, C_L=50pF, (Fig. 2, 3)	V_{DD}=5V			125	ns
			V_{DD}=10V			60	ns
			V_{DD}=15V			50	ns
Sine Wave Distortion		V_{CON}=V_{DD}=5V, V_{SS}=-5V, R_L=10kΩ, V_{IS}=5V_{p-p}, f=1kHz (Fig. 4)			0.1		%
Frequency Response-Switch “ON” (Frequency at -3dB)		V_{CON}=V_{DD}=5V, V_{SS}=-5V, R_L=1kΩ, 20 Log_{10}(V_{OS}/V_{IS})=-3dB, V_{IS}=5.0V_{p-p} (Fig. 4)			40		MHz
Feedthrough - Switch “OFF” (Frequency at -50dB)		V_{DD}=5.0V, V_{CC}=V_{SS}=-5.0V, R_L=1kΩ, V_{IS}=5.0V_{p-p}, 20 Log_{10}(V_{OS}/V_{IS})=-50dB (Fig. 4)			1.25		MHz
Crosstalk Between Any Two Switches (Frequency at -50dB)		V_{DD}=$V_{CON(A)}$=5.0V, R_L=1kΩ, V_{SS}=$V_{CON\ (B)}$=5.0V, $V_{IS(A)}$=5.0V_{p-p}, 20 Log_{10}($V_{OS(B)}$/$V_{IS(A)}$)=-50dB(Fig. 5)			0.9		MHz
Crosstalk, Control Input to Signal Output		V_{DD}=10V, R_L=10kΩ, R_{IN}=1kΩ, V_{CC}=10V Square Wave, C_L=50pF (Fig. 6)			150		mV_{P-P}
Maximum Control Input		R_L=1kΩ, C_L=50pF, $V_{OS(f)}$=½ V_{OS}(1kHz) (Fig. 7)	V_{DD}=5V		6		MHz
			V_{DD}=10V		8		MHz
			V_{DD}=15V		8.5		MHz
Signal Input Capacitance	C_{IS}				8.0		pF
Signal Output Capacitance	C_{OS}	V_{DD}=10V			8.0		pF
Feedthrough Capacitance	C_{IOS}	V_{CON}=0V			0.5		pF
Control Input Capacitance	C_{IN}				5.0	7.5	pF

Notes: 1. AC Parameters are guaranteed by DC correlated testing.
2. These devices should not be connected to circuits with the power “ON”.
3. In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.
4. V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_{CON} is the voltage at the control input.
5. Conditions for V_{IHC}:
   a) V_{IS}=V_{DD}, I_{OS}=standard B series I_{OH}
   b) V_{IS}=0V, I_{OL}= standard B series I_{OL}

■ SPECIAL CONSIDERATION

Using continuously under heavy loads may cause UTC **CD4066** to decrease in the reliability even if the operating conditions are within the absolute maximum ratings and the operating ranges.

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L. This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from UTC **CD4066**.

■ AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

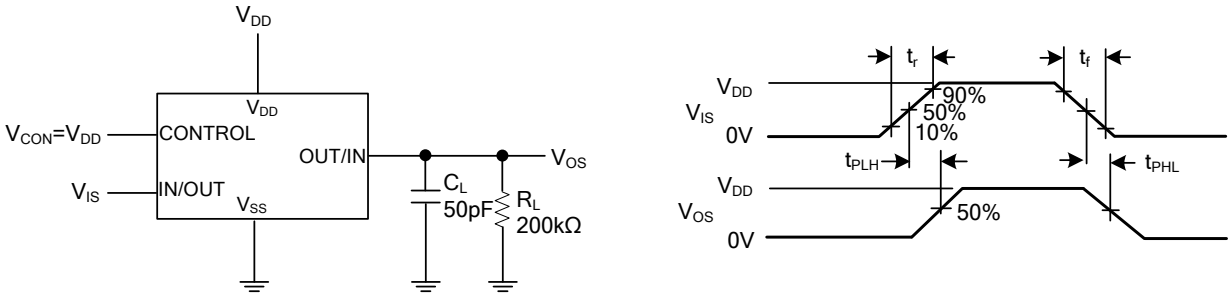


Fig. 1 t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

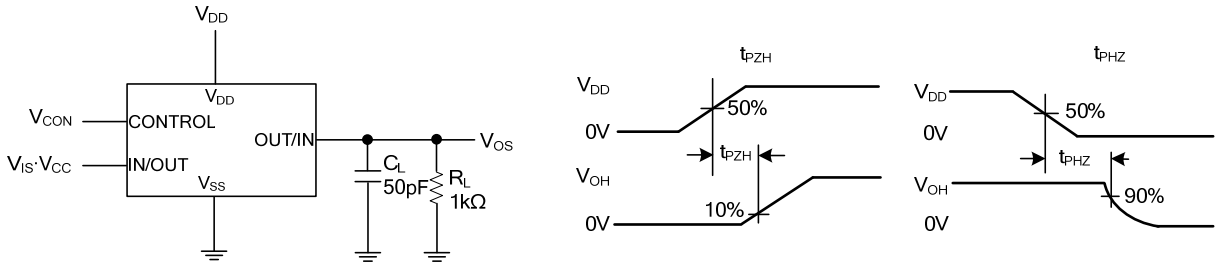


Fig. 2 t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

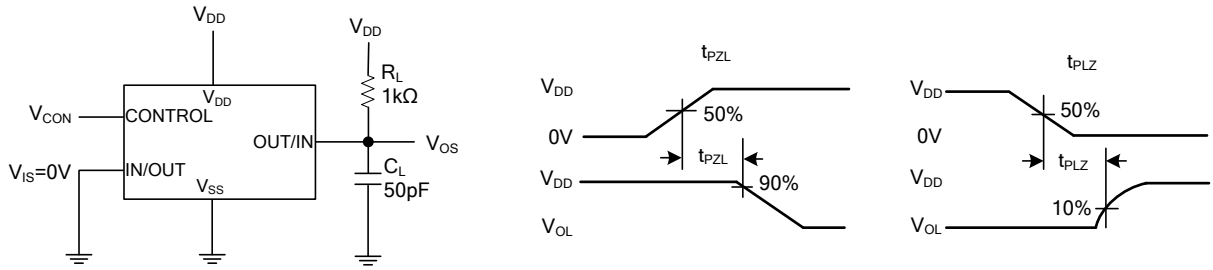
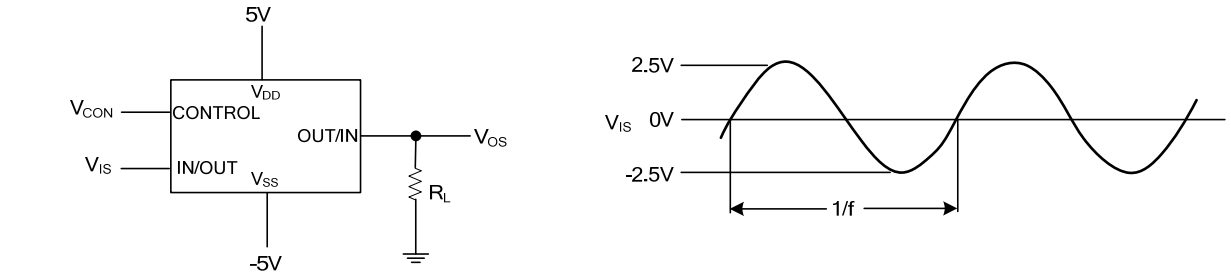


Fig. 3 t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

■ AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS(Cont.)



V_{CON}=V_{DD} for distortion and frequency response tests
V_{CON}=V_{SS} for feedthrough test

Fig. 4 Sine Wave Distortion, Frequency Response and Feedthrough

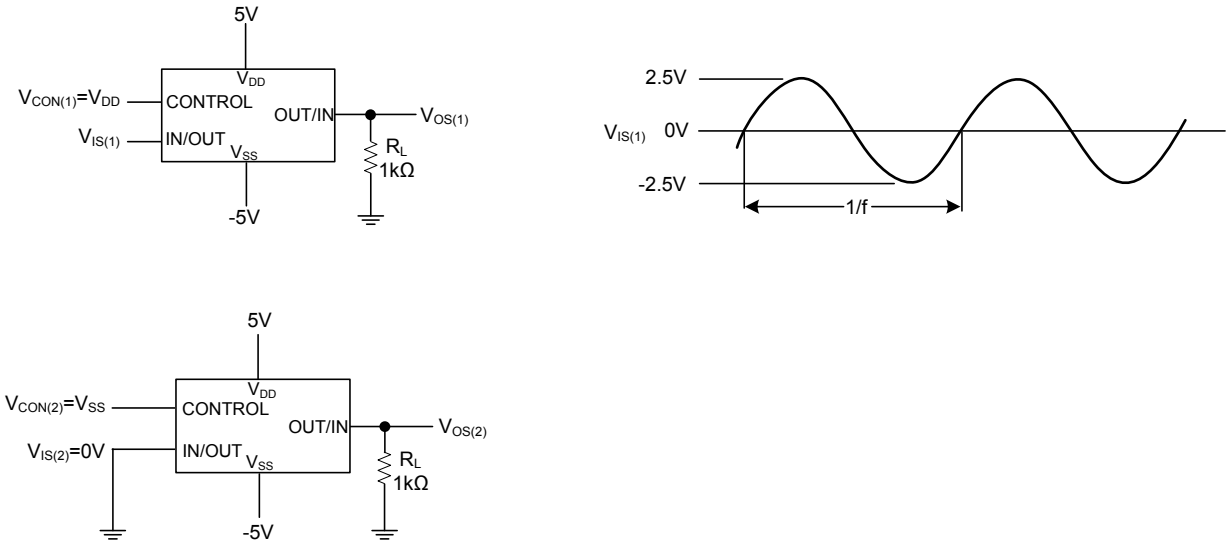


Fig. 5 Crosstalk Between Any Two Switches

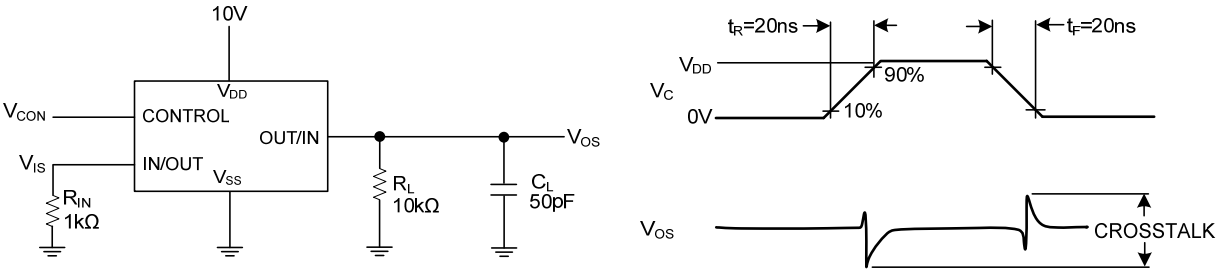


Fig. 6 Crosstalk: Control Input to Signal Output

■ AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS(Cont.)

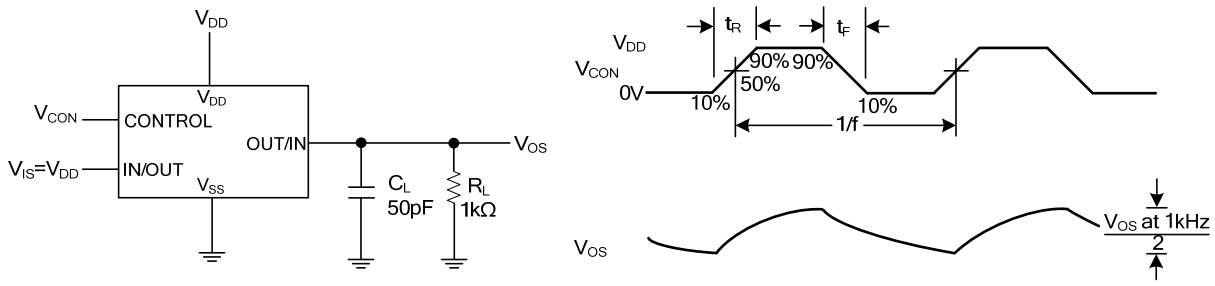


Fig. 7 Maximum Control Input Frequency