

# CD4066A Types

## CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

RCA CD4066A is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to  $V_{SS}$  when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016 is recommended.

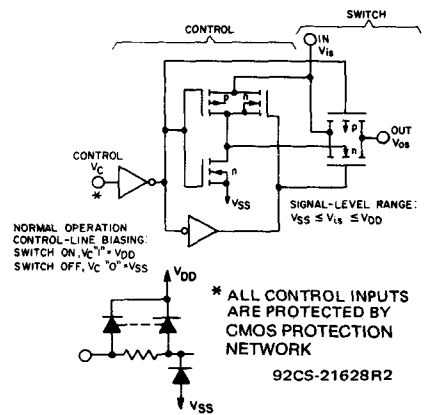
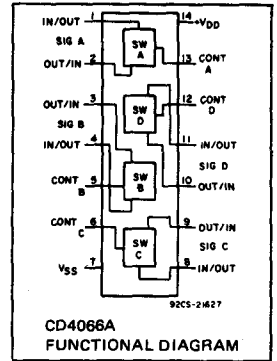
These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

### SPECIAL CONSIDERATIONS - CD4066A

- In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from CD4066A.
- In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from  $R_{ON}$  values shown).
- No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminals 2, 3, 9, or 10.
- Minimum bilateral switch output load resistance is 100  $\Omega$ .

### Features:

- 15-V digital or  $\pm 7.5$ -V peak-to-peak switching
- 80 $\Omega$  typical ON resistance for 15-V operation
- Switch ON resistance matched to within 5  $\Omega$  over 15-V signal-input range
- ON resistance flat over full peak-to-peak signal range
- High ON/OFF output-voltage ratio: 65 dB typ. @  $f_{is} = 10$  kHz,  $R_L = 10$  k $\Omega$
- High degree of linearity: < 0.5% distortion typ. @  $f_{is} = 1$  kHz,  $V_{is} = 5$  V<sub>p-p</sub>,  $V_{DD} - V_{SS} \geq 10$  V,  $R_L = 10$  k $\Omega$
- Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @  $V_{DD} - V_{SS} = 10$  V,  $T_A = 25^\circ\text{C}$
- Extremely high control input impedance (control circuit isolated from signal circuit):  $10^{12}$   $\Omega$  typ.
- Low crosstalk between switches: -50 dB typ. @  $f_{is} = 0.9$  MHz,  $R_L = 1$  k $\Omega$
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch ON = 40 MHz (typ.)
- Quiescent current specified to 15-V
- Maximum control input leakage current of 1- $\mu$ A at 15-V (Full package-temperature range)



### MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	-65 to +125 $^\circ\text{C}$
OPERATING TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPES D, F, K, H	-55 to +125 $^\circ\text{C}$
PACKAGE TYPE E	-40 to +85 $^\circ\text{C}$
DC SUPPLY VOLTAGE RANGE, $V_{DD}$ (Voltages referenced to $V_{SS}$ )	-0.5 to +15 V
INPUT CURRENT (TRANSMISSION GATE INCL.)	$\pm 10$ mA
POWER DISSIPATION PER PACKAGE:	
FOR $T_A = -40$ to +60 $^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85 $^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 12 mW/ $^\circ\text{C}$	200 mW
FOR $T_A = -55$ to +100 $^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125 $^\circ\text{C}$ (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/ $^\circ\text{C}$	200 mW
DEVICE DISSIPATION PER SECTION:	
FOR $T_A = \text{FULL PACKAGE TEMPERATURE RANGE (ALL PACKAGE TYPES)}$	100 mW
ALL SIGNAL AND DIGITAL CONTROL INPUTS	$V_{SS} \leq V_i \leq V_{DD}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79 mm) from case for 10 s max.	+265 $^\circ\text{C}$

### OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	$V_{DD}$	MIN.	MAX.	UNITS
Supply Voltage Range ( $T_A = \text{Full Package Temperature Range}$ )	-	3	12	V

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## Applications:

- Analog signal switching/multiplexing
  - Signal gating
  - Modulator
  - Squelch control
  - Demodulator
  - Chopper
  - Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

## ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS All Voltage Values Are in Volts		LIMITS						UNITS	
			Values at -55°C, +25°C, +125°C Apply to D, F, K, H Packages							
			Values at -40°C, +25°C, +85°C Apply to E Package							
	V <sub>DD</sub> (V)	-55°	-40°	+85°	+125°	+25°				
						TYP.	MAX.			
Quiescent Device Current, <i>I</i> <sub>L</sub> max. D, F, H Pkgs.	5	0.25	-	-	7.5	0.01	0.25	μA		
	10	0.5	-	-	15	0.01	0.5	μA		
	15	2	-	-	40	0.02	2	μA		
E Pkg.	5	-	2.5	15	-	0.25	2.5	μA		
	10	-	5	30	-	0.25	5	μA		
	15	-	50	500	-	0.5	50	μA		
SIGNAL INPUTS (V <sub>is</sub> ) AND OUTPUTS (V <sub>os</sub> )										
ON Resistance, R <sub>ON</sub> Max.	V <sub>C</sub> = V <sub>DD</sub>	V <sub>SS</sub>	V <sub>is</sub>							
	R <sub>L</sub> = 10kΩ*			220	250	300	320	80	280	Ω
	+7.5	-7.5	-7.5 to +7.5							
	+15	0	0 to +15							
	+5	-5	-5 to +5	400	450	520	550	120	500	
	+10	0	0 to +10							
	+2.5	-2.5	-2.5 to +2.5	3000	3500	5200	5500	270	5000	
-5	0	0 to +5								
Δ ON Resistance Between Any 2 of 4 Switches, Δ R <sub>ON</sub>	R <sub>L</sub> = 10kΩ*						5	-	Ω	
	+7.5	-7.5	+7.5 to -7.5							
	+15	0	+15 to 0							
Sine Wave Response (Distortion)	R <sub>L</sub> = 10kΩ f <sub>is</sub> = 1kHz						0.4	-	%	
	+5	-5	-5 p-p							
Frequency Response Switch ON (Sine-Wave Input)	R <sub>L</sub> = 1kΩ						40	-	MHz	
	20 log <sub>10</sub> $\frac{V_{os}}{V_{is}}$ = -3dB									
Feedthrough-Switch OFF	R <sub>L</sub> = 1kΩ						1.25	-	MHz	
	20 log <sub>10</sub> $\frac{V_{os}}{V_{is}}$ = -50dB									
Input or Output Leakage – Switch OFF (Effective OFF Resistance)	V <sub>DD</sub>	V <sub>C</sub> = V <sub>SS</sub>					±0.1	±100*	nA	
	+7.5	-7.5	±7.5							
	+5	-5	±5				±0.1	±100*		
Crosstalk Between Any 2 of the 4 Switches (f at -50 dB)	V <sub>C</sub> (A) = V <sub>DD</sub> +5 V <sub>C</sub> (B) = V <sub>SS</sub> -5 R <sub>L</sub> = 1kΩ		(A) 5V p-p				0.9	-	MHz	
	20 log <sub>10</sub> $\frac{V_{os}(B)}{V_{is}(A)}$ = -50dB									

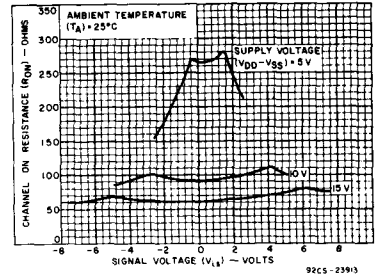


Fig. 2 (a) – Typical channel ON resistance vs. signal voltage for three values of supply voltage (V<sub>DD</sub> - V<sub>SS</sub>) = 5V.

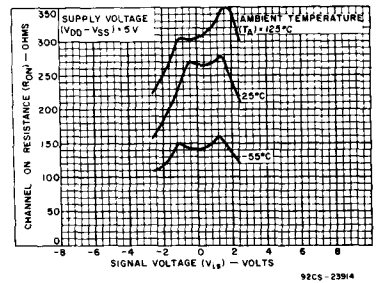


Fig. 2 (b) – Typical channel ON resistance vs. signal voltage with supply voltage (V<sub>DD</sub> - V<sub>SS</sub>) = 5V.

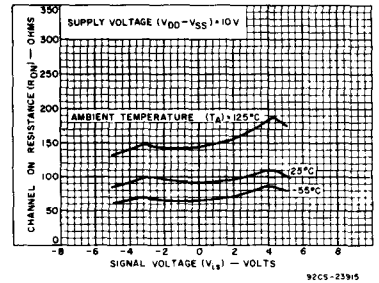


Fig. 2 (c) – Typical channel ON resistance vs. signal voltage with supply voltage (V<sub>DD</sub> - V<sub>SS</sub>) = 10V.

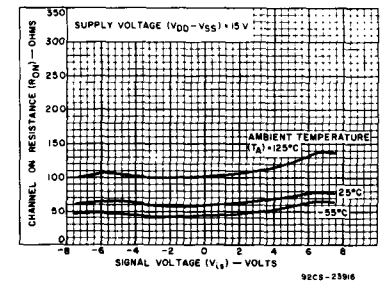


Fig. 2 (d) – Typical channel ON resistance vs. signal voltage with supply voltage (V<sub>DD</sub> - V<sub>SS</sub>) = 15V.

# CD4066A Types

## ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS All Voltage Values Are in Volts	LIMITS						UNITS
		Values at -55°C, +25°C, +125°C Apply to D, F, K, H Packages Values at -40°C, +25°C, +85°C Apply to E Package						
		V <sub>DD</sub> (V)		-55°	-40°	+85°	+125°	
						TYP.	MAX.	
Propagation Delay (Signal Input to Signal Output) <i>t</i> <sub>pd</sub>	V <sub>DD</sub> = 5 V <sub>SS</sub> = GND C <sub>L</sub> = 15pF V <sub>is</sub> = sq. wave	-	-	-	-	20	50	ns
	V <sub>DD</sub> = 10 <i>t</i> <sub>r</sub> , <i>t</i> <sub>f</sub> = 20 ns (Input Signal)	-	-	-	-	10	25	
Capacitance: Input, C <sub>is</sub> Output, C <sub>os</sub> Feedthrough, C <sub>ios</sub>	V <sub>DD</sub> = +5 V <sub>CC</sub> = V <sub>SS</sub> = -5	-	-	-	-	8	-	pF
		-	-	-	-	8	-	
		-	-	-	-	0.5	-	
<b>CONTROL (V<sub>C</sub>)</b>								
Noise Immunity, V <sub>NL</sub> Min.	V <sub>is</sub> ≤ V <sub>DD</sub> I <sub>s</sub> = 10μA V <sub>DD</sub> - V <sub>SS</sub> = 10	2	2	2	2	2 min 4.5	-	V
Input Leakage Current, I <sub>IL</sub> Max.	V <sub>is</sub> ≤ V <sub>DD</sub> V <sub>DD</sub> - V <sub>SS</sub> = 15 V <sub>C</sub> ≤ V <sub>DD</sub> - V <sub>SS</sub>	-	-	±1	-	±10 <sup>-6</sup>	±1	μA
Crosstalk Control Input to Signal Output	V <sub>DD</sub> - V <sub>SS</sub> = 10 V <sub>C</sub> = 10 (sq. wave) R <sub>L</sub> = 10kΩ	-	-	-	-	50	-	mV
Propagation Delay, <i>t</i> <sub>pdC</sub>	<i>t</i> <sub>rc</sub> = <i>t</i> <sub>fc</sub> = 20 ns R <sub>L</sub> = 300kΩ V <sub>is</sub> ≤ 10 C <sub>L</sub> = 15pF	-	-	-	-	35	-	ns
Maximum Allowable Control Input Repetition Rate	V <sub>DD</sub> = 10, V <sub>SS</sub> = GND R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF V <sub>C</sub> = 10 (sq. wave) <i>t</i> <sub>r</sub> , <i>t</i> <sub>f</sub> = 20 ns	-	-	-	-	10	-	MHz
Av. Input Capacitance, C <sub>i</sub>		-	-	-	-	5	-	pF

\* Limit determined by minimum feasible leakage measurement for automatic testing.

Δ Symmetrical about 0 volts. • For all test conditions.

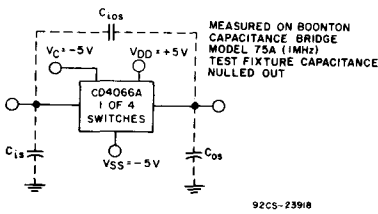


Fig. 6 - Capacitance test circuit.

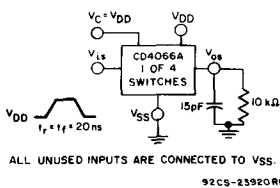


Fig. 8 - Propagation delay time signal input (V<sub>is</sub>) to signal output (V<sub>os</sub>).

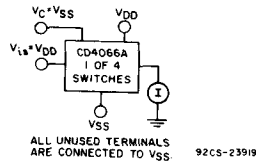


Fig. 7 - OFF switch input or output leakage.

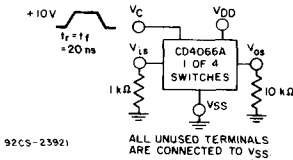


Fig. 9 - Crosstalk-control input to signal output.

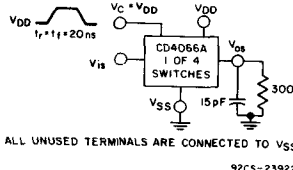


Fig. 11 - Propagation delay *t*<sub>PLH</sub>, *t*<sub>PHL</sub> control-signal output.

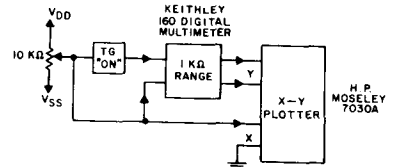


Fig. 3 - Channel ON resistance measurement circuit.

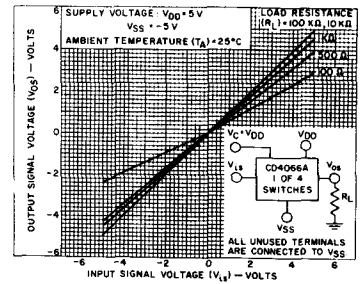


Fig. 4 - Typical ON characteristics for 1 of 4 channels.

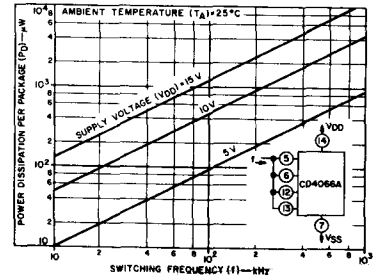


Fig. 5 - Power dissipation per package vs. switching frequency.

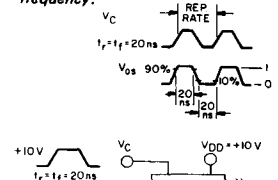


Fig. 10 - Maximum allowable control input repetition rate.

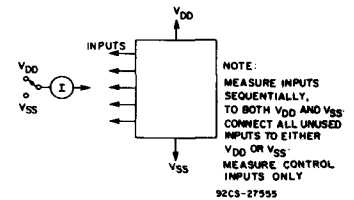


Fig. 12 - Input leakage current test circuit.