

CD4085B Types

CMOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (20-Volt Rating)

The RCA-CD4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

The CD4085B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation — $t_{PH} = 90$ ns; $t_{PL} = 125$ ns (typ.) at 10 V
- Individual inhibit controls
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of $1 \mu A$ at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

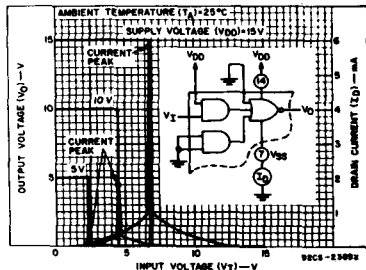
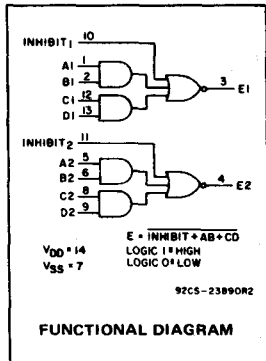


Fig. 1 — Typical voltage and current transfer characteristics.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	—0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	—0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ C$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ C$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ C$ to 200 mW
For $T_A = -55$ to $+100^\circ C$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ C$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ C$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	—55 to $+125^\circ C$
PACKAGE TYPE E	—40 to $+85^\circ C$
STORAGE TEMPERATURE RANGE (T_{stg})	—65 to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ C$

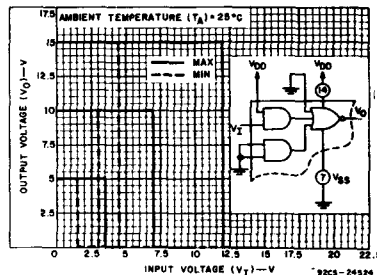
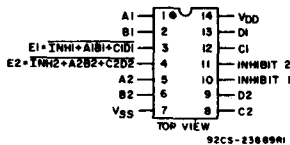


Fig. 2 — Min. and max. voltage transfer characteristics.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	3	18	V



Terminal Assignment

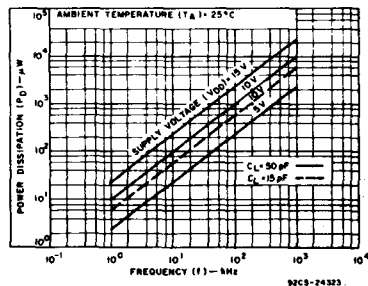


Fig. 3 — Typical power dissipation vs. frequency.

CD4085B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H Pkgs.				Values at -40, +25, +85 Apply to E Pkgs.			
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I _{DD} Max.	-	0,5	5	1	1	30	30	-	0.02	1	μA
	-	0,10	10	2	2	60	60	-	0.02	2	
	-	0,15	15	4	4	120	120	-	0.02	4	
	-	0,20	20	20	20	600	600	-	0.04	20	
Output Low (Sink) Current, I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
Output High (Source) Current, I _{OH} Min.	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	mA
	-	0,5	5	-	-	-	-	-	-	-	
	-	0,10	10	-	-	-	-	-	-	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	-	-	0.05	-	-	0	0.05	V
	-	0,10	10	-	-	0.05	-	-	0	0.05	
	-	0,15	15	-	-	0.05	-	-	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	-	-	4.95	-	4.95	5	-	V
	-	0,10	10	-	-	9.95	-	9.95	10	-	
	-	0,15	15	-	-	14.95	-	14.95	15	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	-	-	1.5	-	-	-	1.5	V
	1.9	-	10	-	-	3	-	-	-	3	
	1.5, 13.5	-	15	-	-	4	-	-	-	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	-	-	3.5	-	3.5	-	-	V
	1.9	-	10	-	-	7	-	7	-	-	
	1.5, 13.5	-	15	-	-	11	-	11	-	-	
Input Current, I _{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

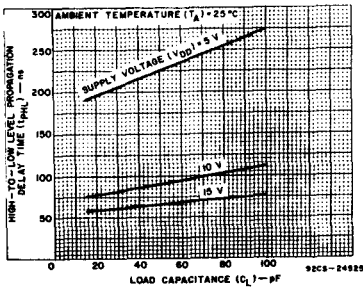


Fig. 4 - Typical data high-to-low level propagation delay time vs. load capacitance.

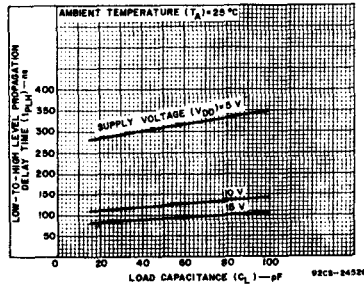


Fig. 5 - Typical data low-to-high level propagation delay time vs. load capacitance.

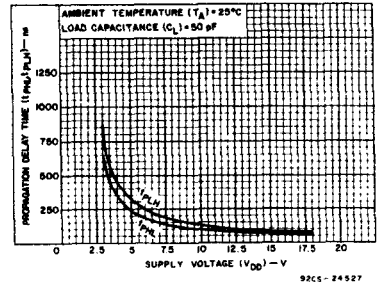


Fig. 6 - Typical data propagation delay time vs. supply voltage.

CD405B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS	
		V_{DD} V	Typ.		Max.
Propagation Delay Time (Data): High-to-Low Level, t_{PHL}		5	225	450	ns
		10	90	180	
		15	65	130	
Propagation Delay Time (Data): Low-to-High Level, t_{PLH}		5	310	620	ns
		10	125	250	
		15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level, t_{PHL}		5	150	300	ns
		10	60	120	
		15	40	80	
Propagation Delay Time (Inhibit): Low-to-High Level, t_{PLH}		5	250	500	ns
		10	100	200	
		15	70	140	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF	

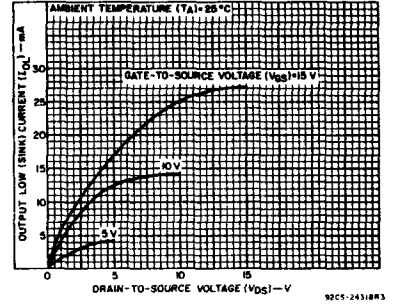


Fig. 7 - Typical output low (sink) current characteristics.

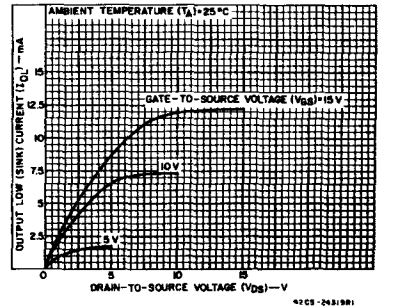


Fig. 8 - Minimum output low (sink) current characteristics.

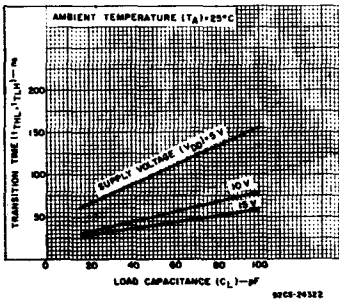


Fig. 9 - Typical transition time vs. load capacitance.

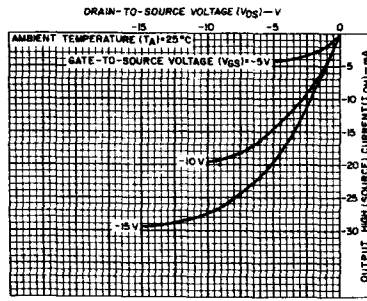


Fig. 10 - Typical output high (source) current characteristics.

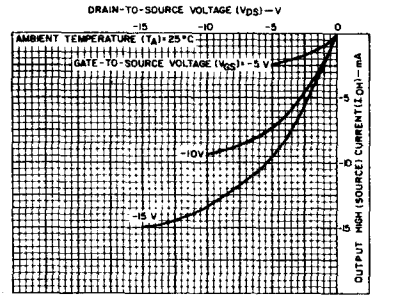


Fig. 11 - Minimum output high (source) current characteristics.

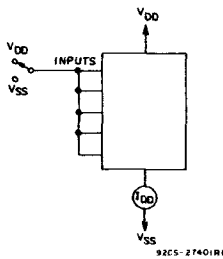


Fig. 12 - Quiescent device current test circuit.

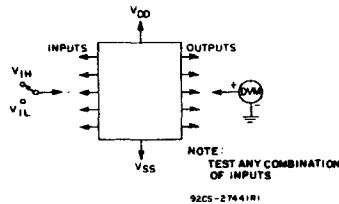


Fig. 13 - Input voltage test circuit.

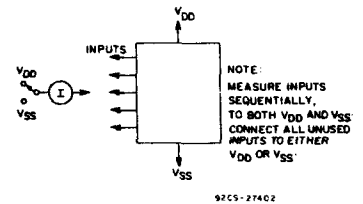


Fig. 14 - Input current test circuit.

CD4085B Types

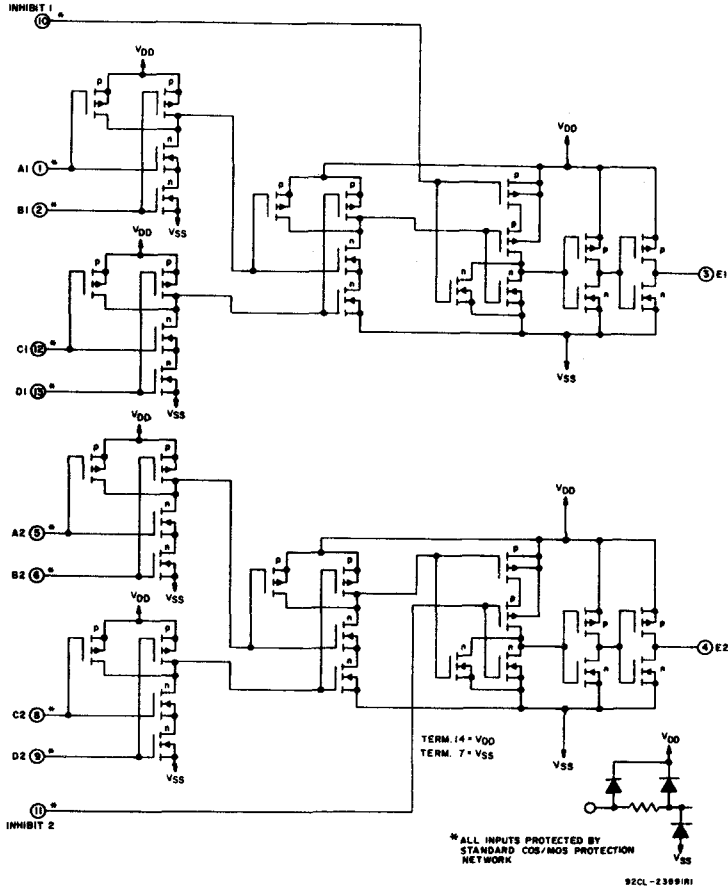
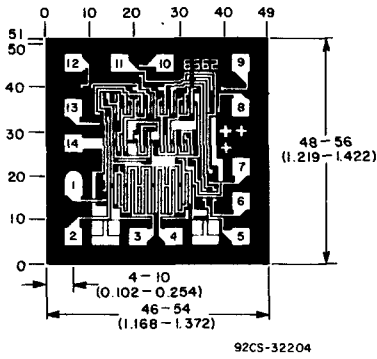


Fig. 15 - CD4085 schematic diagram.



92CS-32204

Dimensions and Pad Layout for CD4085BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.