National **S**emiconductor

CD4512BM/CD4512BC 8-Channel Buffered Data Selector

General Description

The CD4512BM/CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) input forces the output into the TRI-STATE condition. Low levels at both the Inhibit and ($\overline{\text{OE}}$) inputs allow normal operation.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- TRI-STATE output
- Low quiescent power dissipation — 0.25 μW/package (typ.) @ V_{CC} = 5.0V
- Plug-in replacement for Motorola MC14512

Connection Diagram and Truth Table

Dual-In-Line Package

Top View

TL/F/5993–1
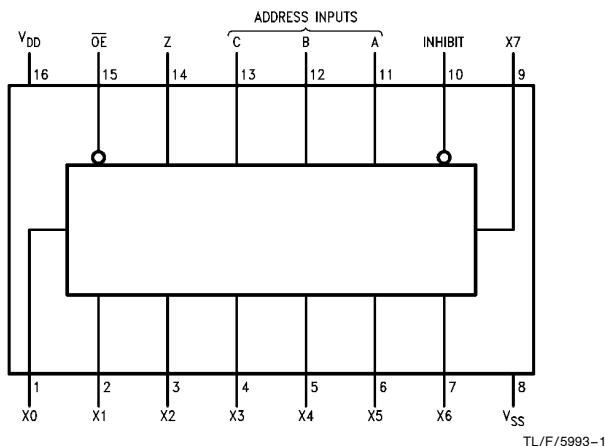
Order Number CD4512B

Address Inputs			Control Inputs		Output
C	B	A	Inhibit	$\overline{\text{OE}}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
①	①	①	1	0	0
①	①	①	①	1	Hi-Z

① = Don't care

Hi-Z = TRI-STATE condition

Xn = Data at input n

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD} + 0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$

Power Dissipation (P_D)
Dual-In-Line   700 mW
Small Outline   500 mW
Lead Temperature, (T_L)
(Soldering, 10 seconds)   260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3.0 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}

Operating Temperature Range (T_A)
CD4512BM $-55°C$ to $+125°C$
CD4512BC $-40°C$ to $+85°C$

DC Electrical Characteristics CD4512BM (Note 2)

Symbol	Parameter	Conditions	$-55°C$		$+25°C$			$+125°C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5.0		0.005	5.0		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.010	10		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ $\}$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ $\}$ $|I_{OL}| < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ $\}$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ $\}$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$ $\}$ $|I_{OH}| < 1\ \mu A$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$ $\}$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.78		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.0		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	-0.25		-0.2			-0.14		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-0.62		-0.5			-0.35		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-1.8		-1.5			-1.1		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	TRI-STATE Output Current	$V_{DD} = 15V$, $V_O = 0V$		± 0.1		-10^{-5}	± 0.1		± 3.0	μA
		$V_{DD} = 15V$, $V_O = 15V$								

DC Electrical Characteristics CD4512BC (Note 2)

Symbol	Parameter	Conditions	$-40°C$		$+25°C$			$+85°C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.005	20		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		40		0.010	40		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ $\}$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ $\}$ $|I_{OL}| < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ $\}$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ $\}$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$ $\}$ $|I_{OH}| < 1\ \mu A$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$ $\}$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6.75	4.0		4.0	V

DC Electrical Characteristics CD4512BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Units
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.78		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.0		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.2		−0.16			−0.12		mA
		$V_{DD} = 10V$, $V_O = 9.5$	−0.5		−0.4			−0.3		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.4		−1.2			−1.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	TRI-STATE Output Current	$V_{DD} = 15V$, $V_O = 0V$		±1.0		$\pm 10^{-5}$	±1.0		±7.5	μA
		$V_{DD} = 15V$, $V_O = 15V$								

AC Electrical Characteristics* $T_A = 25°C$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

Symbol	Parameter	Conditions	CD4512BM Min	CD4512BM Typ	CD4512BM Max	CD4512BC Min	CD4512BC Typ	CD4512BC Max	Units
t_{PHL}	Propagation Delay High-to-Low Level	$V_{DD} = 5V$		225	500		225	750	ns
		$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	ns
t_{PLH}	Propagation Delay Low-to-High Level	$V_{DD} = 5V$		225	500		225	750	ns
		$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		70	200		70	200	ns
		$V_{DD} = 10V$		35	100		35	100	ns
		$V_{DD} = 15V$		25	80		25	80	ns
t_{PHZ}, t_{PLZ}	Propagation Delay into TRI-STATE from Logic Level	$V_{DD} = 5V$		50	125		50	125	ns
		$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	ns
t_{PZH}, t_{PZL}	Propagation Delay to Logic Level from TRI-STATE	$V_{DD} = 5V$		50	125		50	125	ns
		$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	ns
C_{IN}	Input Capacitance	(Note 4)		7.5	15		7.5	15	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		7.5	15		7.5	15	pF
C_{PD}	Power Dissipation Capacity	(Note 5)		150			150		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: ''Absolute Maximum Ratings'' are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of ''Recommended Operating Conditions'' and ''Electrical Characteristics'' provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

**Note 4:** Capacitance guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note, AN-90.

Logic Diagram
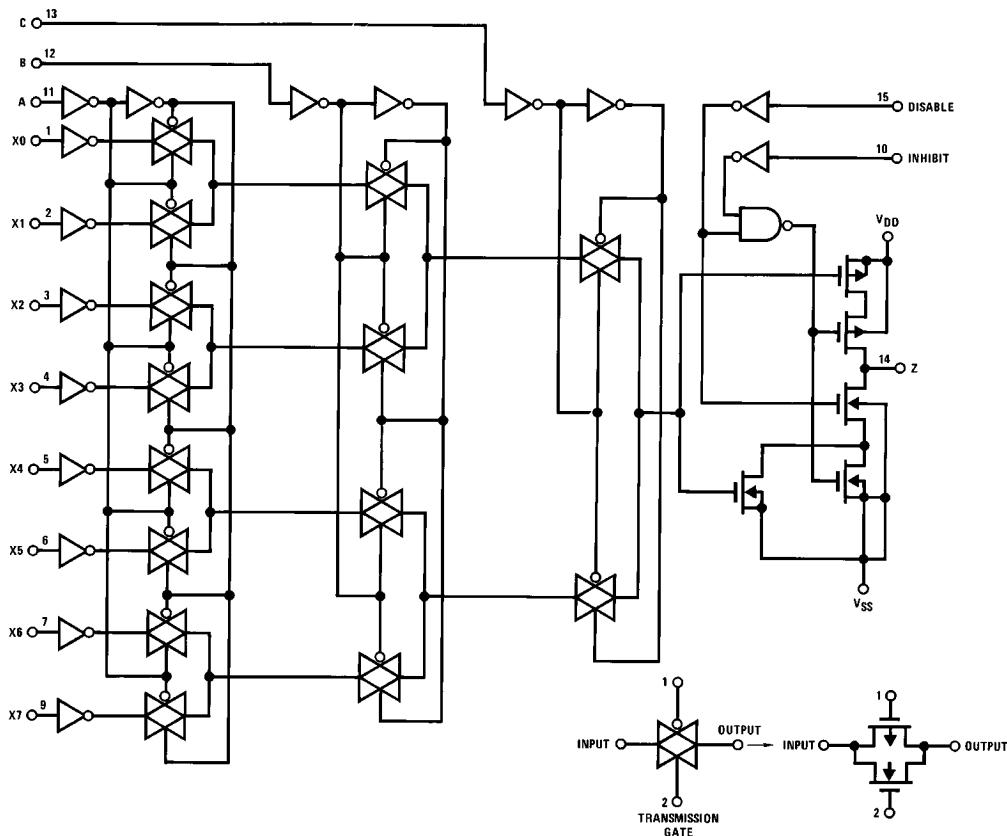
TL/F/5993-2

Typical Application
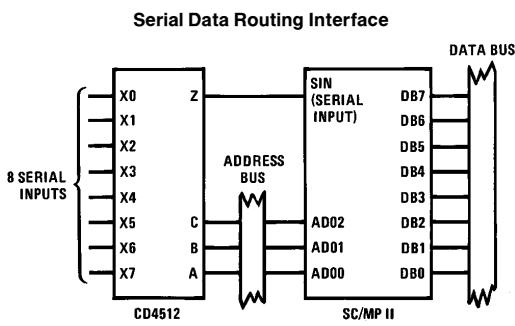
Serial Data Routing Interface

TL/F/5993-3

4

AC Test Circuit and Switching Time Waveforms
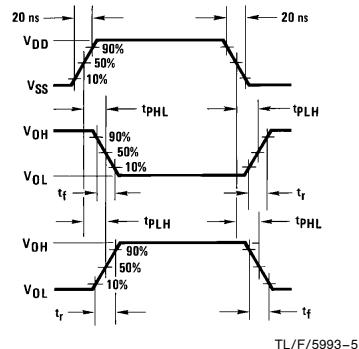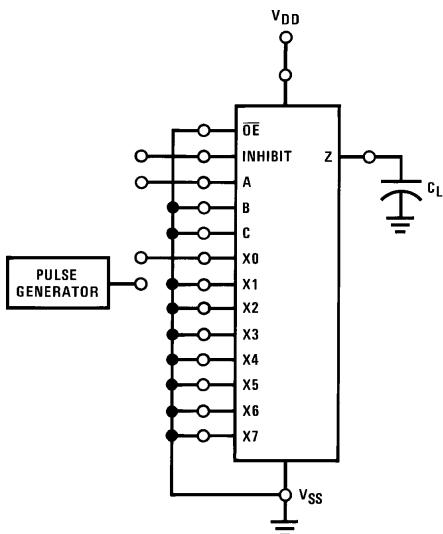
TL/F/5993–4

TL/F/5993–5

Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

Test	Inhibit	A	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

TRI-STATE AC Test Circuit and Switching Time Waveforms
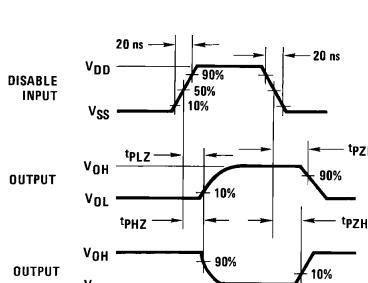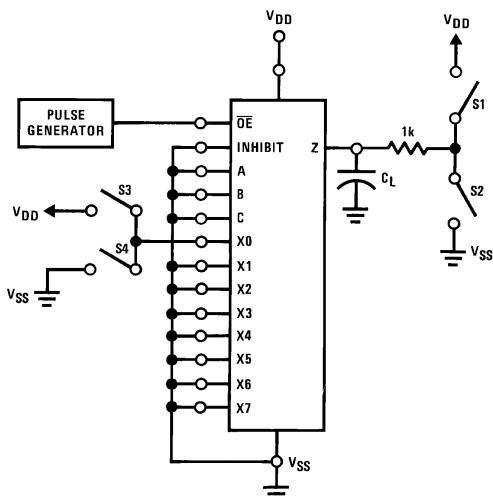
TL/F/5993–6

TL/F/5993–7

Switch Positions for TRI-STATE Test

Test	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

5

Physical Dimensions inches (millimeters)

0.785
[19.94] MAX

16   9

0.220–0.310
[5.59–7.87]

R 0.025
[0.64]

1   8

R 0.005–0.020 TYP
[0.13–0.51]

0.037 ± 0.005 TYP
[0.94 ± 0.13]

0.005
[0.13]
MIN TYP

0.055 ± 0.005 TYP
[1.40 ± 0.13]

0.290–0.320
[7.37–8.13]

GLASS SEALANT

0.200
[5.08]
MAX TYP

0.020–0.060 TYP
[0.51–1.52]

0.180 MAX
[4.57]

0.010 ± 0.002 TYP
[0.25 ± 0.05]

0.150 MIN TYP
[3.81]

0.125–0.200 TYP
[3.18–5.08]

90° ± 4° TYP

95° ± 5° TYP

0.080 MAX
[2.03]
BOTH ENDS

0.018 ± 0.003 TYP
[0.46 ± 0.08]

0.310–0.410
[7.87–10.41]

J16A (REV L)

0.100 ± 0.010 TYP
[2.54 ± 0.25]

Ceramic Dual-In-Line Package (J)
Order Number CD4512BMJ or CD4512BCJ
NS Package Number J16A

0.740 – 0.780
(18.80 – 19.81)

0.090
(2.286)

16 15 14 13 12 11 10 9

0.250 ± 0.010
(6.350 ± 0.254)

INDEX
AREA

16 15

PIN NO. 1
IDENT

1 2 3 4 5 6 7 8

OPTION 01

PIN NO. 1
IDENT

1 2

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060 TYP
(1.524)

4° TYP
OPTIONAL

0.300 – 0.320
(7.620 – 8.128)

0.145 – 0.200
(3.683 – 5.080)

0.020 MIN
(0.508)

0.125 – 0.150
(3.175 – 3.810)

90° ± 4° TYP

0.030 ± 0.015
(0.762 ± 0.381)

95° ± 5°

0.008 – 0.016 TYP
(0.203 – 0.406)

0.280
(7.112)
MIN

0.014 – 0.023 TYP
(0.356 – 0.584)

0.100 ± 0.010
(2.540 ± 0.254)
TYP

0.050 ± 0.010 TYP
(1.270 ± 0.254)

(0.325 +0.040 −0.015)
(8.255 +1.016 −0.381)

N16E (REV F)

Molded Dual-In-Line Package (N)
Order Number CD4512BMN or CD4512BCN
NS Package Number N16E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.