CMOS Dual 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4517B dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the CD4517B. Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.
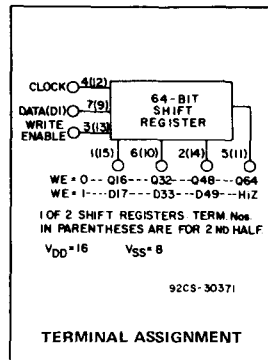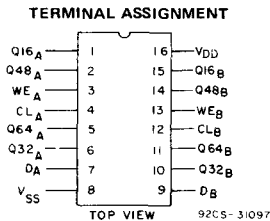
The CD4517B is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Low quiescent current — 10 nA/pkg (typ.) at $V_{DD} = 5$ V
- Clock frequency 12 MHz (typ.) at $V_{DD} = 10$ V
- Schmitt trigger clock inputs allow operation with very slow clock rise and fall times
- Capable of driving two low-power TTL loads, one low-power Schottky TTL load, or two HTL loads
- Three-state outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Time-delay circuits
- Scratch-pad memories
- General-purpose serial shift-register applications

TERMINAL ASSIGNMENT

Q16$_A$	1	16	V$_{DD}$
Q48$_A$	2	15	Q16$_B$
WE$_A$	3	14	Q48$_B$
CL$_A$	4	13	WE$_B$
Q64$_A$	5	12	CL$_B$
Q32$_A$	6	11	Q64$_B$
D$_A$	7	10	Q32$_B$
V$_{SS}$	8	9	D$_B$

TOP VIEW   92CS-31097

CLOCK 4(2)
DATA(DI) 7(9)
WRITE ENABLE 3(13)

64-BIT SHIFT REGISTER

1(15) 6(10) 2(14) 5(11)

WE = 0 -- Q16--- Q32--Q48--Q64
WE = I---DI7---D33--D49--HiZ
I OF 2 SHIFT REGISTERS TERM. Nos.
IN PARENTHESES ARE FOR 2 ND HALF
V_{DD} = 16 V_{SS} = 8

92CS-30371

TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
    For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . 500 mW
    For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . Derate Linearly at 12 mW/°C to 200 mW
    For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . 500 mW
    For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
    FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
    PACKAGE TYPES D, F, K, H . . . . −55 to +125°C
    PACKAGE TYPE E . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
    At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

TRUTH TABLE

Clock	Write Enable	Data	Stage 16 Tap	Stage 32 Tap	Stage 48 Tap	Stage 64 Tap
0	0	X	Q16	Q32	Q48	Q64
0	1	X	Z	Z	Z	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z
⟋	0	DI In	Q16	Q32	Q48	Q64
⟋	1	DI In	D17 In	D33 In	D49 In	Z
⟋	0	X	Q16	Q32	Q48	Q64
⟋	1	X	Z	Z	Z	Z

X = Don't Care   Z = High Impedance

CD4517B Types

92CM-31098RI

Fig. 1—CD4517B functional block diagram (one half).

▲ PROTECTED BY COS/MOS PROTECTION NETWORK

* PROTECTED BY COS/MOS PROTECTION NETWORK
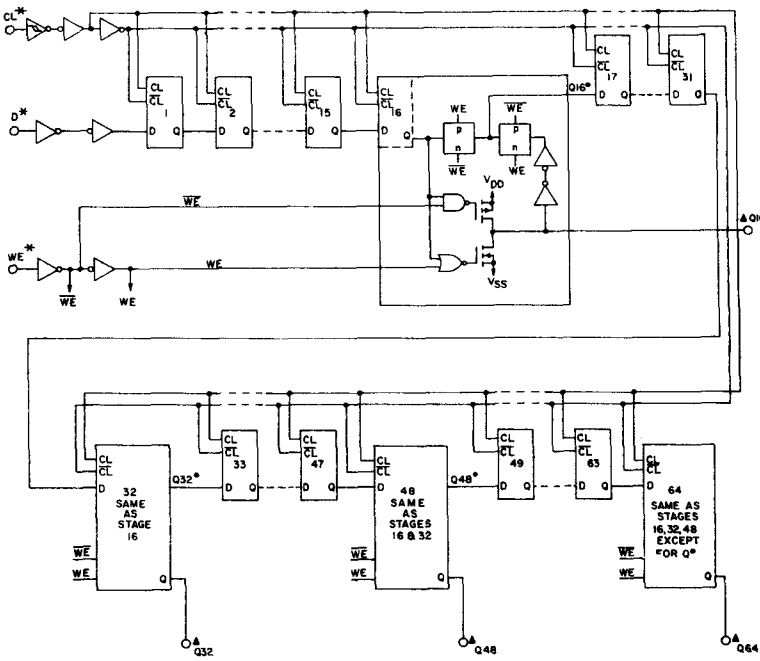
92CL-32765
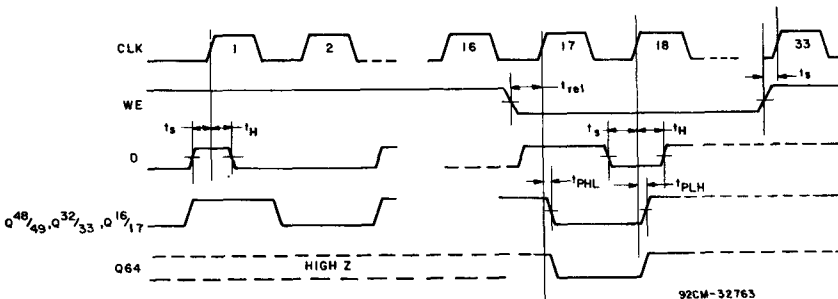
Fig. 2—CD4517B logic block diagram (one half).

92CM-32763

Fig. 3—Dynamic test waveforms.

STATIC ELECTRICAL CHARACTERISTICS

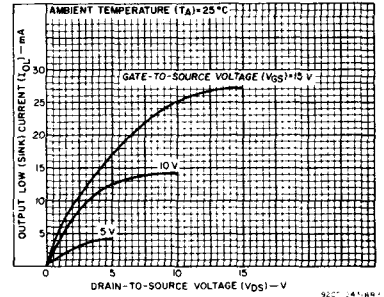| CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$\pm10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	$\pm10^{-4}$	±0.4	μA

Fig. 4—Typical n-channel output low (sink) current characteristics.
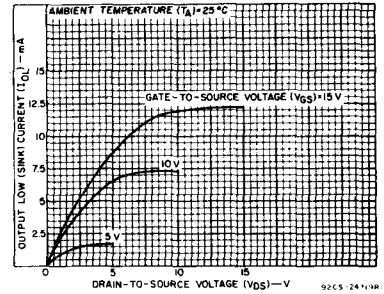

Fig. 5—Minimum n-channel output low (sink) current characteristics.
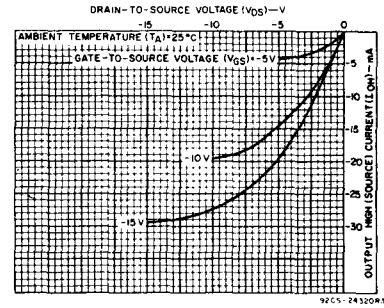

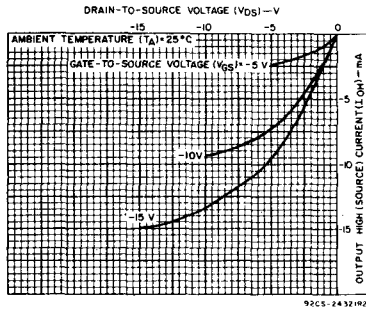Fig. 6—Typical p-channel output high (source) current characteristics.

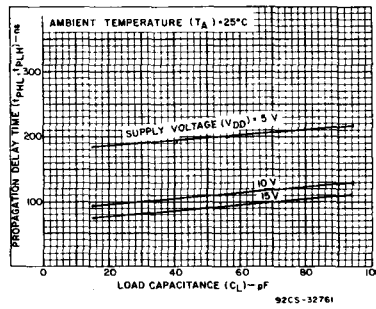Fig. 7—Minimum p-channel output high (source) current characteristics.

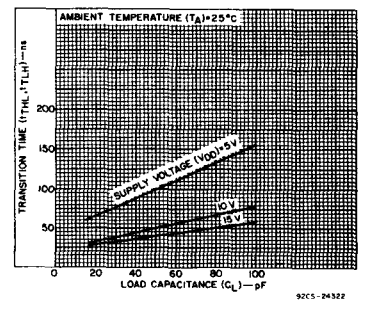Fig. 8—Typical propagation delay time as a function of load capacitance.

Fig. 9—Typical transition time a a function of load capacitance.

CD4517B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$; Input t_r, $t_f = 20\,ns$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time: CL to Bit 16 Tap t_{PHL}, t_{PLH}		5	—	200	400	
		10	—	110	220	ns
		15	—	90	180	
3-State Output, WE to Bit 16 Tap t_{PHZ}, t_{PLZ}; t_{PZH}, t_{PZL} (See Note)		5	—	75	150	
		10	—	40	80	ns
		15	—	30	60	
Output Transition Time t_{THL}, t_{TLH}		5	—	100	200	
		10	—	50	100	ns
		15	—	40	80	
Write Enable-to-Clock Setup Time		5	0	−50	—	
		10	0	−25	—	ns
		15	0	−15	—	
Data-to-Clock Setup Time, t_S		5	20	0	—	
		10	10	0	—	ns
		15	10	0	—	
Minimum Write Enable-to-Clock Release Time		5	—	50	100	
		10	—	25	50	ns
		15	—	20	40	
Minimum Data-to-Clock Hold Time, t_H		5	—	100	200	
		10	—	50	100	ns
		15	—	25	50	
Minimum Clock Pulse Width, t_W		5	—	90	180	
		10	—	40	80	ns
		15	—	25	50	
Maximum Clock Input Frequency, f_{CL}		5	3	6	—	
		10	6	12	—	MHz
		15	8	15	—	
Maximum Clock Input Rise or Fall Time, t_{fCL} t_{rCL}		5 10 15		UNLIMITED		µs
Input Capacitance C_{IN}	Any Input		—	5	7.5	pF

NOTE: Measured at the point of 10% change in output with an output load of 50 pF, R_L = 1 kΩ to V_{DD} for t_{PZL}, t_{PLZ} and R_L = 1 kΩ to V_{SS} for t_{PZH}, t_{PHZ}.
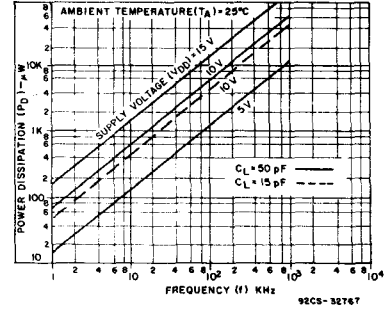

Fig. 10—Typical power dissipation as a function of frequency.
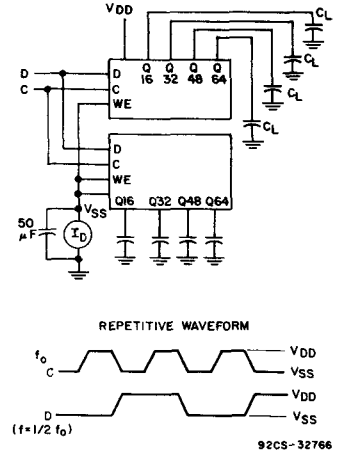

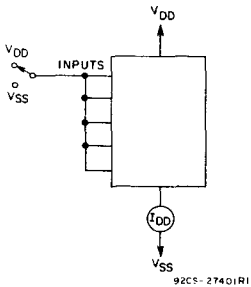Fig. 11—Dynamic power dissipation test circuit and waveforms.
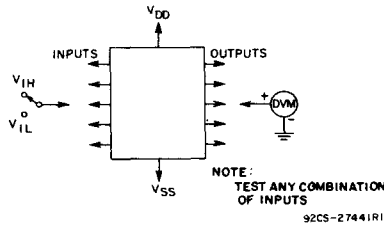

Fig. 12—Quiescent-device-current test circuit.
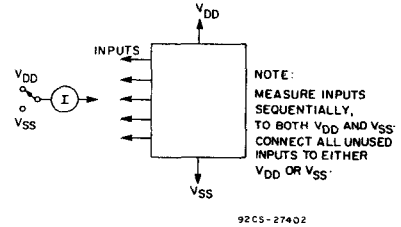

Fig. 13—Input-voltage test circuit.
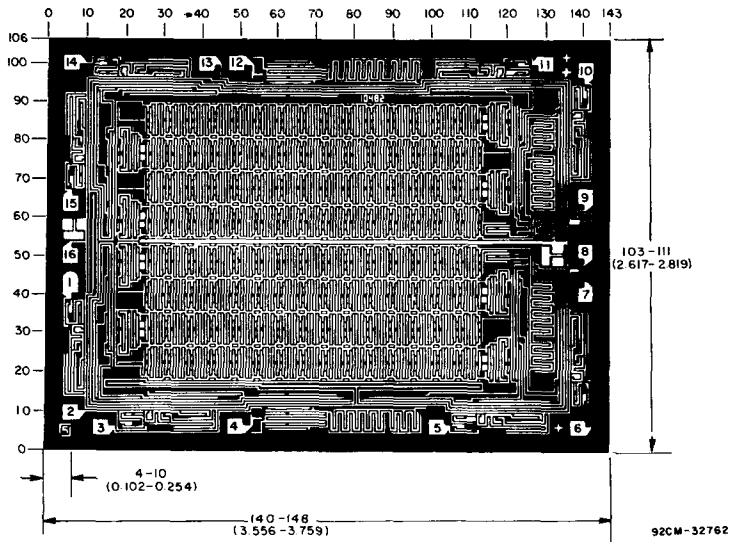

Fig. 14—Input current test circuit.

Dimensions and pad layout for CD4517B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.