CD4538B DualPrecisionMonostable

General Description

The CD4538B is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active low and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

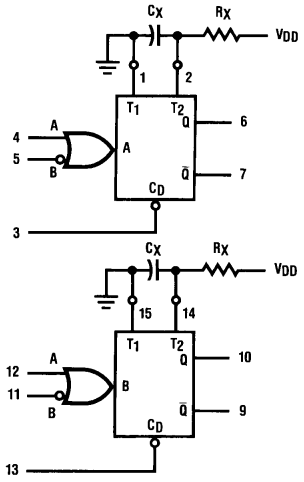
Features

- Wide supply voltage range 5.0V to 15V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power TTL compatibility Fan out of 2 driving 74L or 1 driving 74LS
- New formula: $PW_{OUT} = RC$ (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range 1 μs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current 5 nA (typ.) @ 5 V_{DC}
- Pin compatible to CD4528B

ORDERING INFORMATION

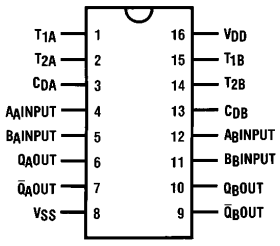
DEVICE	Package Type	MARKING	Packing	Packing Qty
CD4538BE	DIP-16L	CD4538B	TUBE	1000pcs/box
CD4538BM/TR	SOP-16L	CD4538B	REEL	2500pcs/reel

Block and Connection Diagrams



R_X and C_X are External Components
V_{DD} = Pin 16
V_{SS} = Pin 8

Dual-In-Line Package
CD4538BM



Top View

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	5 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4538B	−40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V V_{IH} = V_{DD}, V_{IL} = V_{SS}, All Outputs Open		20 40 80		0.005 0.010 0.015	20 40 80		150 300 600	μA μA μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V $\|I_O\|$ < 1 μA, V_{IH} = V_{DD}, V_{IL} = V_{SS}		0.05 0.05 0.05		0 0 0	0.05 0.05 0.05		0.05 0.05 0.05	V V V
V_{OH}	High Level Output Voltage	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V $\|I_O\|$ < 1 μA, V_{IH} = V_{DD}, V_{IL} = V_{SS}	4.95 9.95 14.95		4.95 9.95 14.95	5 10 15		4.95 9.95 14.95		V V V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1 μA V_{DD} = 5V, V_O = 0.5V or 4.5V V_{DD} = 10V, V_O = 1.0V or 9.0V V_{DD} = 15V, V_O = 1.5V or 13.5V		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V V V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1 μA V_{DD} = 5V, V_O = 0.5V or 4.5V V_{DD} = 10V, V_O = 1.0V or 9.0V V_{DD} = 15V, V_O = 1.5V or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.50 8.25		3.5 7.0 11.0		V V V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V V_{DD} = 10V, V_O = 0.5V V_D = 15V, V_O = 1.5V V_{IH} = V_{DD}, V_{IL} = V_{SS}	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.25 8.8		0.36 0.9 2.4		mA mA mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V V_{DD} = 10V, V_O = 9.5V V_D = 15V, V_O = 13.5V V_{IL} = V_{SS}	−0.52 −1.3 −3.6		−0.44 −1.1 −3.0	−0.88 −2.25 −8.8		−0.36 −0.9 −2.4		mA mA mA
I_{IN}	Input Current, Pin 2 or 14	V_{DD} = 15V, V_{IN} = 0V or 15V		±0.02		$\pm 10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current Other Inputs	V_{DD} = 15V, V_{IN} = 0V or 15V		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for acutal device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, and $t_r = t_f = 20$ ns unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{TLH}, t_{THL}	Output Transition Time	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$			100 50 40	200 100 80	ns ns ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Trigger Operation— A or B to Q or $\overline{Q}$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ Reset Operation— C_D to Q or $\overline{Q}$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$			 300 150 100 250 125 95	 600 300 220 500 250 190	 ns ns ns ns ns ns
t_{WL}, t_{WH}	Minimum Input Pulse Width A, B, or C_D	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$			35 30 25	70 60 50	ns ns ns
t_{RR}	Minimum Retrigger Time	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$			 0 	0 0 0	ns ns ns
C_{IN}	Input Capacitance	Pin 2 or 14 Other Inputs			10 5	 7.5	pF pF
PW_{OUT}	Output Pulse Width (Q or $\overline{Q}$) **(Note:** For Typical Distribution, see *Figure 9*)	$R_X = 100$ kΩ $C_X = 0.002$ μF	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	208 211 216	226 230 235	244 248 254	μs μs μs
		$R_X = 100$ kΩ $C_X = 0.1$ μF	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	8.83 9.02 9.20	9.60 9.80 10.00	10.37 10.59 10.80	ms ms ms
		$R_X = 100$ kΩ $C_X = 10.0$ μF	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$	0.87 0.89 0.91	0.95 0.97 0.99	1.03 1.05 1.07	s s s
Pulse Width Match between Circuits in the Same Package $C_X = 0.1$ μF, $R_X = 100$ kΩ		$R_X = 100$ kΩ $C_X = 0.1$ μF	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		±1 ±1 ±1		% % %
Operating Conditions							
R_X C_X	External Timing Resistance External Timing Capacitance			5.0 0		** No Limit	kΩ pF

*AC parameters are guaranteed by DC correlated testing.

**The maximum usable resistance R_X is a function of the leakage of the Capacitor C_X, leakage of the CD4538B, and leakage due to board layout, surface resistance, etc.

Logic Diagram

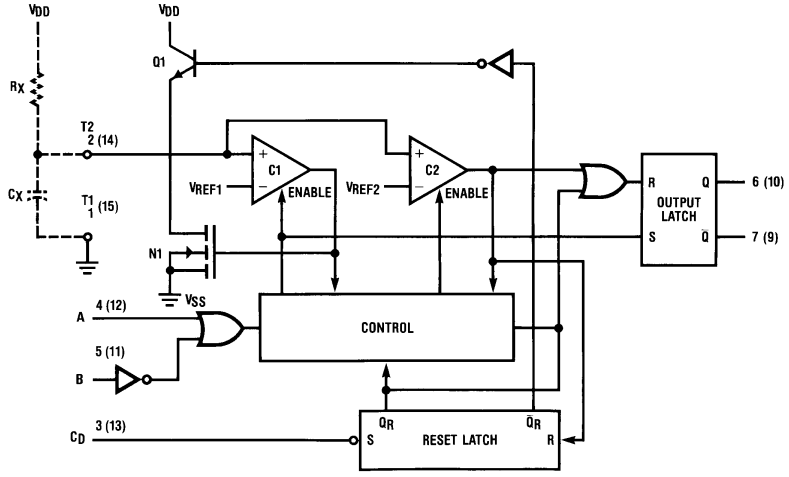


FIGURE 1

Theory of Operation

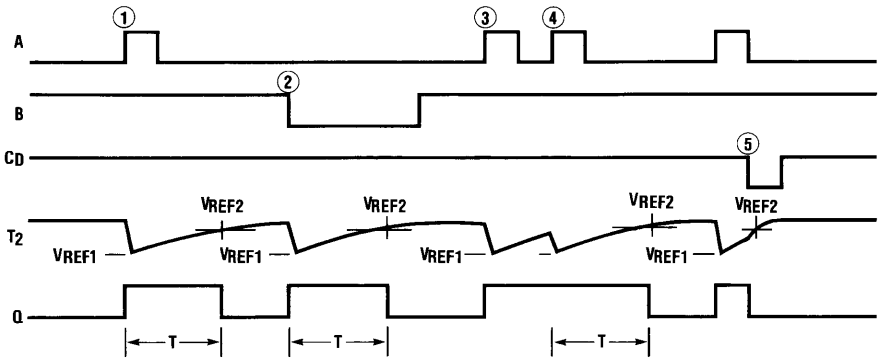


FIGURE 2

Trigger Operation

The block diagram of the CD4538B is shown in *Figure 1*, with circuit operation following.

As shown in *Figures 1* and *2*, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})②.

It should be noted that in the quiescent state C_X is fully charged to V_{DD}, causing the current through resistor R_X to be zero. Both comparators are ‘‘off’’ with the total device current due only to reverse junction leakages. An added feature of the CD4538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

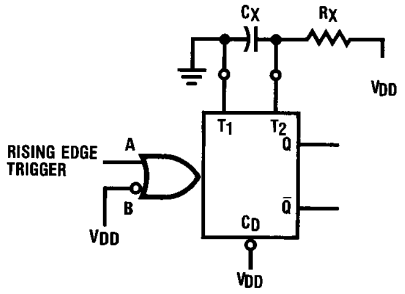
Retrigger Operation

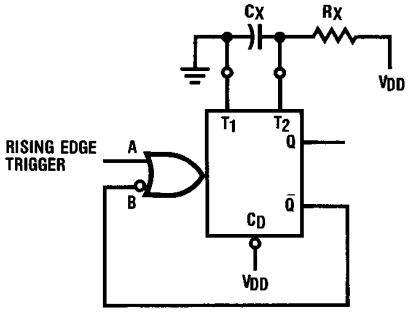
The CD4538B is retriggered if a valid trigger occurs③ followed by another valid trigger④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated④, the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

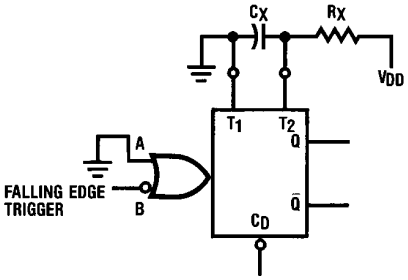
Reset Operation

The CD4538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Applications







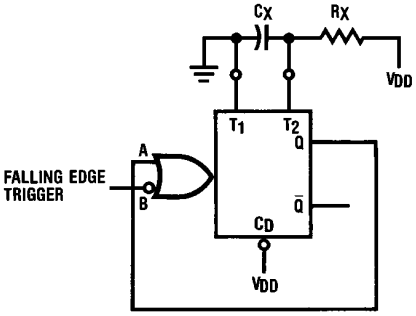


FIGURE 3. Retriggerable Monostables Circuitry

FIGURE 4. Non-Retriggerable Monostables Circuitry

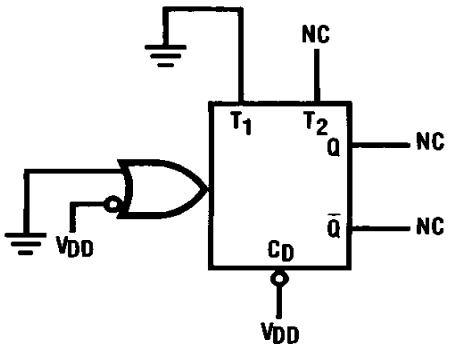


FIGURE 5. Connection of Unused Sections

Typical Applications (Continued)

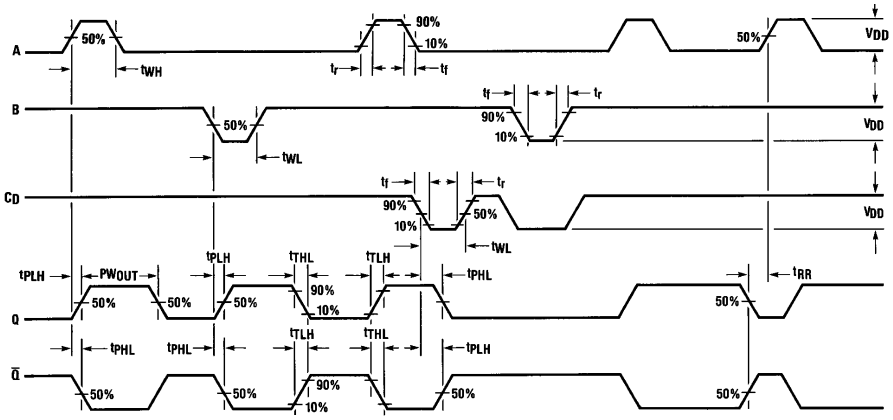
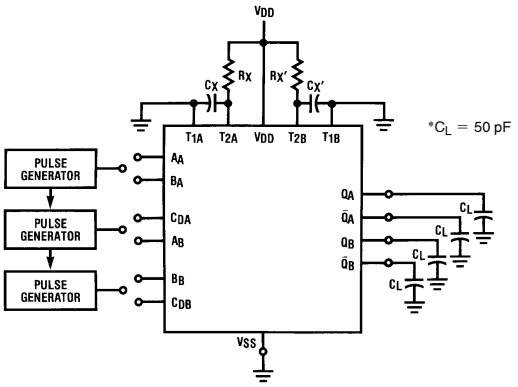
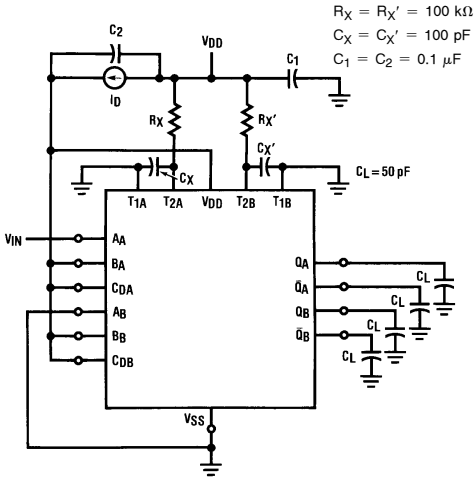


FIGURE 6. Switching Test Waveforms





Input Connections

Characteristics	CD	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic

Note: Switching test waveforms for PG1, PG2, PG3 are shown in *Figure 6*.

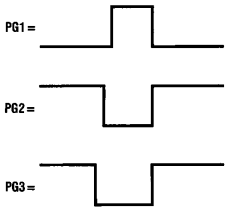
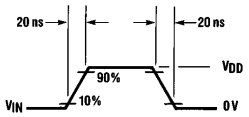


FIGURE 7. Switching Test Circuit



Duty Cycle = 50%

FIGURE 8. Power Dissipation Test Circuit and Waveforms

Typical Applications (Continued)

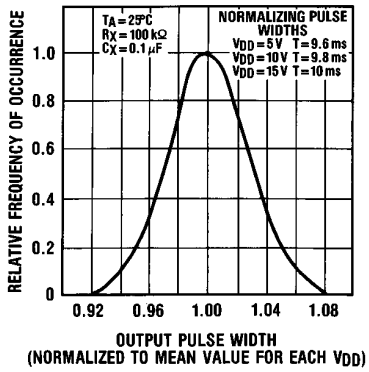


FIGURE 9. Typical Normalized Distribution of Units for Output Pulse Width

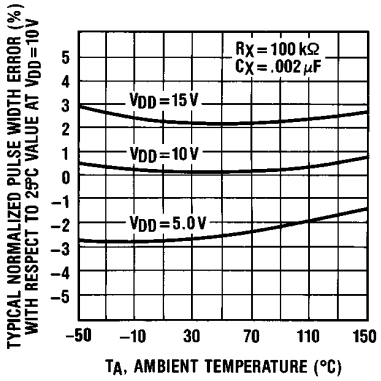


FIGURE 12. Typical Pulse Width Error Versus Temperature

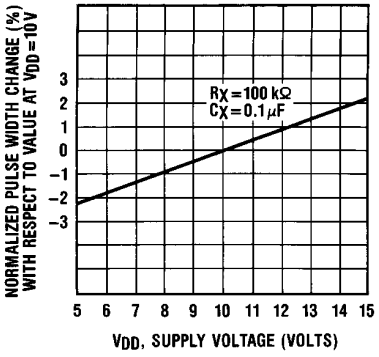


FIGURE 10. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

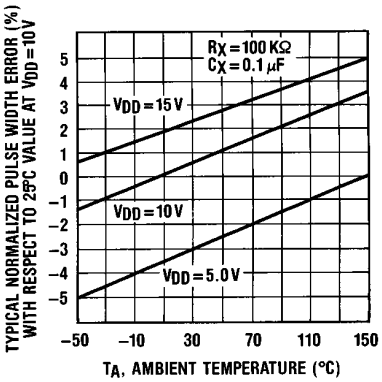


FIGURE 13. Typical Pulse Width Error Versus Temperature

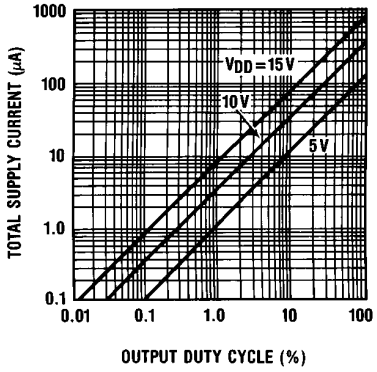


FIGURE 11. Typical Total Supply Current Versus Output Duty Cycle, R_X = 100 kΩ, C_L = 50 pF, C_X = 100 pF, One Monostable Switching Only

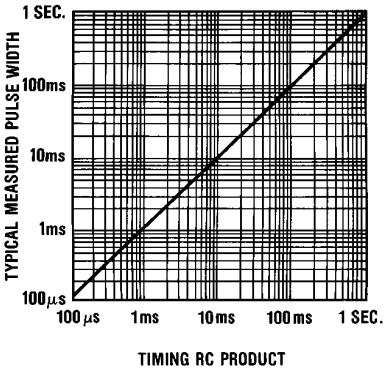
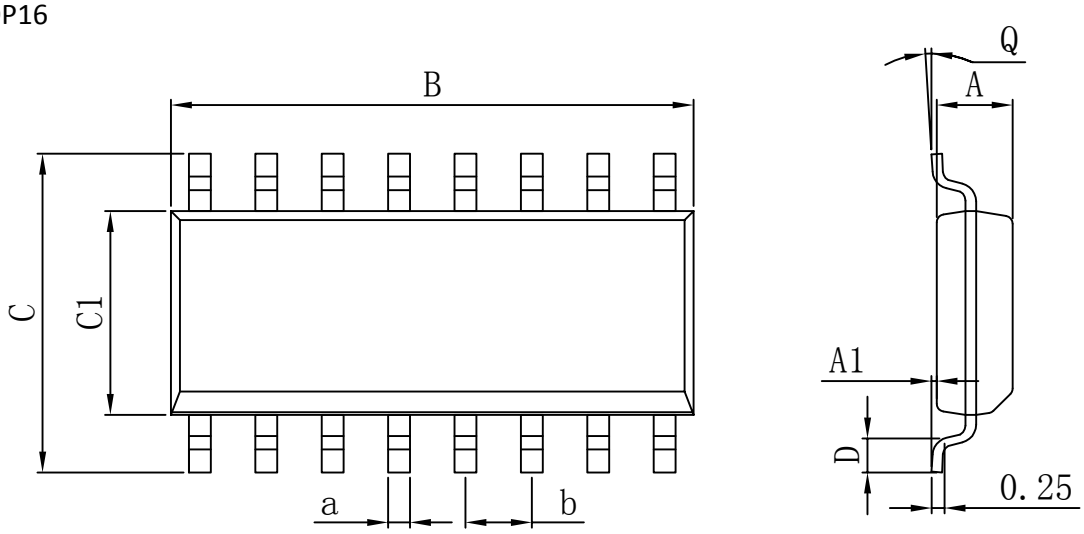


FIGURE 14. Typical Pulse Width Versus Timing RC Product

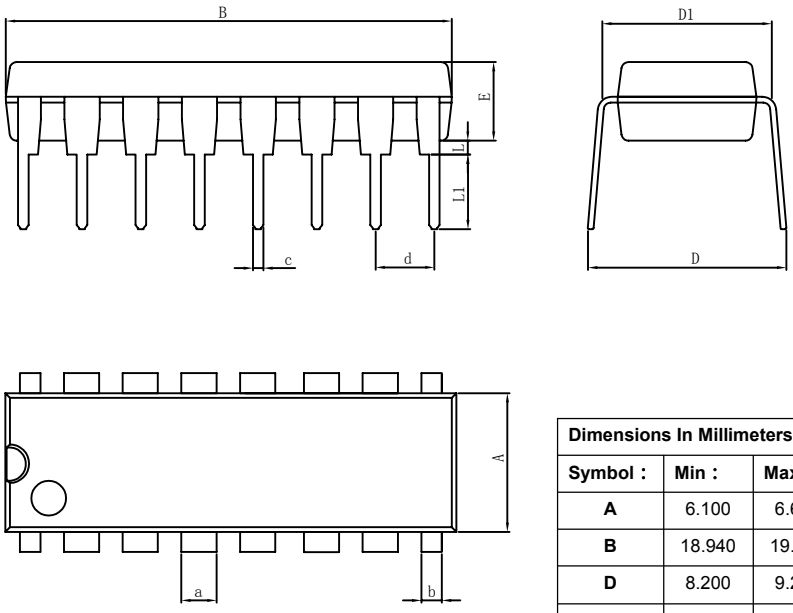
PACKAGE

SOP16



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	1.225	1.570	**D**	0.400	0.950
A1	0.100	0.250	**Q**	0°	8°
B	9.800	10.00	**a**	0.420 TYP	
C	5.800	6.250	**b**	1.270 TYP	
C1	3.800	4.000			

DIP16



Dimensions In Millimeters					
Symbol :	**Min :**	**Max :**	**Symbol :**	**Min :**	**Max :**
A	6.100	6.680	**L**	0.500	0.800
B	18.940	19.560	**a**	1.524 TYP	
D	8.200	9.200	**b**	0.889 TYP	
D1	7.42	7.820	**c**	0.457 TYP	
E	3.100	3.550	**d**	2.540 TYP	
L	0.500	0.800			

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