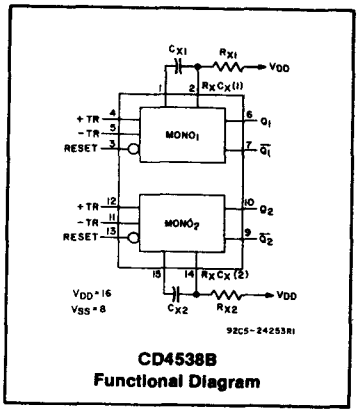
CMOS Dual Precision Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

Features:
- *Retriggerable/resettable capability*
- *Trigger and reset propagation delays independent of R_X, C_X*
- *Triggering from leading or trailing edge*
- *Q and $\overline{Q}$ buffered outputs available*
- *Separate resets*
- *Wide range of output-pulse widths*
- *Schmitt trigger input allows unlimited rise and fall times on +TR and −TR inputs*



CD4538B
Functional Diagram

The RCA-CD4538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused -TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4538B is not used, its inputs must be tied to either V_{DD} or V_{SS}. See Table I.

In normal operation the circuit retriggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used. The time period (T) for this multivibrator can be calculated by: $T=R_XC_X$.

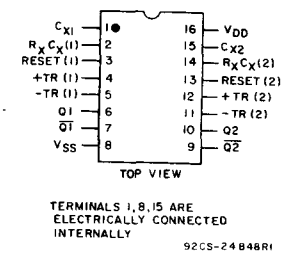
The minimum value of external resistance, R_X, is 4 KΩ. The maximum and minimum values of external capacitance, C_X, are 100 μF and 5000 pF, respectively.

The CD4538B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD4538B is similar to type MC14538 and is pin-for-pin compatible with the CD4098B.

- *100% tested for maximum quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C*
- *Noise margin (full package-temperature range): 1 V at V_{DD}=5 V; 2 V at V_{DD}=10 V; 2.5 V at V_{DD}=15 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Standardized, symmetrical output characteristics*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."*

Applications:
- *Pulse delay and timing*
- *Pulse shaping*



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

92CS-24848R1

Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A=-55 to +100°C (PACKAGE TYPES D,F,K) ..... 500 mW
For T_A=+100 to +125°C (PACKAGE TYPES D,F,K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D,F,K,H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

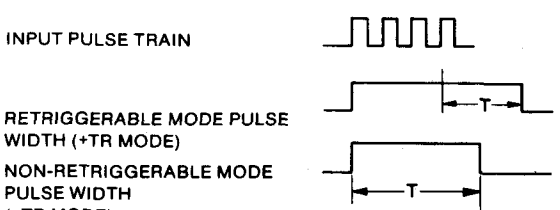
RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS		UNITS
			Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		—	3	18	V
Input Pulse Width +TR, -TR, or RESET	t_{WH}, t_{WL}	5	140	—	ns
		10	80	—	
		15	60	—	

TABLE I
CD4538B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTIION	V_{DD} TO TERM. NO.		V_{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:
1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON—RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.



92CS-32816

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Pkgs. Values at -40, +25, +85 Apply to E Pkgs.							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	+25 Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

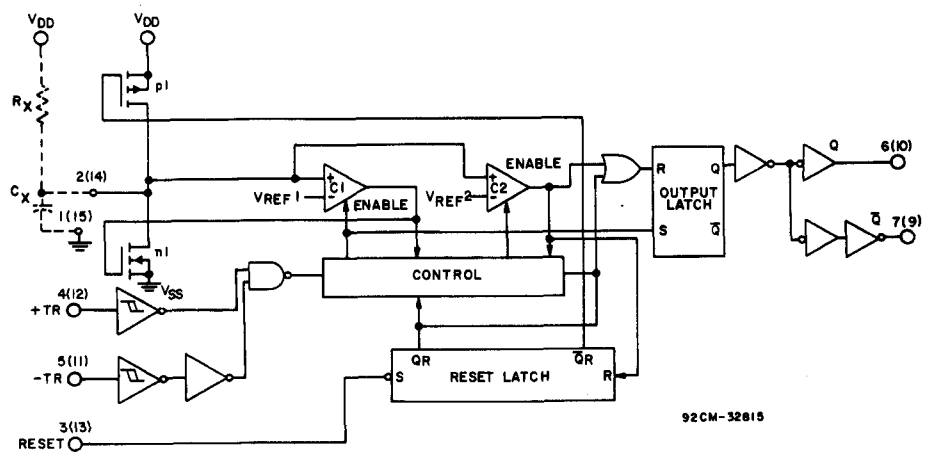


Fig. 1 - Logic diagram (½ of device shown).

DYNAMIC ELECTRICAL CHARACTERISTICS, At T_A=25° C; Input t_r,t_f=20 ns, C_L=50 pF

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Transition Time	t_{TLH}, t_{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time: +TR or -TR to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	5	—	300	600	
		10	—	150	300	
		15	—	100	220	
Reset to Q or $\overline{Q}$		5	—	250	500	
		10	—	125	250	
		15	—	95	190	
Minimum Input Pulse Width: +TR, -TR or Reset	t_{WH}, t_{WL}	5	—	80	140	
		10	—	40	80	
		15	—	30	60	
Output Pulse Width - Q or $\overline{Q}$: C_X=0.005 μF, R_X=10 KΩ*	T	5	57	60.6	64.5	μs
		10	55	58.9	63.0	
		15	55	59.1	63.5	
C_X=0.1 μF, R_X=100 KΩ		5	9.4	9.97	10.5	ms
		10	9.4	9.95	10.6	
		15	9.5	10.00	10.6	
C_X=10 μF, R_X=100 KΩ		5	0.95	1.00	1.06	s
		10	0.95	1.00	1.06	
		15	0.96	1.01	1.07	
Pulse Width Match between circuits in same package: C_X=0.1 μF, R_X=100 KΩ	$\frac{100\ (T_1-T_2)}{T_1}$	5	—	±1	—	%
		10	—	±1	—	
		15	—	±1	—	
Minimum Retrigger Time	t_{rr}	5	0	—	—	ns
		10	0	—	—	
		15	0	—	—	
Input Capacitance	C_{IN}	Any Input	—	5.0	7.5	pF

*Note: Minimum R_X value=4 KΩ, minimum C_X value=5000 pF.

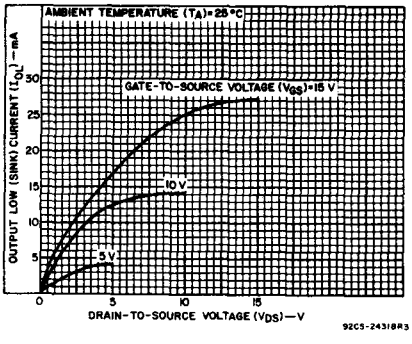


Fig. 2 - Typical output low (sink) current characteristics.

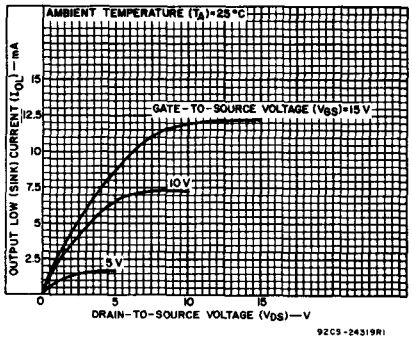


Fig. 3 - Minimum output low (sink) current characteristics.

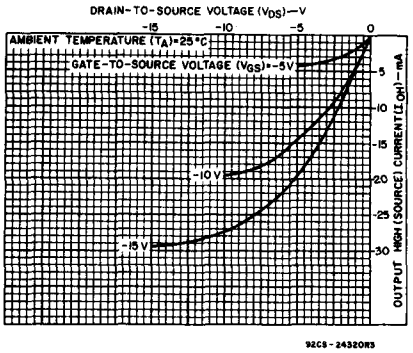


Fig. 4 - Typical output high (source) current characteristics.

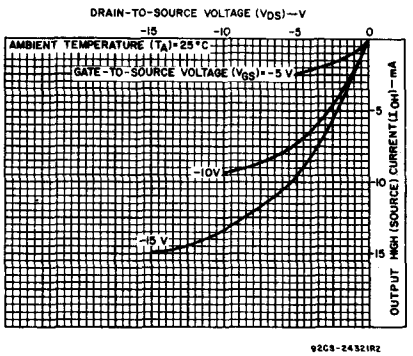


Fig. 5 - Minimum output high (source) current characteristics.

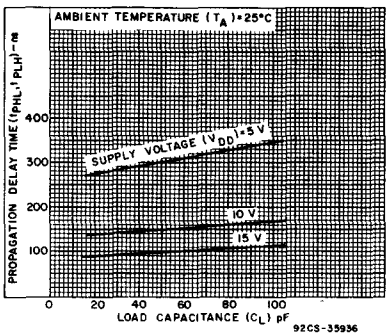


Fig. 6 - Typical propagation delay time as a function of load capacitance (+TR or −TR to Q or $\overline{Q}$).

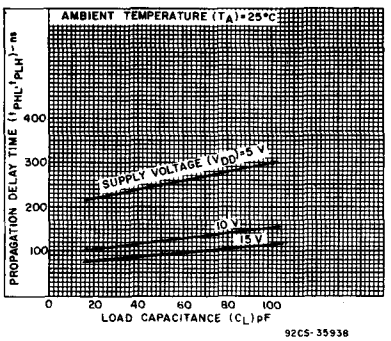


Fig. 7 - Typical propagation delay time as a function of load capacitance (RESET to Q or $\overline{Q}$).

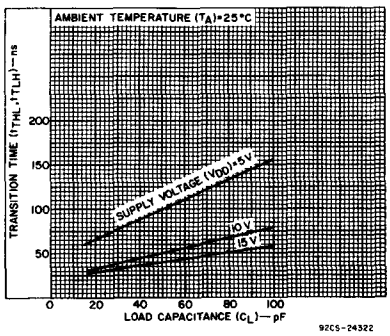


Fig. 8 - Typical transition time as a function of load capacitance.

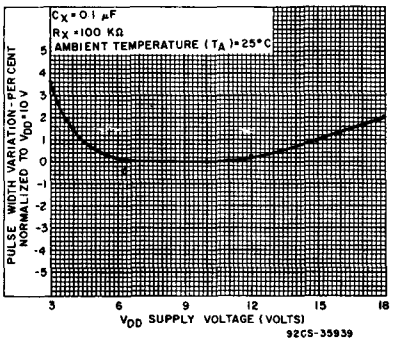


Fig. 9 - Typical pulse-width variation as a function of supply voltage.

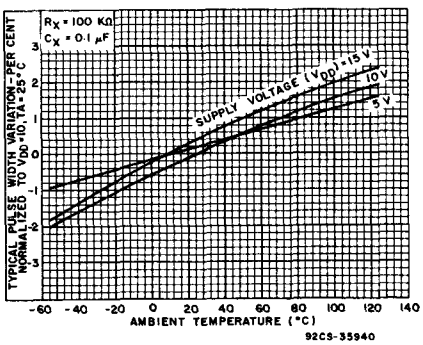


Fig. 10 - Typical pulse-width variation as a function of temperature (R_X=100 KΩ, C_X=0.1 μF).

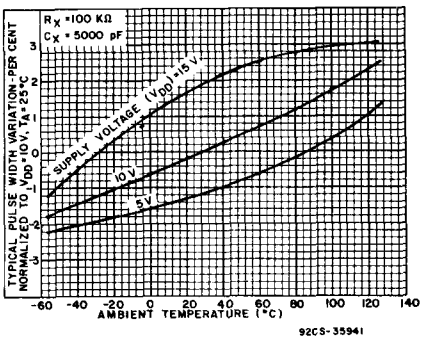


Fig. 11 - Typical pulse-width variation as a function of temperature (R_X=100 KΩ, C_X=5000 pF).

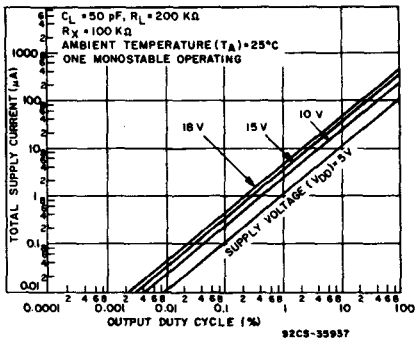


Fig. 12 - Typical total supply current as a function of output duty cycle.

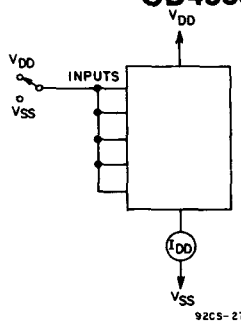
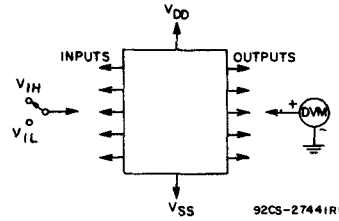


Fig. 13 - Quiescent device current test circuit.



Test any combination of inputs.

Fig. 14 - Input-voltage test circuit.

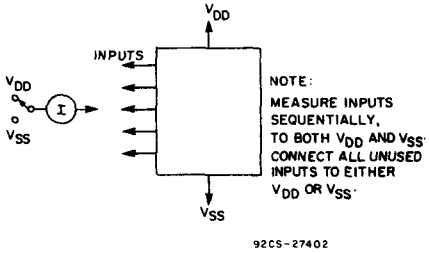


Fig. 15 - Input-leakage-current test circuit.

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_X is ≥ 0.5 microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Fig. 16.

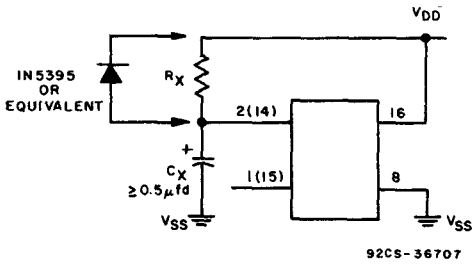


Fig. 16 - Rapid power-down protection circuit.

An alternate protection method is shown in Fig. 17, where a 51-ohm current-limiting resistor is inserted in series with C_X. Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.

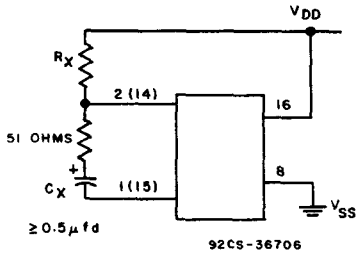
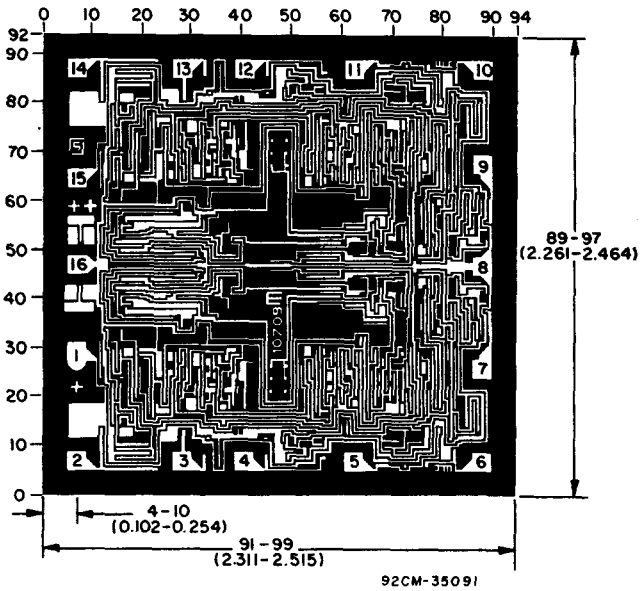


Fig. 17 - Alternate rapid power-down protection circuit.



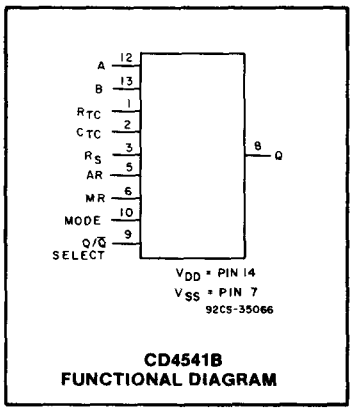
Dimensions and pad layout for CD4538BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimension as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

CMOS Programmable Timer

High-Voltage Types (20-Volt Rating)



CD4541B FUNCTIONAL DIAGRAM

Features:

- *Low symmetrical output resistance, typically 100Ω at V_{DD} = 15 V*
- *Built-in low-power RC oscillator*
- *Oscillator frequency range: DC to 100 kHz*
- *External clock (applied to pin 3) can be used instead of oscillator*
- *Operates as 2^N* frequency divider or as a single-transition timer
- *Q/$\overline{Q}$ select provides output logic level flexibility*
- *AUTO or MASTER RESET disables oscillator during reset to reduce power dissipation*
- *Operates with very slow clock rise and fall times*
- *Capable of driving six low power TTL loads, three low-power Schottky loads, or six HTL loads over the rated temperature range*
- *Symmetrical output characteristics*
- *100% tested for quiescent current at 20 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"*

The RCA-CD4541B programmable timer consists of a 16-stage binary counter, an oscillator that is controlled by external R-C components (2 resistors and a capacitor), an automatic power-on reset circuit, and output control logic. The counter increments on positive-edge clock transitions and can also be reset via the MASTER RESET input.

The output from this timer is the Q or $\overline{Q}$ output from the 8th, 10th, 13th, or 16th counter stage. The desired stage is chosen using time-select inputs A and B (see frequency select table). The output is available in either of two modes selectable via the MODE input, pin 10 (see truth table). When this MODE input is a logic "1", the output will be a continuous square wave having a frequency equal to the oscillator frequency divided by 2^N. With the MODE input set to logic "0" and after a MASTER RESET is initiated, the output (assuming Q output has been selected) changes from a low to a high state after 2^{N-1} counts and remains in that state until another MASTER RESET pulse is applied or the MODE input is set to a logic "1".

Timing is initialized by setting the AUTO RESET input (pin 5) to logic "0" and turning power on. If pin 5 is set to logic "1", the AUTO RESET circuit is disabled and counting will not start until after a positive MASTER RESET pulse is applied and returns to a low level. The AUTO RESET consumes an appreciable amount of power and should not be used if low-power operation is desired.

The RC oscillator, shown in Fig. 2, oscillates with a frequency determined by the R-C network and is calculated using:

$$f = \frac{1}{2.3\ R_{TC}C_{TC}}$$

where f is between 1 kHz and 100 kHz and $R_S \geq 10\ k\Omega$ and $\approx 2R_{TC}$

The CD4541B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

FREQUENCY SELECTION TABLE

A	B	No. of Stages N	Count 2^N
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

PIN	STATE	
	0	1
5	Auto Reset On	Auto Reset Disable
6	Master Reset Off	Master Reset On
9	Output Initially Low After Reset (Q)	Output Initially High After Reset ($\overline{Q}$)
10	Single Transition Mode	Recycle Mode