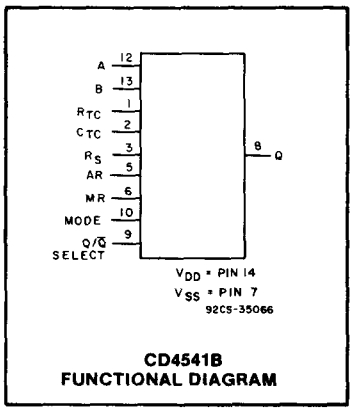
# CMOS Programmable Timer

High-Voltage Types (20-Volt Rating)

**Features:**

- *Low symmetrical output resistance, typically 100Ω at $V_{DD}$ = 15 V*
- *Built-in low-power RC oscillator*
- *Oscillator frequency range: DC to 100 kHz*
- *External clock (applied to pin 3) can be used instead of oscillator*
- *Operates as $2^N$ frequency divider or as a single-transition timer*
- *Q/$\overline{Q}$ select provides output logic level flexibility*
- *AUTO or MASTER RESET disables oscillator during reset to reduce power dissipation*
- *Operates with very slow clock rise and fall times*




**CD4541B FUNCTIONAL DIAGRAM**

- *Capable of driving six low power TTL loads, three low-power Schottky loads, or six HTL loads over the rated temperature range*
- *Symmetrical output characteristics*
- *100% tested for quiescent current at 20 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"*

The RCA-CD4541B programmable timer consists of a 16-stage binary counter, an oscillator that is controlled by external R-C components (2 resistors and a capacitor), an automatic power-on reset circuit, and output control logic. The counter increments on positive-edge clock transitions and can also be reset via the MASTER RESET input.

The output from this timer is the Q or $\overline{Q}$ output from the 8th, 10th, 13th, or 16th counter stage. The desired stage is chosen using time-select inputs A and B (see frequency select table). The output is available in either of two modes selectable via the MODE input, pin 10 (see truth table). When this MODE input is a logic "1", the output will be a continuous square wave having a frequency equal to the oscillator frequency divided by $2^N$. With the MODE input set to logic "0" and after a MASTER RESET is initiated, the output (assuming Q output has been selected) changes from a low to a high state after $2^{N-1}$ counts and remains in that state until another MASTER RESET pulse is applied or the MODE input is set to a logic "1".

Timing is initialized by setting the AUTO RESET input (pin 5) to logic "0" and turning power on. If pin 5 is set to logic "1", the AUTO RESET circuit is disabled and counting will not start until after a positive MASTER RESET pulse is applied and returns to a low level. The AUTO RESET consumes an appreciable amount of power and should not be used if low-power operation is desired.

The RC oscillator, shown in Fig. 2, oscillates with a frequency determined by the R-C network and is calculated using:

$$f = \frac{1}{2.3\,R_{TC}C_{TC}}$$

where f is between 1 kHz and 100 kHz and $R_S \geq 10\ k\Omega$ and $\approx 2R_{TC}$

The CD4541B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

**FREQUENCY SELECTION TABLE**

| A | B | No. of Stages N | Count $2^N$ |
|---|---|---|---|
| 0 | 0 | 13 | 8192 |
| 0 | 1 | 10 | 1024 |
| 1 | 0 | 8 | 256 |
| 1 | 1 | 16 | 65536 |

**TRUTH TABLE**

| PIN | STATE | |
|---|---|---|
| | 0 | 1 |
| 5 | Auto Reset On | Auto Reset Disable |
| 6 | Master Reset Off | Master Reset On |
| 9 | Output Initially Low After Reset (Q) | Output Initially High After Reset ($\overline{Q}$) |
| 10 | Single Transition Mode | Recycle Mode |

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to $V_{DD}$ + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For $T_A$ = −55 to +100°C (PACKAGE TYPES D, F) ..... 500 mW
For $T_A$ = + 100 to +125°C (PACKAGE TYPES D, F) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPES D, F, H ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

**RECOMMENDED OPERATING CONDITIONS**

*For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

| CHARACTERISTIC | $V_{DD}$ (V) | LIMITS | | UNITS |
|---|---|---|---|---|
| | | MIN. | TYP. | |
| Supply-Voltage Range (For $T_A$ = Full Package-Temperature Range) | — | 3 | 18 | V |

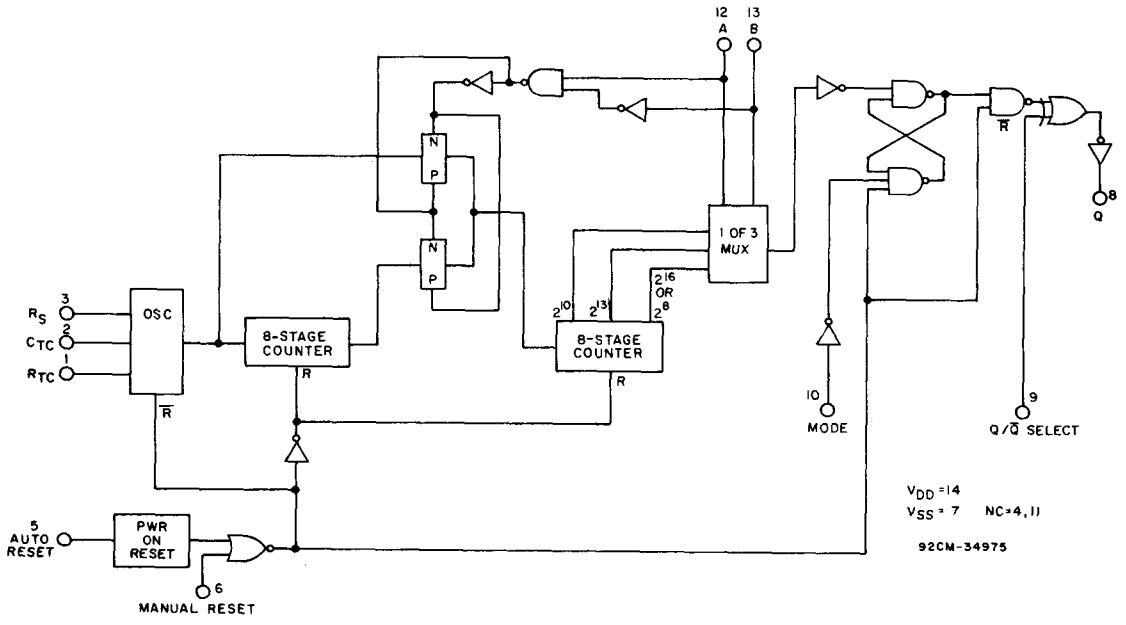
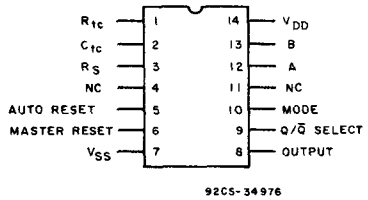



*Fig. 1 — CD4541B functional diagram.*

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, H Packages Values at -40, +25, +85 Apply to E Package | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | -55 | -40 | +85 | +125 | +25 MIN. | +25 TYP. | +25 MAX. | |
| Quiescent Device Current, $I_{DD}$ Max. | — | 0,5 | 5 | 5 | 5 | 150 | 150 | — | 0.04 | 5 | μA |
| | — | 0,10 | 10 | 10 | 10 | 300 | 300 | — | 0.04 | 10 | |
| | — | 0,15 | 15 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| | — | 0,20 | 20 | 100 | 100 | 3000 | 3000 | — | 0.08 | 100 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 1.9 | 1.85 | 1.26 | 1.08 | 1.55 | 3.1 | — | mA |
| | 0.5 | 0,10 | 10 | 5 | 4.8 | 3.3 | 2.8 | 4 | 8 | — | |
| | 1.5 | 0,15 | 15 | 12.6 | 12 | 8.4 | 7.2 | 10 | 20 | — | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | -1.9 | -1.85 | -1.26 | -1.08 | -1.55 | -3.1 | — | |
| | 2.5 | 0,5 | 5 | -6.2 | -6 | -4.1 | -3 | -5 | -10 | — | |
| | 9.5 | 0,10 | 10 | -5 | -4.8 | -3.3 | -2.8 | -4 | -8 | — | |
| | 13.5 | 0,15 | 15 | -12.6 | -12 | -8.4 | -7.2 | -10 | -20 | — | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | — | 0,5 | 5 | — | 0.05 | | | — | 0 | 0.05 | V |
| | — | 0,10 | 10 | — | 0.05 | | | — | 0 | 0.05 | |
| | — | 0,15 | 15 | — | 0.05 | | | — | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | — | 0,5 | 5 | — | 4.95 | | | 4.95 | 5 | — | |
| | — | 0,10 | 10 | — | 9.95 | | | 9.95 | 10 | — | |
| | — | 0,15 | 15 | — | 14.95 | | | 14.95 | 15 | — | |
| Input Low Voltage $V_{IL}$ Max. | 0.5, 4.5 | — | 5 | — | 1.5 | | | — | — | 1.5 | V |
| | 1,9 | — | 10 | — | 3 | | | — | — | 3 | |
| | 1.5,13.5 | — | 15 | — | 4 | | | — | — | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5,4.5 | — | 5 | — | 3.5 | | | 3.5 | — | — | |
| | 1,9 | — | 10 | — | 7 | | | 7 | — | — | |
| | 1.5,13.5 | — | 15 | — | 11 | | | 11 | — | — | |
| Input Current $I_{IN}$ Max. | — | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | $\pm 10^{-5}$ | ±0.1 | μA |




**TERMINAL ASSIGNMENT**

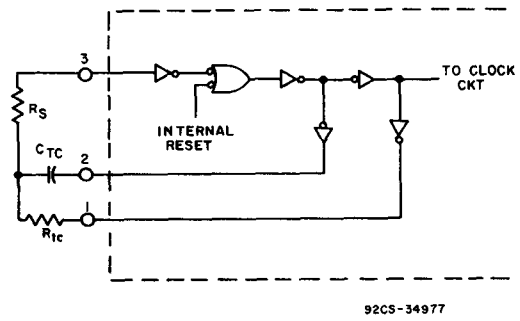



*Fig. 2 — RC oscillator circuit.*

**DYNAMIC ELECTRICAL CHARACTERISTICS,** *at $T_A$ = 25° C, Input $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200 kΩ*

| CHARACTERISTIC | | $V_{DD}$ (V) | LIMITS MIN. | LIMITS TYP. | LIMITS MAX. | UNITS |
|---|---|---|---|---|---|---|
| Propagation Delay Times: Clock to Q | ($2^8$) $t_{PHL}$, $t_{PLH}$ | 5 | — | 3.5 | 10.5 | μs |
| | | 10 | — | 1.25 | 3.8 | |
| | | 15 | — | 0.9 | 2.9 | |
| | ($2^{16}$) $t_{PHL}$, $t_{PLH}$, | 5 | — | 6 | 18 | μs |
| | | 10 | — | 3.5 | 10 | |
| | | 15 | — | 2.5 | 7.5 | |
| Transition Time, | $t_{THL}$ | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| | $t_{TLH}$ | 5 | — | 180 | 360 | ns |
| | | 10 | — | 90 | 180 | |
| | | 15 | — | 65 | 130 | |
| MASTER RESET, CLOCK Pulse Width | | 5 | 900 | 300 | — | ns |
| | | 10 | 300 | 100 | — | |
| | | 15 | 225 | 85 | — | |
| Maximum Clock Pulse Input Frequency, | $f_{CL}$ | 5 | — | 1.5 | — | MHz |
| | | 10 | — | 4 | — | |
| | | 15 | — | 6 | — | |
| Maximum Clock Pulse Input Rise or Fall Time, | $t_r$, $t_f$ | 5,10,15 | Unlimited | | | μs |

## DIGITAL TIMER APPLICATION

A positive pulse on MASTER RESET resets the counters and latch. The output goes high and remains high until the number of pulses, selected by A and B, are counted. This circuit is retriggerable and is as accurate as the input frequency. If additional accuracy is desired, an external clock can be used on pin 3. A set-up time equal to the width of the one-shot output is required immediately following initial power up, during which time the output will be high.

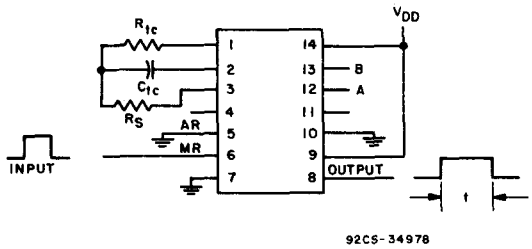
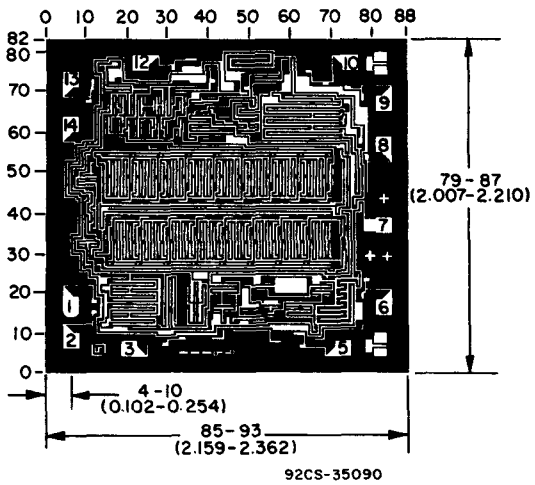



*Fig. 3 - Digital timer application circuit.*




*Dimensions and pad layout for CD4541B.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

*The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.*