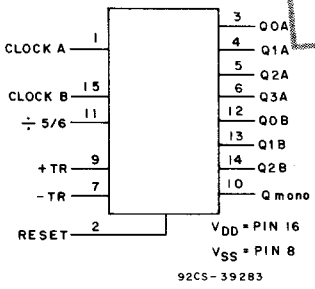
NOT RECOMMENDED FOR NEW DESIGNS

CD4566B Types

CMOS Industrial Time-Base Generator

High-Voltage Types (20-Volt Rating)



FUNCTIONAL DIAGRAM

Features:

- *Falling-edge-triggered counters*
- *Schmitt-trigger clock inputs*
- *Rising or falling-edge-triggered monostable multivibrator*
- *Standardized symmetrical output characteristics*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C*
- *5 V, 10 V, and 15 V parametric ratings*
- *100% tested for quiescent current at 20 V*
- *Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for description of "B" Series CMOS devices"*

■ CD4566B industrial time-base generator consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter which allows stable time generation from a 50 Hz or 60 Hz signal. A LOW on the divide-by-5/6 control selects the divide-by-6 counter a HIGH selects the divide-by-5. A HIGH on the RESET clears the outputs of the counters. Counter outputs are presented in BCD format.

A monostable multivibrator is included which can be used to generate a reset or clock pulse. The monostable multivibrator is triggered either on the rising-edge of the +TR input or on the falling-edge of the -TR input. A LOW on the +TR or a HIGH on the -TR inhibits the output of the monostable multivibrator. An unused +TR input should be tied HIGH; an unused -TR input should be tied LOW.

The CD4566B device is supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), and in chip form (H suffix).

MONOSTABLE MULTIVIBRATOR TRUTH TABLE

INPUTS		OUTPUT
+TR	-TR	Qmono
↑	0	↑
↑	1	0
↓	0	0
↓	1	0
0	↑	0
1	↑	0
0	↓	0
1	↓	↑

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

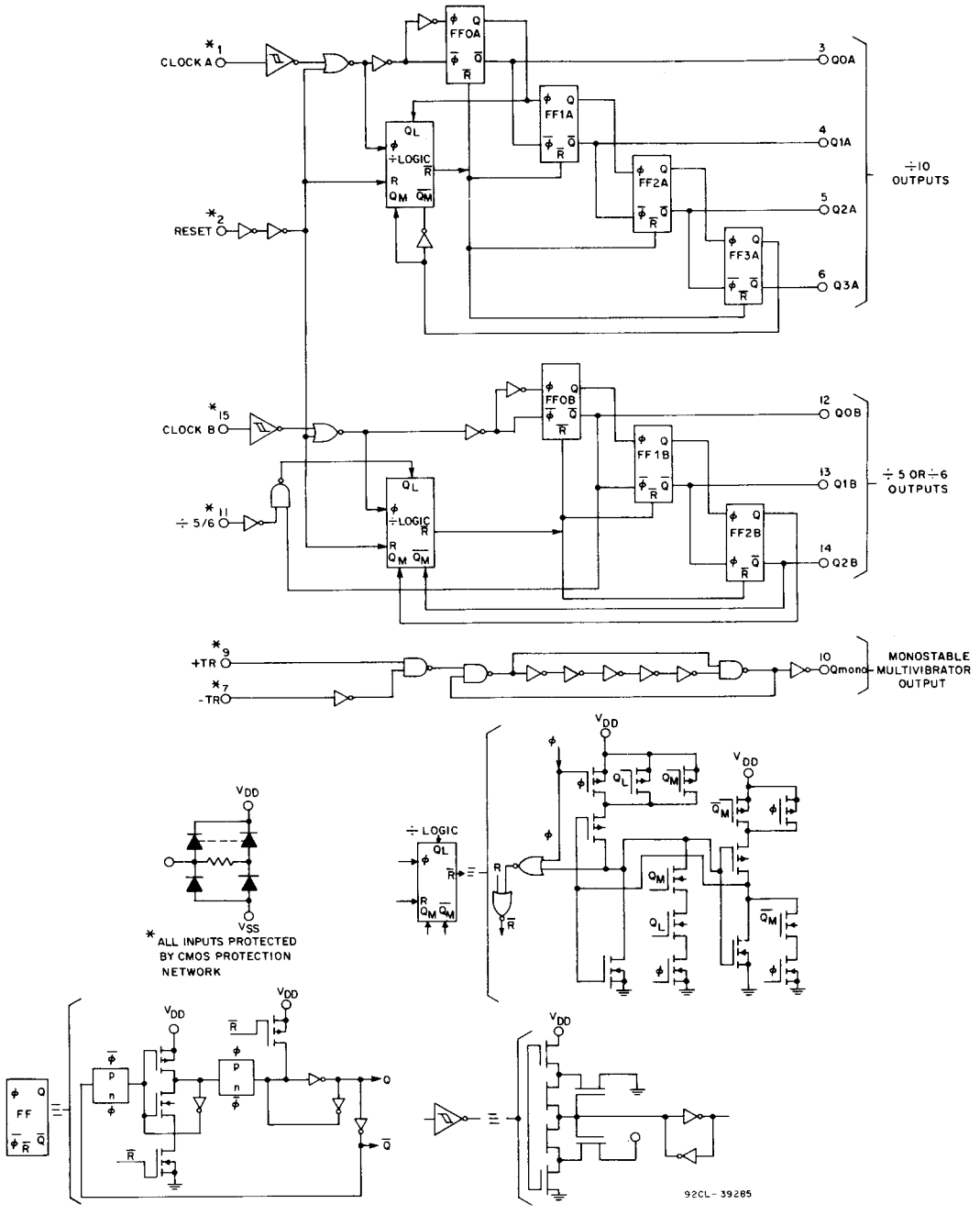


Fig. 1 - Logic diagram for CD4566B.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	MIN.	TYP.	MAX.	
Quiescent Device Current, Max. I_{DD}	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0, 10	10	10	10	300	300	—	0.04	10	
	—	0, 15	15	20	20	600	600	—	0.04	20	
	—	0, 20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, Min. I_{OL}	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, Min. I_{OH}	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage Low-Level, Max. V_{OL}	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage High-Level, Min. V_{OH}	—	0, 5	5	4.95				4.95	5	—	
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage, Max. V_{IL}	0.5,4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, Min. V_{IH}	0.5,4.5	—	5	3.5				3.5	—	—	
	1, 9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, Max. I_{IN}	—	0, 18	18	±0.1	±0.1	±1	±1	—	$\pm 10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS		UNITS
			MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		—	3	18	V
Clock Pulse Width	$t_{w(CL)}$	5	300	—	ns
		10	130	—	
		15	80	—	
Reset Pulse Width	$t_{w(R)}$	5	600	—	ns
		10	300	—	
		15	200	—	
Monostable Multivibrator Pulse Width	$t_{w(mono)}$	5	800	—	ns
		10	300	—	
		15	200	—	

DYNAMIC ELECTRICAL CHARACTERISTICS, at T_A = 25° C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Propagation Delay Time	t_{PHL}	5	—	650	1300	
Clock to Q3A	t_{PLH}	10	—	250	500	ns
		15	—	170	340	
Reset to Q3A		5	—	400	800	
		10	—	170	340	ns
		15	—	120	240	
Minimum Clock Pulse Width	$t_{w(CL)}$	5	—	150	300	
		10	—	65	130	ns
		15	—	40	80	
Minimum Reset Pulse Width	$t_{w(R)}$	5	—	300	600	
		10	—	150	300	ns
		15	—	100	200	
Minimum Monostable Multivibrator Pulse Width	$t_{w(monol}$	5	—	1600	800	
		10	—	600	300	ns
		15	—	400	200	
Transition Time	t_{THL}	5	—	100	200	
	t_{TLH}	10	—	50	100	ns
		15	—	40	80	
Input Capacitance	C_{IN}	Any Input	—	5	7.5	pF

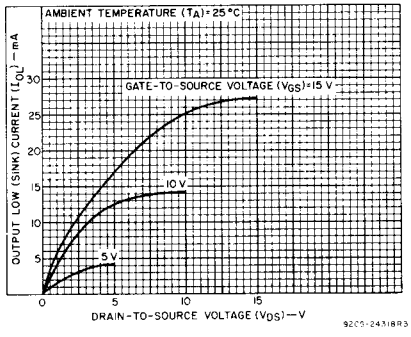


Fig. 2 - Typical output low (sink) current characteristics.

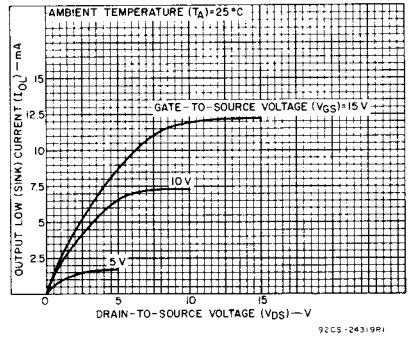


Fig. 3 - Minimum output low (sink) current characteristics.

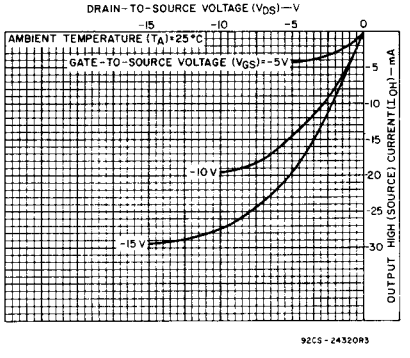


Fig. 4 - Typical output high (source) current characteristics.

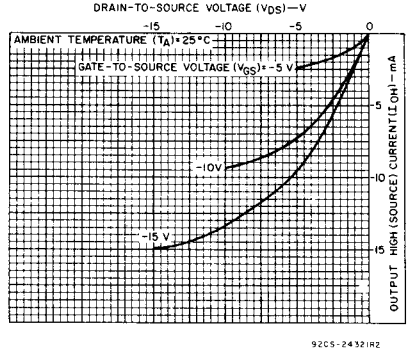


Fig. 5 - Minimum output high (source) current characteristics.

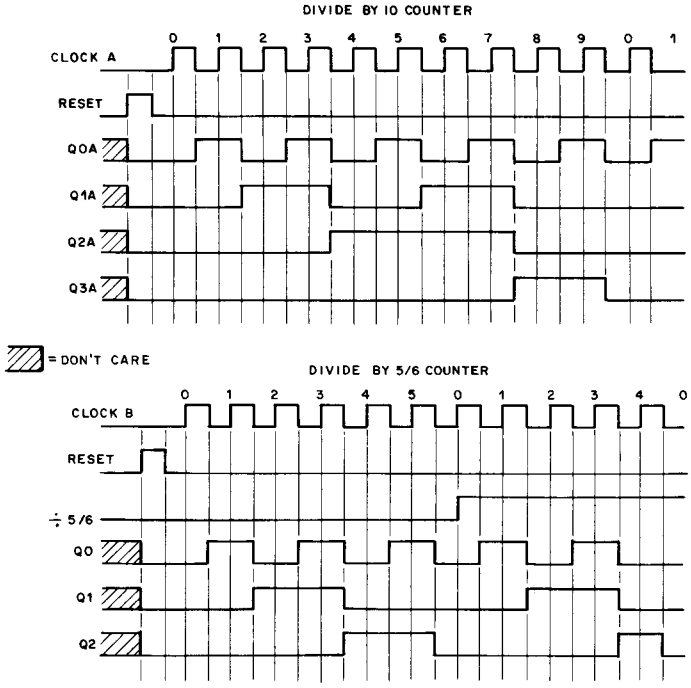


Fig. 6 - Timing diagrams. 92CM-39288

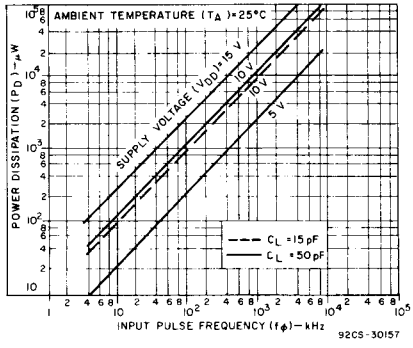
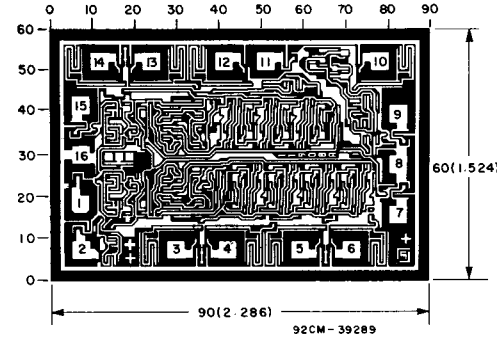
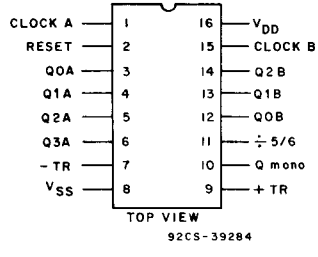


Fig. 7 - Typical dynamic power dissipation as a function of input pulse frequency.



Dimensions and pad layout for CD4566BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



TERMINAL ASSIGNMENT

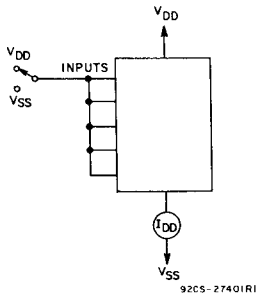


Fig. 8 - Quiescent device current test circuit.

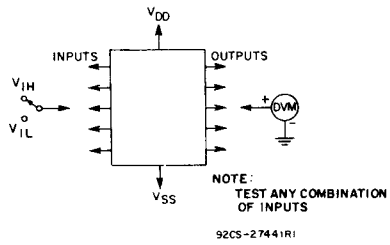


Fig. 9 - Input voltage test circuits.

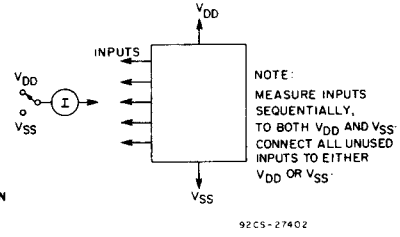


Fig. 10 - Input leakage current test circuit.

APPLICATION CIRCUIT

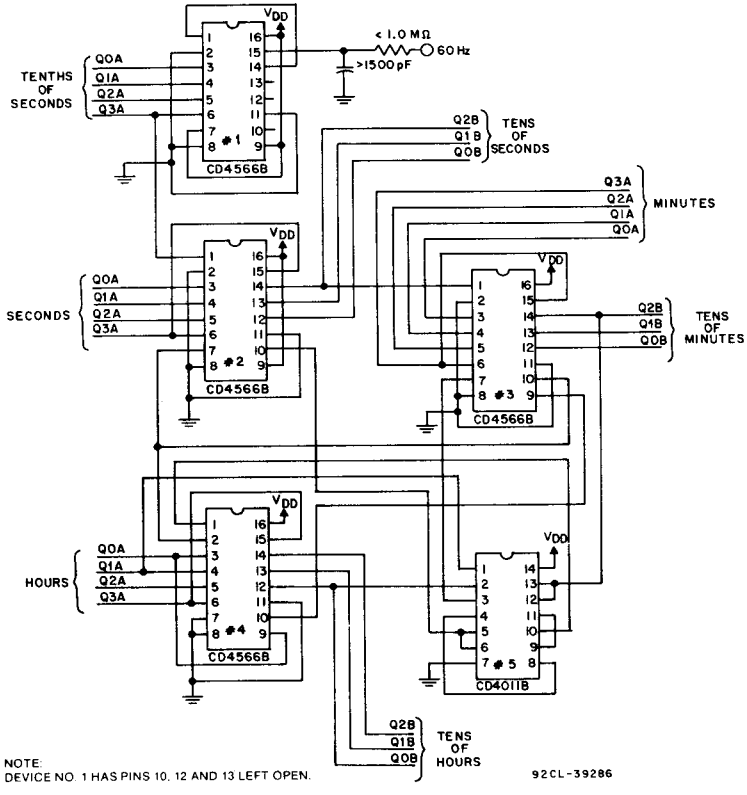


Fig. 11 - 12-hour clock circuit.