

CMOS 8-Bit Addressable Latch

High-Voltage Types (20-Volt Rating)

The RCA-CD4724B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

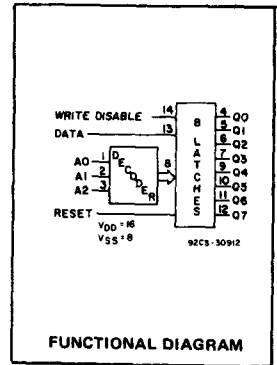
The CD4724B types are supplied in 16-lead hermetic ceramic dual-in-line packages (D and F suffixes), 16-lead plastic dual-in-line packages (E suffix), and in chip form (H suffix).

Features:

- Serial data input ■ Active parallel output
- Storage register capability ■ Master clear
- Can function as demultiplexer
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V (full package-temperature range), 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at $V_{DD} = 5$ V, 2 V at $V_{DD} = 10$ V, 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$



Applications:

- Multi-line decoders
- A/D converters

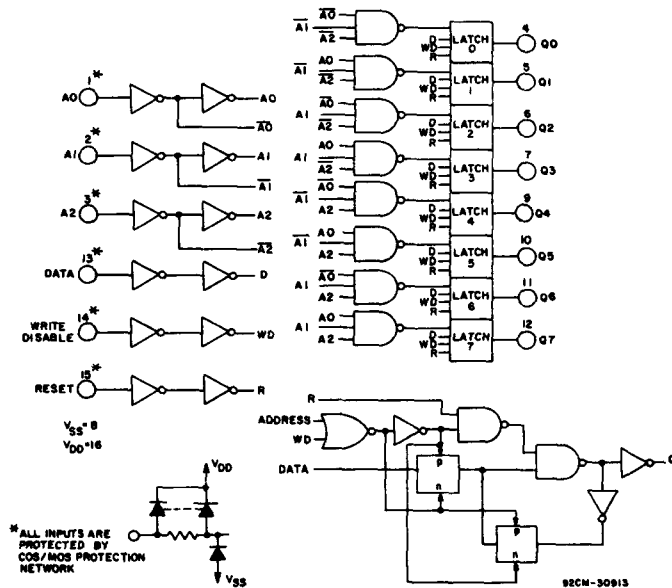
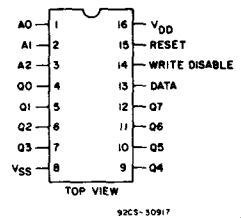


Fig. 1— Logic diagram of CD4724B and detail of 1 of 8 latches.



TERMINAL ASSIGNMENT

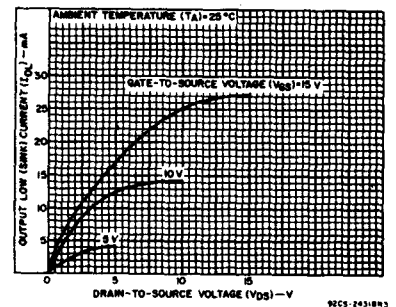


Fig. 2— Typical output low (sink) current characteristics.

CD4724B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$ (Unless otherwise specified)
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	SEE FIG. 15*	V _{DD} (V)	LIMITS		UNITS
			MIN.	MAX.	
Supply Voltage Range: (At $T_A = \text{Full Package Temperature Range}$)			3	18	V
Pulse Width, t_{PW} Data	4	5	200	—	ns
		10	100	—	
		15	80	—	
Address	8	5	400	—	ns
		10	200	—	
		15	125	—	
Reset	5	5	150	—	ns
		10	75	—	
		15	50	—	
Setup Time, t_S Data to WRITE DISABLE	6	5	100	—	ns
		10	50	—	
		15	35	—	
Hold Time, t_H Data to WRITE DISABLE	7	5	150	—	ns
		10	75	—	
		15	50	—	

* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong call from being addressed.

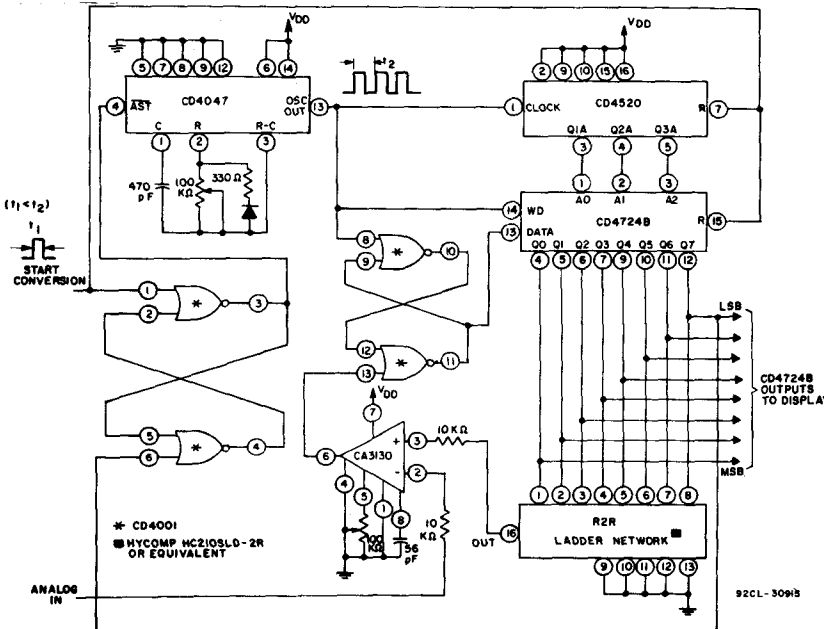
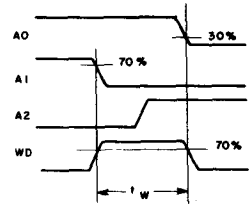


Fig. 5—A/D converter

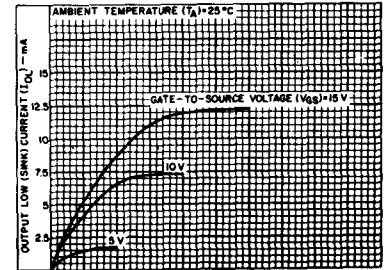
MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R = RESET



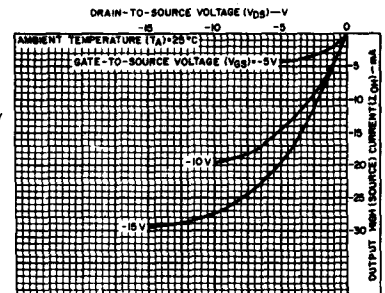
92CS-27676R1

Fig. 3—Definition of WRITE DISABLE ON time.



92CS-24319R1

Fig. 4—Minimum output low (sink) current characteristics.



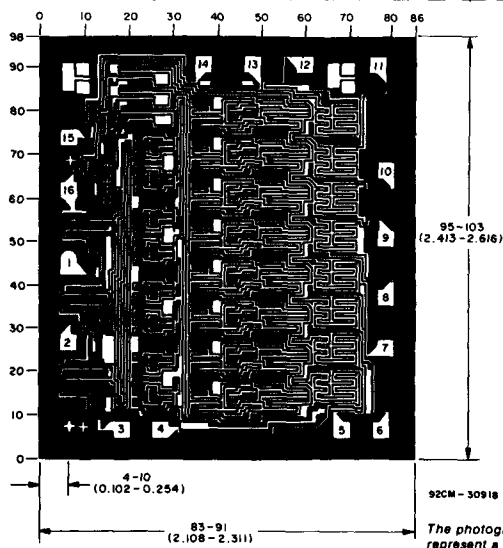
92CS-24320R5

Fig. 5—Typical output high (source) current characteristics.

CD4724B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D,F,H Packages Values at -40, +25, +85 Apply to E Package							
				-55	-40	+85	+125	+25			
				Min.	Typ.	Max.					
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0.04	5	μA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0.05			-	0	0.05	-	V
	-	0,10	10	0.05			-	0	0.05	-	
	-	0,15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4.95			4.95	5	-	-	V
	-	0,10	10	9.95			9.95	10	-	-	
	-	0,15	15	14.95			14.95	15	-	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5			-	-	1.5	-	V
	1, 9	-	10	3			-	-	3	-	
	1.5, 13.5	-	15	4			-	-	4	-	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5			3.5	-	-	-	V
	1, 9	-	10	7			7	-	-	-	
	1.5, 13.5	-	15	11			11	-	-	-	
Input Current I _{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA



CD4724BH DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

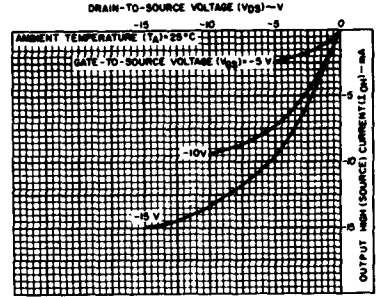


Fig. 7 - Minimum output high (source) current characteristics.

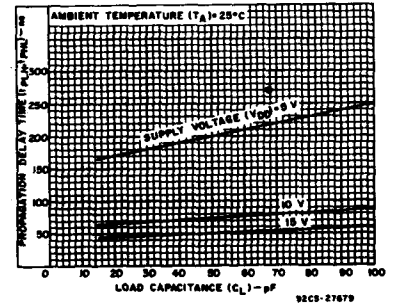


Fig. 8 - Typical propagation delay time (data to Qn) vs. load capacitance.

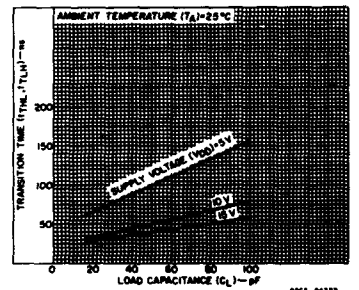


Fig. 9 - Typical transition time vs. load capacitance.

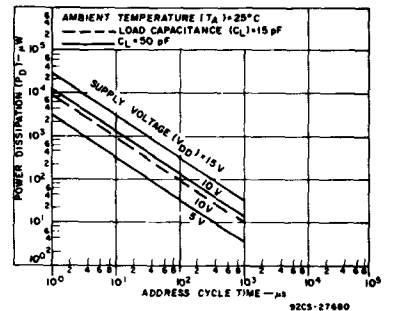


Fig. 10 - Typical dynamic power dissipation vs. address cycle time.

CD4724B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$,
Input $t_r, t_f = 20\text{ ns}$, $R_L = 200\text{ K}\Omega$**

CHARACTERISTIC	CONDITIONS		LIMITS		UNITS
	SEE Fig. 15*	V_{DD} (V)	ALL PACKAGE TYPES		
			TYP.	MAX.	
Propagation Delay: t_{PLH} , t_{PHL}	①	5	200	400	ns
		10	75	150	
		15	50	100	
Data to Output, WRITE DISABLE to Output, t_{PLH} , t_{PHL}	②	5	200	400	
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	③	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH} , t_{PHL}	⑨	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, t_{THL} , (Any Output) t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t_W Data	④	5	100	200	ns
		10	50	100	
		15	40	80	
Address	⑧	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	⑤	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	⑥	5	50	100	ns
		10	25	50	
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	⑦	5	75	150	ns
		10	40	75	
		15	25	50	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

*Circled numbers refer to times indicated on master timing diagram.

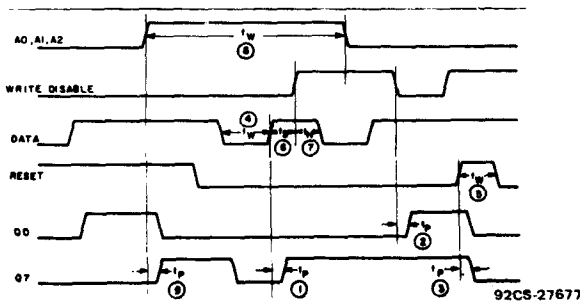


Fig. 15— Master timing diagram.

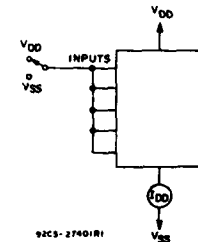


Fig. 11— Quiescent device current test circuit.

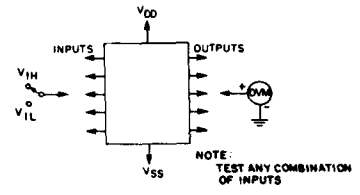


Fig. 12— Input voltage test circuit.

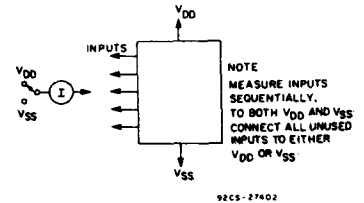


Fig. 13— Input current test circuit.

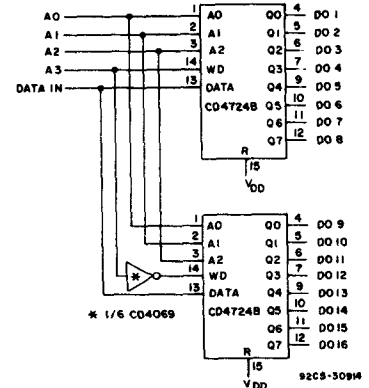


Fig. 14— 1 of 16 decoder/demultiplexer.

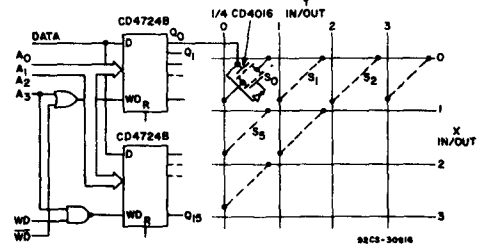


Fig. 16— Multiple selection decoding — 4 x 4 crosspoint switch.