

PWM Controller

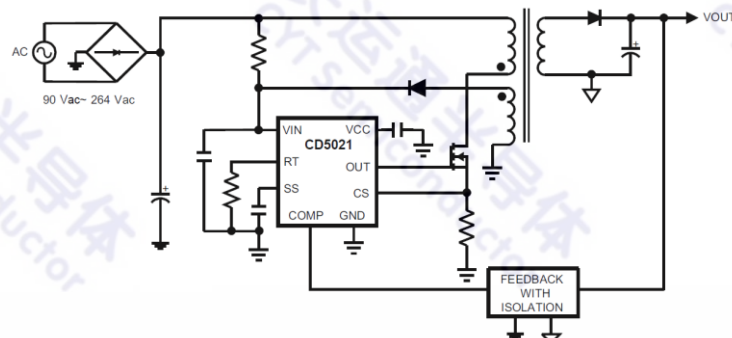
Features

- Ultra-low Startup Current
- Current Mode Control
- Skip Cycle Mode for Low Standby Power
- Single Resistor Programmable Oscillator
- Synchronizable Oscillator
- Adjustable Soft-Start
- Integrated 0.7A Peak Gate Driver
- Direct Opto-Coupler Interface
- Maximum Duty Cycle Limiting 85%
- Slope Compensation
- Undervoltage Lockout (UVLO) with Hysteresis
- Cycle-by-Cycle Overcurrent Protection
- Hiccup Mode for Continuous Overload Protection
- Leading Edge Blanking of Current Sense Signal
- Packages: VSSOP8

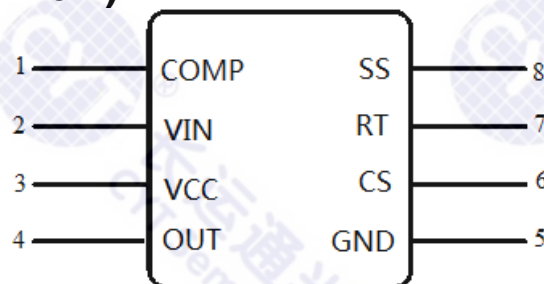
Applications

- DCM/CCM Flyback Converters
- Industrial Power Conversion
- SMPS for Smart Meters and Audio Amplifiers
- Building Automation and White Goods SMPS
- Isolated Telecom Power Supplies

Typical Application Circuit



Pin Configuration (Top View)



Absolute Maximum Ratings

VIN to GND	-0.3V ~ 30V
VCC to GND	-0.3V ~ 10V
CS to GND	-0.3V ~ 1.25V
RT to GND	-0.3V ~ 5.5V
COMP, SS to GND	-0.3V ~ 7V

Recommended Operation Conditions

VIN Voltage ^a	8V ~ 30V
VCC Voltage	8V ~ 10V
operating temperature range	-40°C ~ 125°C

^a When the V_{IN} is greater than or equal to 20V at the first startup, it can work normally.

Electrical Characteristics

Symbol	Character	Conditions	Mni.	Typ.	Max.	Unit
V_{CC}	VCC regulated output	COMP=5V, CS=0V	8.0	8.5	9.0	V
V_{VIN-EN}	VCC Regulator enable threshold	-	17	20	23	V
$V_{VIN-DIS}$	VCC Regulator disable threshold	-	-	7.25	-	V
I_{VIN}	Operating supply current	COMP=0V, CS=0V	-	2.5	3.75	mA
$I_{VCC-limit}$	VCC regulator current limit	COMP=5V, CS=0V	15	22	-	mA
V_{VCC-EN}	Controller enable threshold	VIN=7V, CS=0V	6.5	7.2	7.5	V
$V_{VCC-DIS}$	Controller disable threshold		5.1	5.8	6.3	V
V_{CS}	CS limit threshold	-	0.45	0.50	0.55	V
I_{SS}	Soft-start current source	COMP=2V, CS=SS=0V	15	22	30	μ A
V_{SS-OCV}	SS pin open-circuit voltage	COMP=2V, C _{SS} =5nF	4.3	5.0	6.1	V
V_{COMP}	COMP open circuit voltage	SS=4.5V, C _{SS} =5nF	4.2	4.78	6.0	V
I_{COMP}	COMP short circuit current	COMP=0V, CS=0V	0.6	0.95	1.5	mA
F_{OSC}	Frequency	R _T =44.2k Ω	135	150	165	kHz
$Duty_{(max)}$	Max duty cycle		75	80	85	%
t_r	Rise time	COMP=2V, CS=0V, C _{LOAD} =1nF	-	25	-	ns
t_f	Fall time	COMP=2V, CS=0V, C _{LOAD} =1nF	-	10	-	ns

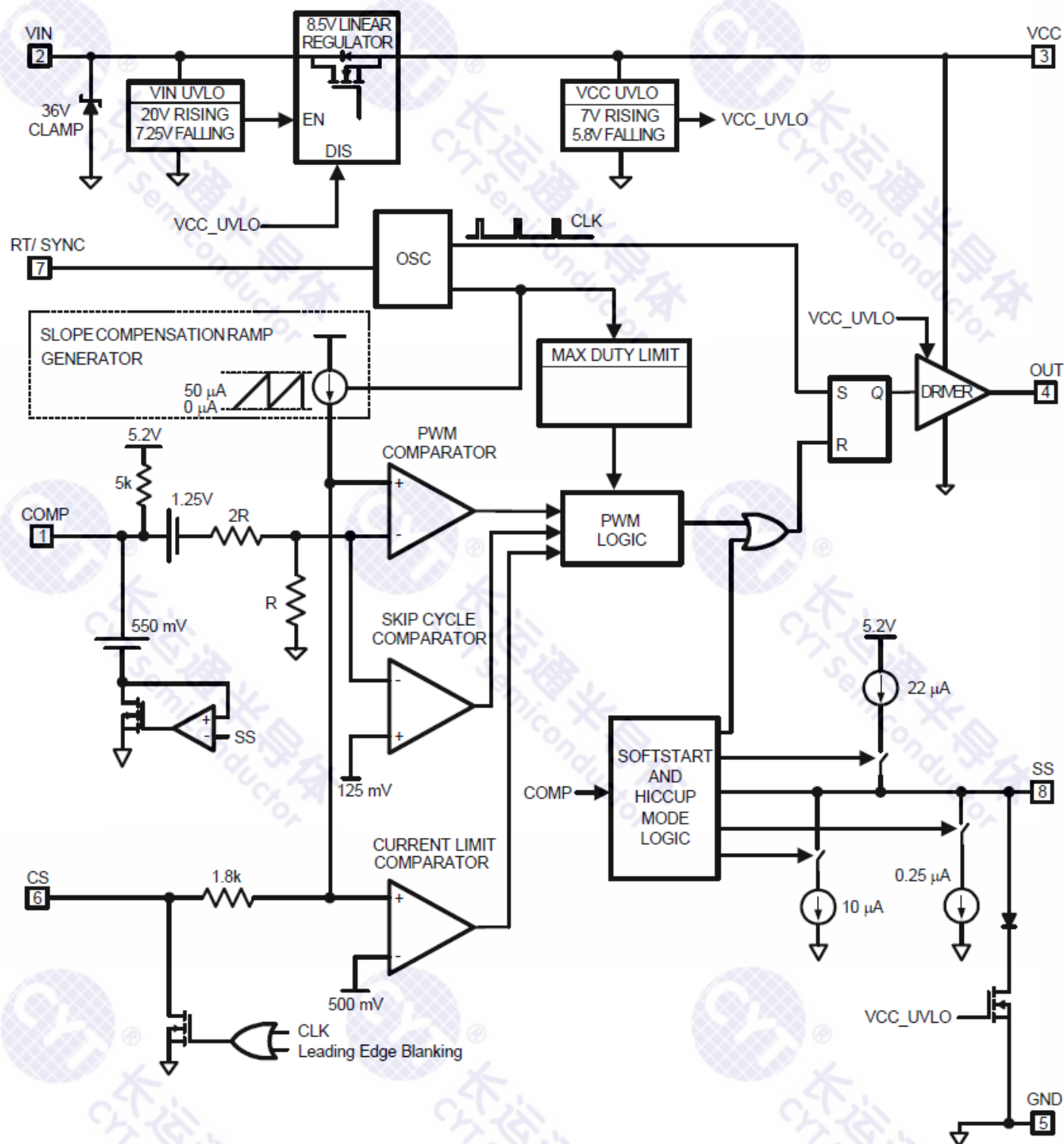
Note1: Unless otherwise specified, $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{IN}=25\text{V}$, $R_T=44.2\text{k}\Omega$

Note2: The frequency is calculated as follows: $R_T=6.63 \times 10^9 / F_{SW}$ (The unit is k Ω for R_T , F_{SW} is the switching frequency, the unit is kHz.)

Pin Functions

NO.	Name	Description	Application Information
1	COMP	Control input for the Pulse Width Modulator and Hiccup comparators.	COMP pull-up is provided by an internal 5K resistor which may be used to bias an opto-coupler transistor.
2	VIN	Input voltage.	Input to start-up regulator. The VIN pin is clamped at 36 V by an internal zener diode.
3	VCC	Output only of a linear bias supply regulator. Nominally 8.5 V.	VCC provides bias to controller and gate drive sections of the CD5021. An external capacitor must be connected from this pin to ground.
4	OUT	MOSFET gate driver output.	High current output to the external MOSFET gate input with source/sink current capability of 0.3 A and 0.7 A respectively.
5	GND	Ground return.	-
6	CS	Current Sense input.	Current sense input for current mode control and over-current protection. Current limiting is accomplished using a dedicated current sense comparator. If the CS comparator input exceeds 0.5 V the OUT pin switches low for cycle-by-cycle current limit. CS is held low for 90ns after OUT switches high to blank the leading edge current spike.
7	RT	Oscillator timing resistor pin and synchronization input.	An external resistor connected from RT to GND sets the oscillator frequency. This pin will also accept synchronization pulses from an external clock.
8	SS	Soft-start / Hiccup time	An external capacitor and an internal 22 μ A current source set the soft-start ramp. The soft -start capacitor controls both the soft-start rate and the hiccup mode period.

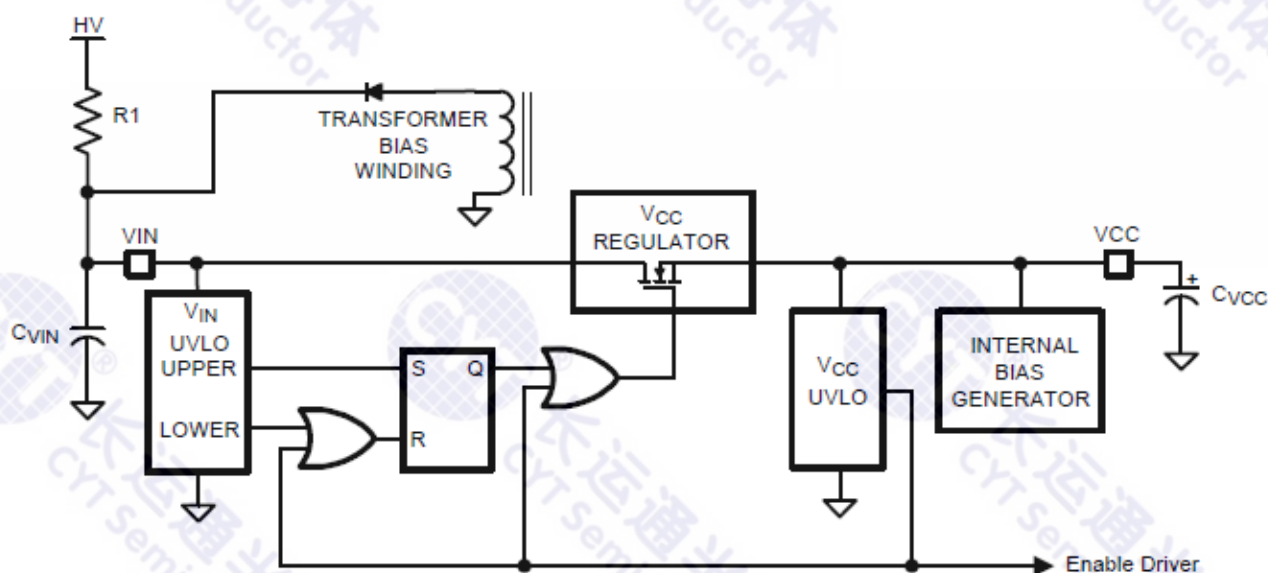
Functional Block Diagram



Application Information

As shown in the following figure, the input capacitor C_{VIN} is trickle charged through the start-up resistor $R1$, when the rectified ac input voltage HV is applied. The V_{IN} current consumed by the CD5021 is only 18 μA (nominal) while the capacitor C_{VIN} is initially charged to the start-up threshold. When the input voltage, V_{IN} reaches the upper V_{IN} UVLO threshold of 20 V, the internal VCC linear regulator is enabled. The VCC regulator will remain on until V_{IN} falls to the lower UVLO threshold of 7.25 V (12.5 V hysteresis). When the VCC regulator is turned on, the external capacitor at the VCC pin begins to charge. The PWM controller, soft-start circuit and gate driver are enabled when the VCC voltage reaches the VCC UVLO upper threshold of 7 V. The VCC UVLO has 1.2 V hysteresis between the upper and lower thresholds to avoid chattering during transients on the VCC pin. When the VCC UVLO enables the switching power supply, energy is transferred from the primary to the secondary transformer winding(s). A bias winding, As shown in the following figure, delivers power to the V_{IN} pin to sustain the VCC regulator. The voltage supplied should be from 11 V (VCC regulated voltage maximum plus VCC regulator dropout voltage) to 30 V (maximum operating V_{IN} voltage). The bias winding should always be connected to the V_{IN} pin. As shown in the following figure, Do not connect the bias winding to the VCC pin. The start-up sequence is completed and normal operation begins when the voltage from the bias winding is sufficient to maintain VCC level greater than the VCC UVLO threshold (5.8 V typical).

The CD5021 is designed for ultra-low start-up current into the V_{IN} pin. To achieve this very low start-up current, the VCC regulator of the CD5021 is unique as compared to the VCC regulator used in other controllers of the CD5xxx family. The CD5021 is designed specifically for applications with the bias winding connected to the V_{IN} pin. As shown in the following figure.

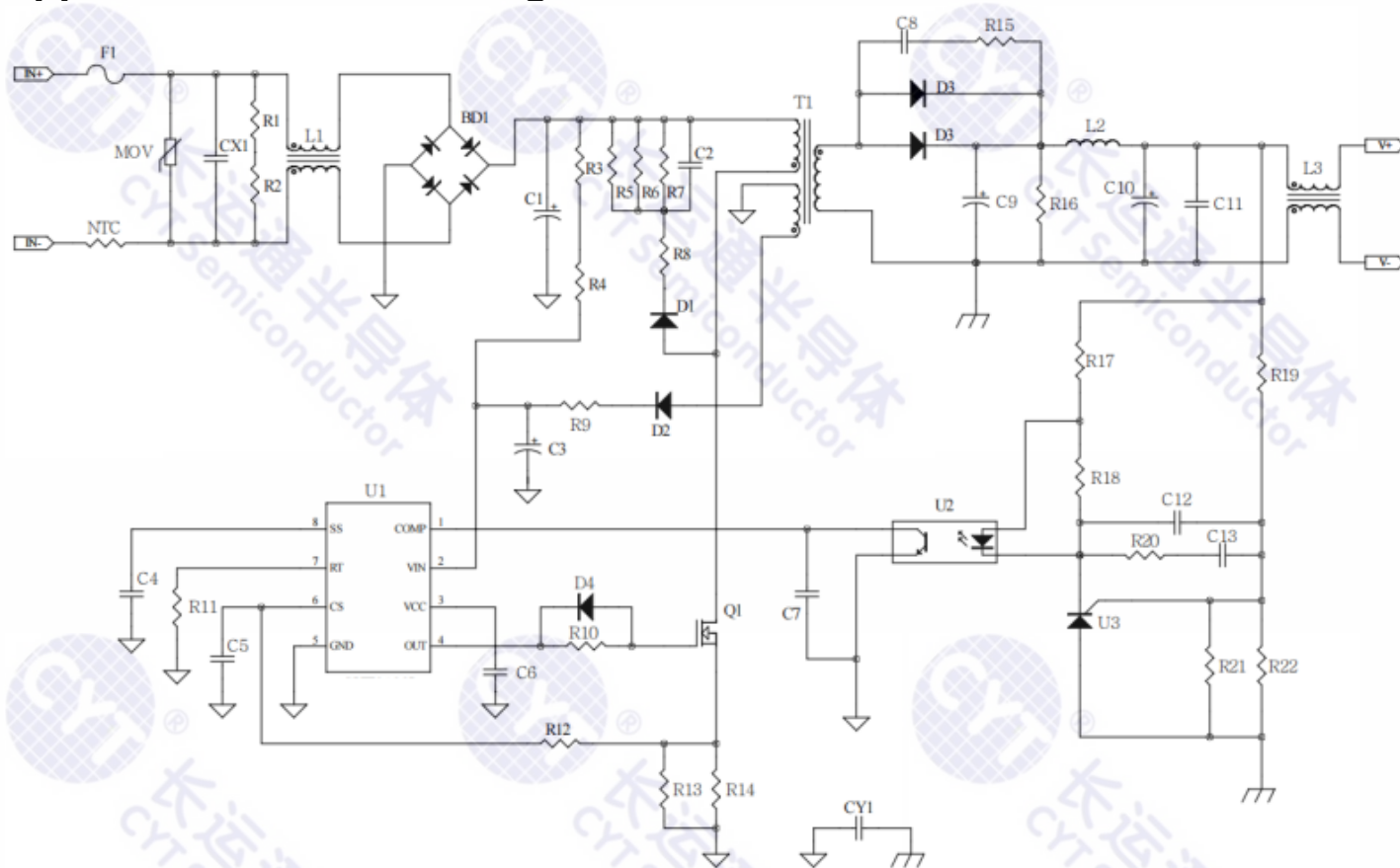


Start-Up Circuit Block Diagram

The size of the start-up resistor R1 not only affects power supply start-up time, but also power supply efficiency since the resistor dissipates power in normal operation. The ultra-low start-up current of the CD5021 allows a large value R1 resistor (up to 3 M Ω) for improved efficiency with reasonable start-up time.

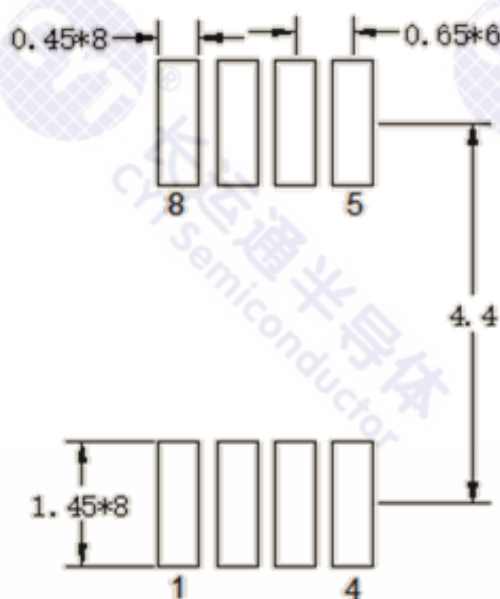
NOTE: It is not recommended that the bias winding be connected to the VCC pin of the CD5021. Doing so can cause the device to operate incorrectly or not at all.

Application schematic diagram



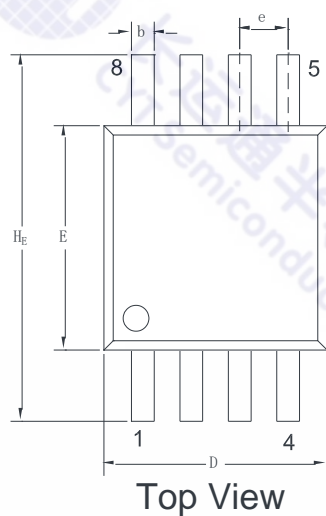
AC-DC Application circuit example

PCB Layout Diagram



VSSOP8

Package Diagram



VSSOP8

Size				
Symbol	Min.	Nom.	Max.	Unit
A	--	-	1.10	mm
A1	0.05	-	0.15	
A2	0.75	0.85	0.96	
A3	0.30	0.35	0.40	
b	0.28	-	0.36	
c	0.15	-	0.19	
D ^a	2.90	3.00	3.10	
E ^a	2.90	3.00	3.10	
e	0.65			
H _E	4.70	4.90	5.10	
L	0.40	-	0.70	
^a The size does not indude burrs.				

Order Information

Model	Package
CD5021IVS	VSSOP8

Declaration

1. The product cannot be used for equipment or devices that may cause personal injury or death for military, aircraft, automobile, medical, life support or life-saving. If you need to apply high reliability products to the above specific equipment or devices, please contact our sales staff to obtain relevant data manuals and samples.
2. Our company shall not be responsible for the quality of any of our products which are damaged by improper use or by exceeding even for a moment the rated value (such as maximum value, operating range, or other parameters) during use.
3. Our company continuously improves product quality, reliability, function or design, and reserves the right to change specifications.
4. Without the authorization of the company, the specification shall not be copied in whole or in part.