TEXAS INSTRUMENTS

# CD74FCT646

Data sheet acquired from Harris Semiconductor
SCHS261

January 1997

NOT RECOMMENDED
FOR NEW DESIGNS
Use CMOS Technology

## BiCMOS FCT Interface Logic, Octal Bus Transceiver/Register, Three-State

### Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at $V_{CC}$ = 5V, $T_A$ = 25$^o$C, $C_L$ = 50pF
- Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at $V_{CC}$ = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to $V_{CC}$
- BiCMOS Technology with Low Quiescent Power

### Ordering Information

| PART NUMBER | TEMP. RANGE ($^o$C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CD74FCT646EN | 0 to 70 | 24 Ld PDIP | E24.3 |
| CD74FCT646M | 0 to 70 | 24 Ld SOIC | M24.3 |
| CD74FCT646SM | 0 to 70 | 24 Ld SSOP | M24.209 |

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

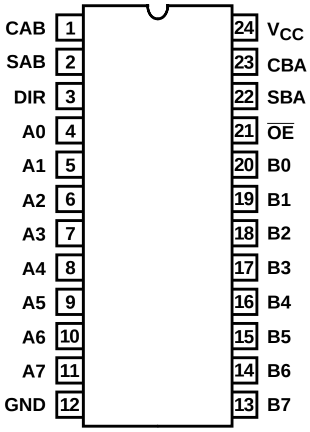
### Description

The CD74FCT646 three-state octal bus transceiver/register uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below $V_{CC}$. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes $V_{CC}$ bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

This device is a bus transceiver with D-Type flip-flops which act as internal storage registers on the LOW to HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

### Pinout

**CD74FCT646**
**(PDIP, SOIC, SSOP)**
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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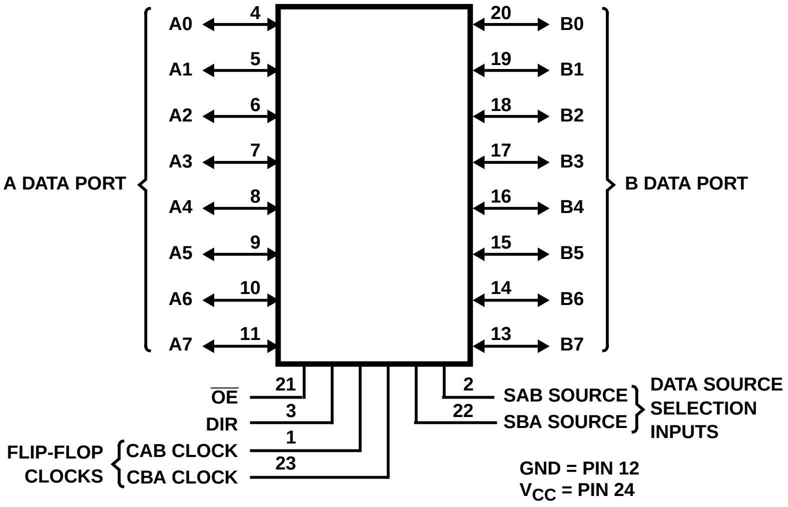
## *Functional Diagram*



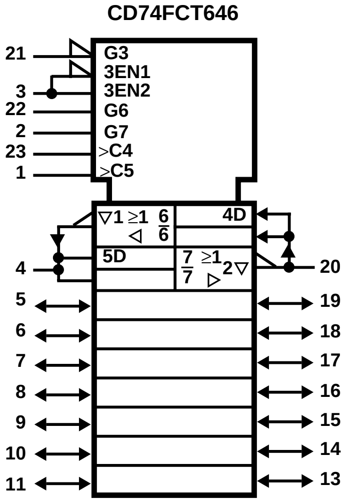
**TRUTH TABLE** (Note 1)

| **INPUTS** | | | | | | **DATA I/O** (Note 2) | | **OPERATION OR FUNCTION** |
|---|---|---|---|---|---|---|---|---|
| **OE** | **DIR** | **CAB** | **CBA** | **SAB** | **SBA** | **A0 THRU A7** | **B0 THRU B7** | **CD74FCT646** |
| X<br>X | X<br>X | ↑<br>X | X<br>↑ | X<br>X | X<br>X | Input<br>Not Specified | Not Specified<br>Input | Store A, B Unspecified<br>Store B, A Unspecified |
| H<br>H | X<br>X | ↑<br>H or L | ↑<br>H or L | X<br>X | X<br>X | Input | Input | Store A and B Data<br>Isolation, Hold Storage |
| L<br>L | L<br>L | X<br>X | X<br>H or L | X<br>X | L<br>H | Output | Input | Real Time B Data to A Bus<br>Stored B Data to A Bus |
| L<br>L | H<br>H | X<br>H or L | X<br>X | L<br>H | X<br>X | Input | Output | Real Time A Data to B Bus<br>Stored A Data to B Bus |

NOTES:

1. H= HIGH Voltage Level
   L = LOW Voltage Level
   ↑ = Transition from Low to High
   X = Immaterial
2. The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low to high transition of the clock inputs. To prevent excess currents in the high Z modes, all I/O terminals should be terminated with 10kΩ resistors.

## IEC Logic Symbol



## Absolute Maximum Ratings

| | |
|---|---|
| DC Supply Voltage ($V_{CC}$) | -0.5V to 6V |
| DC Diode Current, $I_{IK}$ (For $V_I < -0.5V$) | -20mA |
| DC Output Diode Current, $I_{OK}$ (for $V_O < -0.5V$) | -50mA |
| DC Output Sink Current per Output Pin, IO | 70mA |
| DC Output Source Current per Output Pin, IO | -30mA |
| DC $V_{CC}$ Current ($I_{CC}$) | 140mA |
| DC Ground Current ($I_{GND}$) | 528mA |

## Operating Conditions

| | |
|---|---|
| Operating Temperature Range, $T_A$ | $0^{o}C$ to $70^{o}C$ |
| Supply Voltage Range, $V_{CC}$ | 4.75V to 5.25V |
| DC Input Voltage, $V_I$ | 0 to $V_{CC}$ |
| DC Output Voltage, $V_O$ | 0 to $\leq V_{CC}$ |
| Input Rise and Fall Slew Rate, dt/dv | 0 to 10ns/V |

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ ($^{o}C/W$) |
|---|---|
| PDIP Package | 75 |
| SOIC Package | 75 |
| SSOP Package | 125 |
| Maximum Junction Temperature | $150^{o}C$ |
| Maximum Storage Temperature Range | $-65^{o}C$ to $150^{o}C$ |
| Maximum Lead Temperature (Soldering 10s)<br>(SOIC and SSOP-Lead Tips Only) | $300^{o}C$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

3. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

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**Electrical Specifications** Commercial Temperature Range $0^{o}C$ to $70^{o}C$, $V_{CC}$ Max = 5.25V, $V_{CC}$ Min = 4.75V (Note 6)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $25^{o}C$ | | $0^{o}C$ TO $70^{o}C$ | | |
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | MAX | MIN | MAX | |
| High Level Input Voltage | $V_{IH}$ | | | 4.75 to 5.25 | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | | | 4.75 to 5.25 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -15 | Min | 2.4 | - | 2.4 | - | V |
| Low Level Output Voltage | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 64 | Min | - | 0.55 | - | 0.55 | V |
| High Level Input Current | $I_{IH}$ | $V_{CC}$ | | Max | - | 0.1 | - | 1 | µA |
| Low Level Input Current | $I_{IL}$ | GND | | Max | - | -0.1 | - | -1 | µA |
| Three-State Leakage Current | $I_{OZH}$ | $V_{CC}$ | | Max | - | 0.5 | - | 10 | µA |
| | $I_{OZL}$ | GND | | Max | - | -0.5 | - | -10 | µA |
| Input Clamp Voltage | $V_{IK}$ | $V_{CC}$ or GND | -18 | Min | - | -1.2 | - | -1.2 | V |
| Short Circuit Output Current (Note 4) | $I_{OS}$ | $V_O = 0$<br>$V_{CC}$ or GND | | Max | -60 | - | -60 | - | mA |
| Quiescent Supply Current, MSI | $I_{CC}$ | $V_{CC}$ or GND | 0 | Max | - | 8 | - | 80 | µA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load | $\Delta I_{CC}$ | 3.4V (Note 5) | | Max | - | 1.6 | - | 1.6 | mA |

NOTES:

4. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
5. Inputs that are not measured are at $V_{CC}$ or GND.
6. FCT Input Loading: All inputs are 1 unit load. Unit load is $\Delta I_{CC}$ limit specified in Electrical Specifications table, e.g., 1.6mA Max. at $70^{o}C$.

## Switching Specifications Over Operating Range FCT Series $t_r$, $t_f$ = 2.5ns, $C_L$ = 50pF, $R_L$ (Figure 1) (Note 7)

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | 0°C TO 70°C | | UNITS |
|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | |
| Propagation Delays | | (Note 8) | | | | |
| Store An → Bn, Store Bn → An, An → Bn, Bn → An | $t_{PLH}$, $t_{PHL}$ | 5 | 6.8 | 2 | 9 | ns |
| Select to Data | $t_{PLH}$, $t_{PHL}$ | 5 | 8.3 | 2 | 11 | ns |
| Output Enable to Output | $t_{PZL}$, $t_{PZH}$ | 5 | 10.5 | 2 | 14 | ns |
| Output Disable to Output | $t_{PLZ}$, $t_{PHZ}$ | 5 | 6.8 | 2 | 9 | ns |
| Power Dissipation Capacitance | $C_{PD}$ (Note 8) | - | - | - | - | pF |
| Minimum (Valley) $V_{OHV}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OHV}$ | 5 | 0.5 | - | - | V |
| Maximum (Peak) $V_{OLP}$ During Switching of Other Outputs (Output Under Test Not Switching) | $V_{OLP}$ | 5 | 1 | - | - | V |
| Input Capacitance | $C_I$ | - | - | - | 10 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | - | - | 15 | pF |

NOTES:

7. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
8. $C_{PD}$, measured per flip-flop, is used to determine the dynamic power consumption.
   $P_D$ (per package) = $V_{CC}\ I_{CC} + \Sigma(V_{CC}^2\ f_I\ C_{PD} + V_O^2\ f_O C_L + V_{CC}\ \Delta I_{CC}\ D)$ where:
   $V_{CC}$ = supply voltage
   $\Delta I_{CC}$ = flow through current x unit load
   $C_L$ = output load capacitance
   D = duty cycle of input high
   $f_O$ = output frequency
   $f_I$ = input frequency

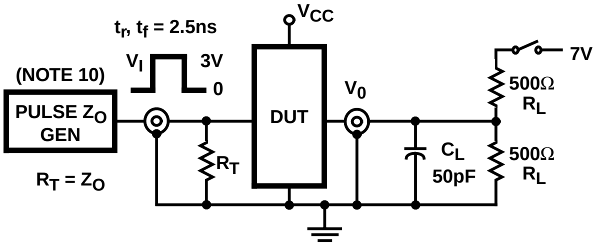
## Prerequisite For Switching

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25°C | 0°C TO 70°C | | UNITS |
|---|---|---|---|---|---|---|
| | | | TYP | MIN | MAX | |
| Maximum Frequency | $f_{MAX}$ | 5 (Note 9) | - | 85 | - | ns |
| Data to Clock Setup Time | $t_{SU}$ | 5 | - | 4 | - | ns |
| Data to Clock Hold Time | $t_H$ | 5 | - | 2 | - | ns |
| Clock Pulse Width | $t_W$ | 5 | - | 6 | - | ns |

NOTE:

9. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

## *Test Circuits and Waveforms*



NOTE:

10. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT}$ ≤ 50Ω; $t_f$, $t_r$ ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

**SWITCH POSITION**

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$, $t_{PZL}$, Open Drain | Closed |
| $t_{PHZ}$, $t_{PZH}$, $t_{PLH}$, $t_{PHL}$ | Open |

DEFINITIONS:

$C_L$ = Load capacitance, includes jig and probe capacitance.

$R_T$ = Termination resistance, should be equal to $Z_{OUT}$ of the Pulse Generator.

$V_{IN}$ = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

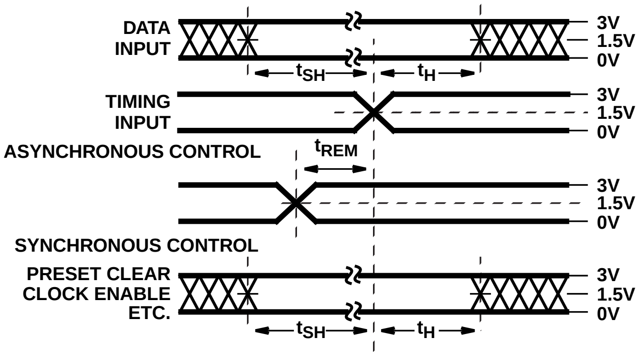


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

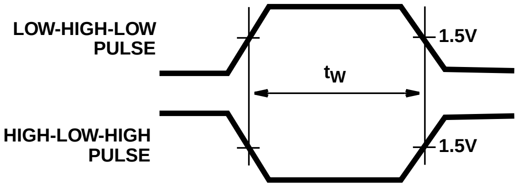


FIGURE 3. PULSE WIDTH

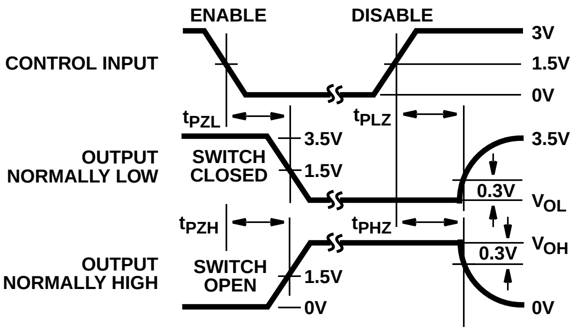


FIGURE 4. ENABLE AND DISABLE TIMING

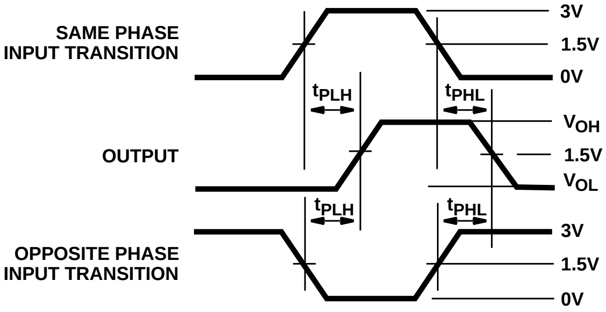
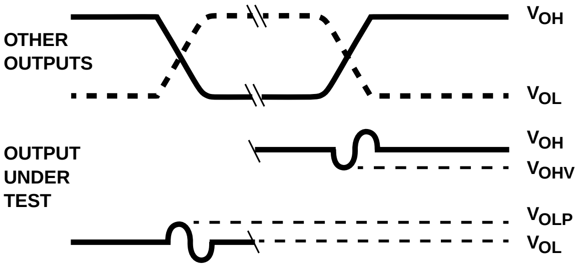


FIGURE 5. PROPAGATION DELAY

## *Test Circuits and Waveforms* (Continued)



NOTES:

11. $V_{OLP}$ is measured with respect to a ground reference near the output under test. $V_{OHV}$ is measured with respect to $V_{OH}$.
12. Input pulses have the following characteristics:
    $P_{RR} \le 1MHz$, $t_r = 2.5ns$, $t_f = 2.5ns$, skew 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

**FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS**

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