

January 1997

**NOT RECOMMENDED  
FOR NEW DESIGNS**  
Use CMOS Technology

# CD74FCT651, CD74FCT652

## BiCMOS FCT Interface Logic, Octal Bus Transceivers/Registers, Three-State

### Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 50pF$
- CD75FCT651
  - Inverting
- CD74FCT652
  - Noninverting
- Family Features
  - SCR Latchup Resistant BiCMOS Process and Circuit Design
  - Speed of Bipolar FAST™/AS/S
  - 64mA Output Sink Current
  - Output Voltage Swing Limited to 3.7V at  $V_{CC} = 5V$
  - Controlled Output Edge Rates
  - Input/Output Isolation to  $V_{CC}$
  - BiCMOS Technology with Low Quiescent Power

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT651EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT652EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT651M	0 to 70	24 Ld SOIC	M24.3
CD74FCT652M	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

### Description

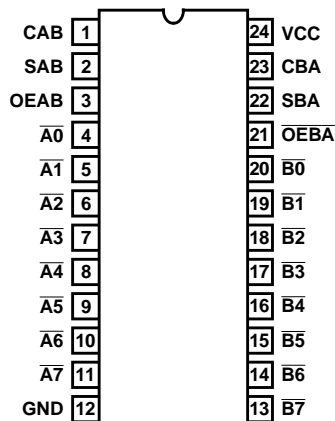
The CD74FCT651 and CD74FCT652 three-state, octal bus transceivers/registers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

These devices consist of bus transceiver circuits, D-Type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and OEBA are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data. The following examples demonstrate the four fundamental bus management functions that can be performed with the octal bus transceivers and registers.

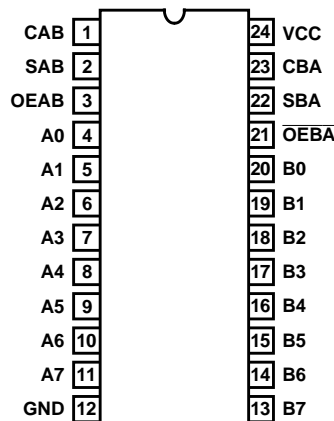
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low to high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-Type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

### Pinouts

CD74FCT651 (PDIP, SOIC)  
TOP VIEW

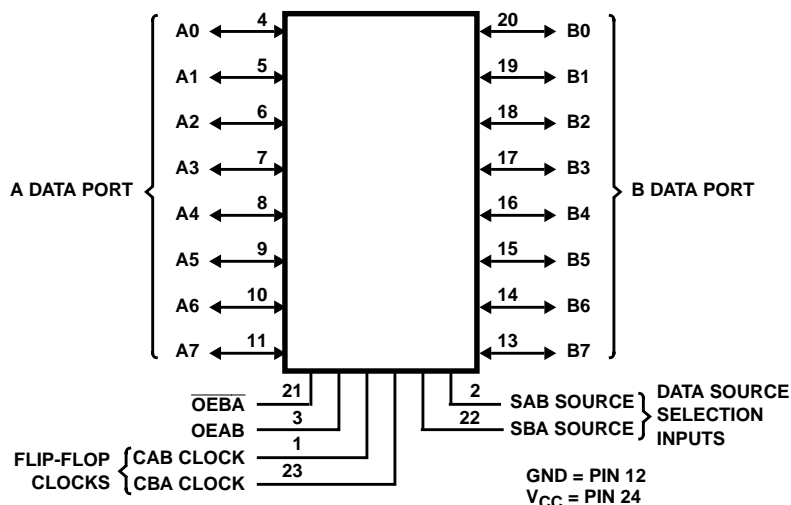


CD74FCT652 (PDIP, SOIC)  
TOP VIEW



# CD74FCT651, CD74FCT652

## Functional Diagram



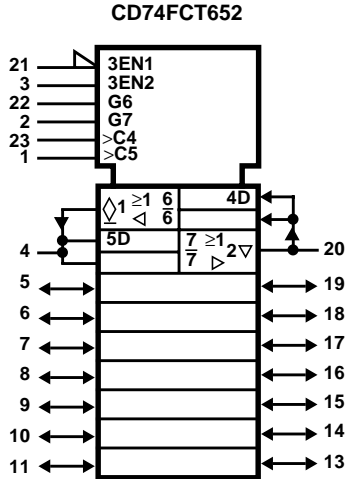
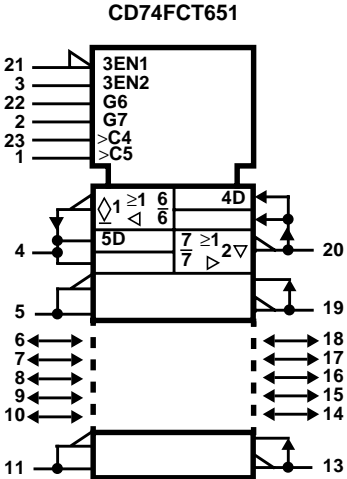
TRUTH TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	OEBA	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD74FCT651	CD74FCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation (Note 1)	Isolation (Note 1)
L	H	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified (2)	Store A, Hold B	Store A, Hold B
X	H	↑	↑	X (3)	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified (2)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X (3)	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\bar{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\bar{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\bar{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\bar{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\bar{A}$ Data to B Bus	Stored A Data to B Bus
								Stored $\bar{B}$ Data to A Bus	Stored B Data to A Bus

### NOTES:

1. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
2. The data output functions may be enabled or disabled by various signals at the OEAB or  $\overline{OEBA}$  inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select control = L; clocks can occur simultaneously. Select control = H; clocks must be staggered in order to load both registers.

**IEC Logic Symbol**



# CD74FCT651, CD74FCT652

## Absolute Maximum Ratings

DC Supply Voltage ( $V_{CC}$ )	-0.5V to 6V
DC Input Diode Current, $I_{IK}$ (For $V_I < -0.5V$ )	-20mA
DC Output Diode Current, $I_{OK}$ (for $V_O < -0.5V$ )	-50mA
DC Output Sink Current per Output Pin, $I_O$	70mA
DC Output Source Current per Output Pin, $I_O$	-30mA
DC $V_{CC}$ Current ( $I_{CC}$ )	140mA
DC Ground Current ( $I_{GND}$ )	528mA

## Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	75
SOIC Package	75
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC-Lead Tips Only)

## Operating Conditions

Operating Temperature Range ( $T_A$ )	0 $^{\circ}C$ to 70 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	4.75V to 5.25V
DC Input Voltage, $V_I$	0 to $V_{CC}$
DC Output Voltage, $V_O$	0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, $dt/dv$	0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications Commercial Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$ , $V_{CC}$ Max = 5.25V, $V_{CC}$ Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> )				UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		25°C		0°C TO 70°C		
					MIN	MAX	MIN	MAX	
High Level Input Voltage	V <sub>IH</sub>			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	64	Min	-	0.55	-	0.55	V
High Level Input Current	I <sub>IH</sub>	V <sub>CC</sub>		Max	-	0.1	-	1	μA
Low Level Input Current	I <sub>IL</sub>	GND		Max	-	-0.1	-	-1	μA
Three-State Leakage Current	I <sub>OZH</sub>	V <sub>CC</sub>		Max	-	0.5	-	10	μA
	I <sub>OZL</sub>	GND		Max	-	-0.5	-	-10	μA
Input Clamp Voltage	V <sub>IK</sub>	V <sub>CC</sub> or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 5)	I <sub>OS</sub>	V <sub>O</sub> = 0 V <sub>CC</sub> or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	Max	-	8	-	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI <sub>CC</sub>	3.4V (Note 6)		Max	-	1.6	-	1.6	mA

NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at  $V_{CC}$  or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is  $\Delta I_{CC}$  limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70 $^{\circ}C$ .

## CD74FCT651, CD74FCT652

### Switching Specifications Over Operating Range FCT Series $t_r, t_f = 2.5\text{ns}$ , $C_L = 50\text{pF}$ , $R_L$ (Figure 4)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C	0°C TO 70°C		UNITS	
			TYP	MIN	MAX		
Propagation Delays							
Stored $\overline{A_n} \rightarrow B_n$	CD74FCT651	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
Stored $A_n \rightarrow B_n$	CD74FCT652	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
Stored $\overline{B_n} \rightarrow A_n$	CD74FCT651	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
Stored $B_n \rightarrow A_n$	CD74FCT652	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
$\overline{A_n} \rightarrow B_n$	CD74FCT651	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
$A_n \rightarrow B_n$	CD74FCT652	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
$\overline{B_n} \rightarrow A_n$	CD74FCT651	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
$B_n \rightarrow A_n$	CD74FCT652	t <sub>PLH</sub> , t <sub>PHL</sub>	5	6.8	2	9	ns
Select to Data	CD74FCT651, CD74FCT652	t <sub>PLH</sub> , t <sub>PHL</sub>	5	8.3	2	11	ns
Three-State Enabling Time, Bus to Output or Register to Output	CD74FCT651, CD74FCT652	t <sub>PZL</sub> , t <sub>PZH</sub>	5	7.5	2	10	ns
Three-State Disabling Time, Bus to Output or Register to Output	CD74FCT651, CD74FCT652	t <sub>PLZ</sub> , t <sub>PHZ</sub>	5	7.5	2	10	ns
Power Dissipation Capacitance	C <sub>PD</sub> (Note 8)	–				pF	
Minimum (Valley) V <sub>OHV</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub>	5	0.5 Typical at 25°C			V	
Maximum (Peak) V <sub>OLP</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub>	5	1 Typical at 25°C			V	
Input Capacitance	C <sub>I</sub>	-	-	-	10	pF	
Input/Output Capacitance	C <sub>I/O</sub>	-	-	-	15	pF	

NOTE:

8.  $C_{PD}$ , measured per flip-flop, is used to determine the dynamic power consumption.

$P_D$  (per package) =  $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$  where:

$V_{CC}$  = supply voltage

$\Delta I_{CC}$  = flow through current x unit load

$C_L$  = output load capacitance

$D$  = duty cycle of input high

$f_O$  = output frequency

$f_I$  = input frequency

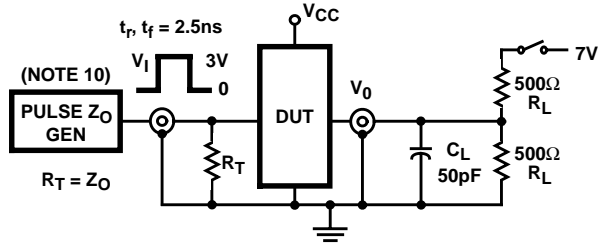
### Prerequisite for Switching

PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Maximum Frequency	$f_{MAX}$	5 (Note 9)	–	85	–	MHz
Data to Clock Setup Time	$t_{SU}$	5	–	4	–	ns
Data to Clock Hold Time	$t_H$	5	–	2	–	ns
Clock Pulse Width	$t_W$	5	–	6	–	ns

NOTE:

9. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

## Test Circuits and Waveforms



NOTE:

10. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_r, t_f \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

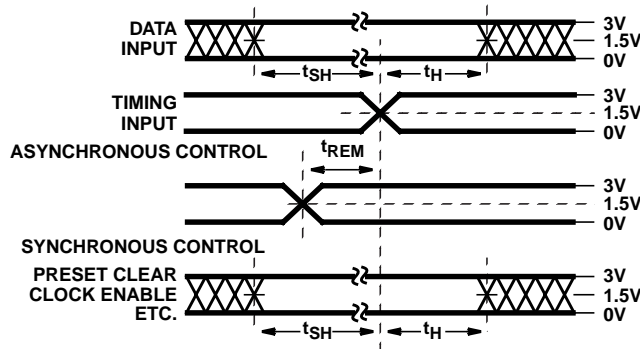


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

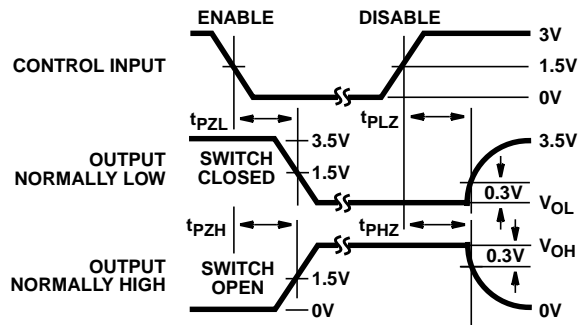


FIGURE 4. ENABLE AND DISABLE TIMING

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}$ , Open Drain	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.

$R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

$V_{IN} = 0\text{V}$  to  $3\text{V}$ .

Input:  $t_r = t_f = 2.5\text{ns}$  (10% to 90%), unless otherwise specified

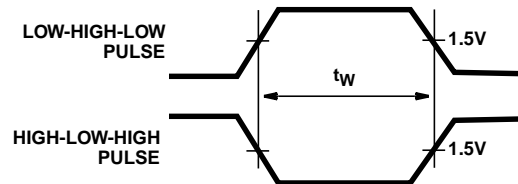


FIGURE 3. PULSE WIDTH

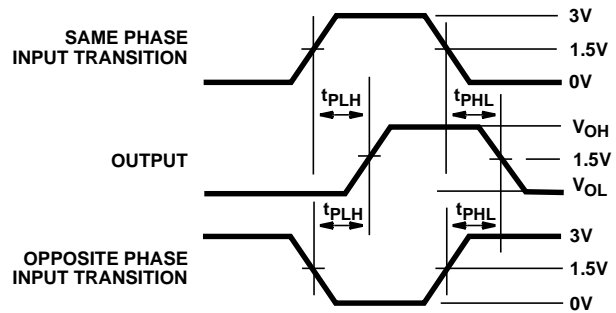
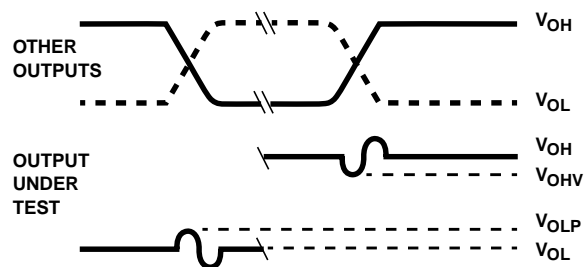


FIGURE 5. PROPAGATION DELAY

## Test Circuits and Waveforms (Continued)



### NOTES:

11.  $V_{OLP}$  is measured with respect to a ground reference near the output under test.  $V_{OHV}$  is measured with respect to  $V_{OH}$ .
12. Input pulses have the following characteristics:  
 $PRR \leq 1\text{MHz}$ ,  $t_r = 2.5\text{ns}$ ,  $t_f = 2.5\text{ns}$ , skew 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1 $\mu\text{F}$  capacitor. Scope and probes require 700MHz bandwidth.

**FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS**

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74FCT651EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
CD74FCT651M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
CD74FCT652EN	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
CD74FCT652M	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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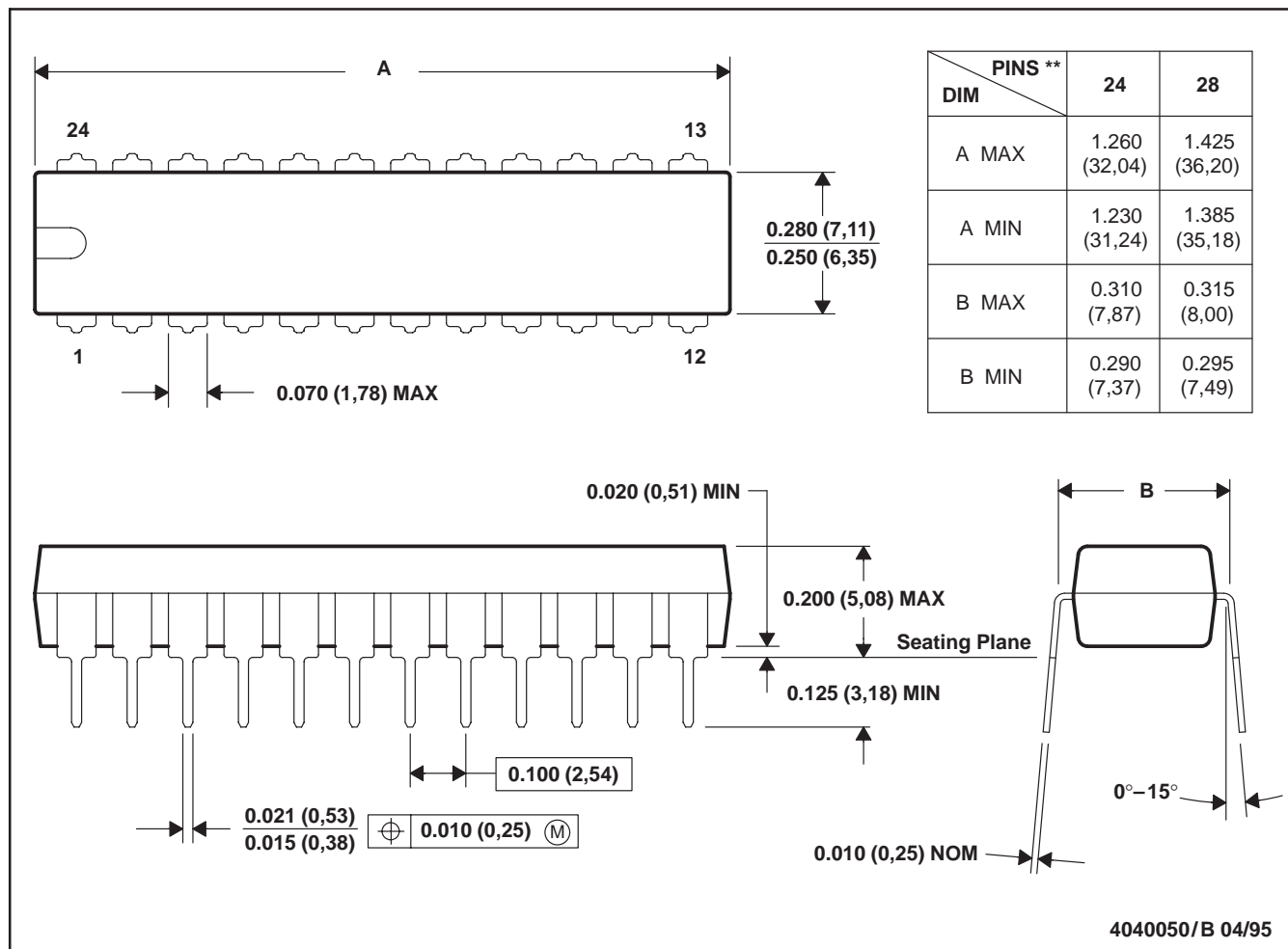
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## NT (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

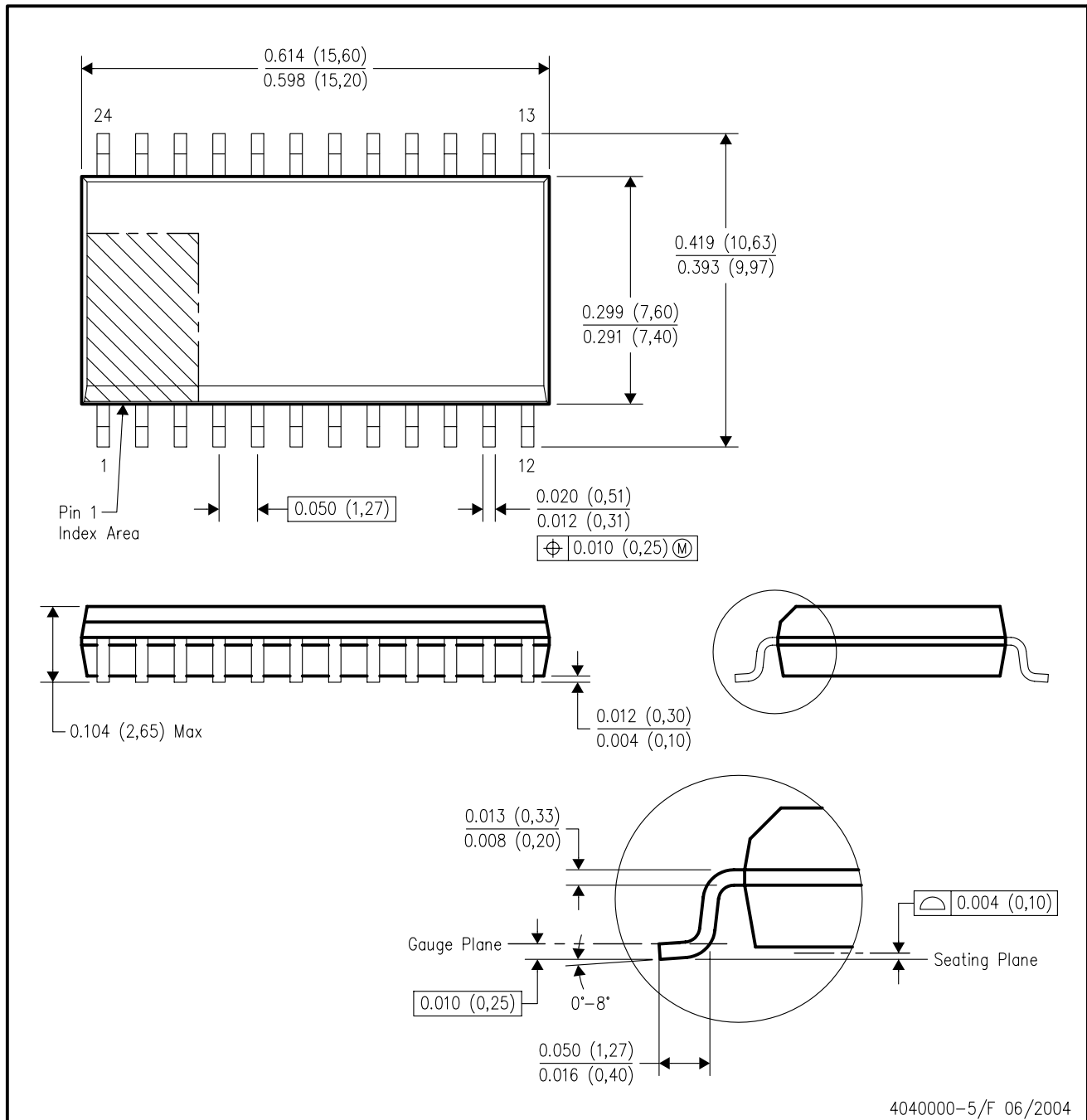
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

## DW (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

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Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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