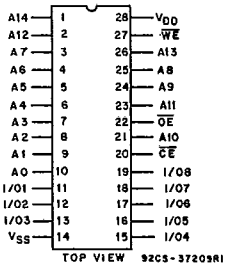
CDM62256C/3

T-46-23-14

Advance Information

High-Reliability CMOS 32,768-Word By 8-Bit LSI Static RAM

Features:
- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Industry-standard 28-pin configuration*
- *Input address buffers gated off with chip disable*
- *Fast access time: t_{AA} = 100 ns/120 ns*
- *Low standby and operating power: I_{DDS1} = 1 mA typical I_{DDA} = 90 mA maximum*
- *Operating temperature range (max. rating): −55° C to +125° C*
- *Data retention voltage: 2.5 V minimum*



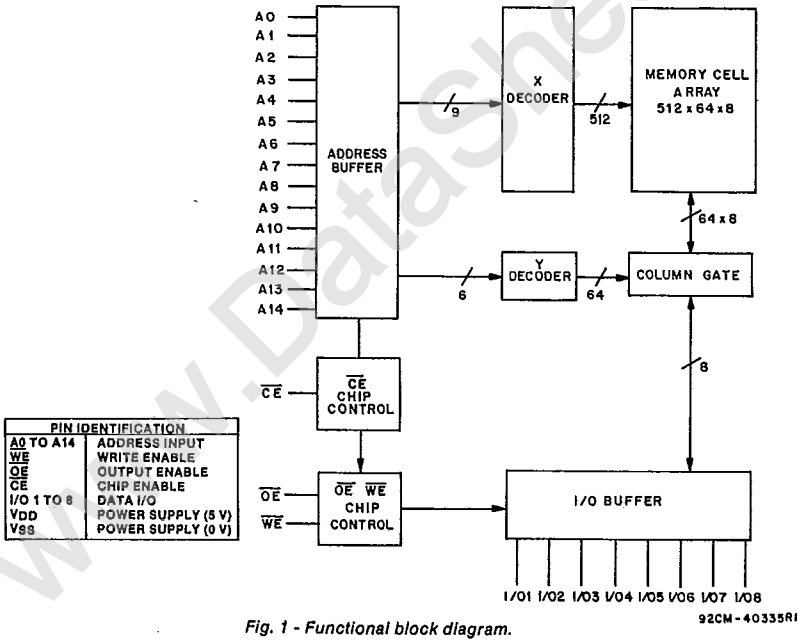
TERMINAL ASSIGNMENT
28-Lead Package

Package Specifications
See Section 11, Fig. 7, b1

The RCA-CDM62256C/3 is a high-reliability 32,768-word by 8-bit static random-access memory. It is designed for use in memory systems where high speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

Chip Enable ($\overline{CE}$) gates the address and output buffers and powers down the chip to the low power standby mode. The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM62256C/3 is supplied in a 28-lead hermetic, dual-in-line side-brazed ceramic package (D suffix) and in a leadless chip package (J suffix) as a custom selection.



PIN IDENTIFICATION	
A0 TO A14	ADDRESS INPUT
WE	WRITE ENABLE
OE	OUTPUT ENABLE
CE	CHIP ENABLE
I/O 1 TO 8	DATA I/O
VDD	POWER SUPPLY (5 V)
VSS	POWER SUPPLY (0 V)

Fig. 1 - Functional block diagram.

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TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	STANDBY	HIGH Z	STANDBY
L	X	L	STABLE	WRITE	DATA IN	ACTIVE
L	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	H	STABLE	OUTPUT DISABLE	HIGH Z	ACTIVE

L = Low H = High X = H or L

MAXIMUM RATINGS, *Absolute-Maximum Values:*

*DC SUPPLY-VOLTAGE RANGE, (V_{DD}): ..... -0.5 to +7 V
*INPUT VOLTAGE RANGE, (V_{IN}) ..... -0.5** to +7 V
*INPUT/OUTPUT VOLTAGE RANGE ($V_{I/O}$): ..... -0.5** to V_{DD} +0.3 V
*(Voltage referenced to V_{SS} terminal)
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -55 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

**Min. V_{IN}, $V_{I/O}$ = -1 V for pulse width ≤ 50 ns.

RECOMMENDED DC OPERATING CONDITIONS at T_A = -55 to +125°C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
DC Operating Voltage Range	V_{DD}	4.5	5	5.5	V
Input Voltage Range	V_{IH}	2.2	3.5	V_{DD} + 0.3	
	V_{IL}	-0.3Δ	0	0.8	

Δ Minimum V_{IL} = -1 V for pulse width ≤ 50 ns.

STATIC ELECTRICAL CHARACTERISTICS at T_A = -55 to +125°C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		TEST CONDITIONS	LIMITS +25/-55°C MIN.	LIMITS +25/-55°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS
Input Leakage	I_{LI}	V_I = 0 to V_{DD}	—	±2	-1	±2	μA
Standby Supply Current	I_{DDS}	$\overline{CE}$ = V_{IH}	—	3.5	—	4	mA
	I_{DDS1}	$\overline{CE}$ ≥ V_{DD} -0.2 V	—	200	—	1000	μA
Average Operating Current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0 mA, t_{cyc} = Min.	—	90	—	90	mA
Output Leakage	I_{LO}	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{DD}	—	±2	—	±2	μA
High Level Output Voltage	V_{OH}	I_{OH} = -1 mA	2.4	—	2.4	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.4	—	0.4	

TERMINAL CAPACITANCE (f = 1 MHz, T_A = -55 to +125°C)

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Address Capacitance	C_{ADD}	V_{ADD} = 0 V	—	10*	pF
Input Capacitance	C_I	V_I = 0 V	—	10*	
I/O Terminal Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	—	10*	

* Guaranteed, not tested.

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SIGNAL DESCRIPTIONS

A0-A14 (Address Inputs):

These inputs must be stable prior to a write operation, but may change asynchronously during read functions.

I/01-I/08:

8-bit tristate data bus.

$\overline{CE}$ (Chip Enable):

Powers down the chip, disables Read and Write functions, and gates off address inputs.

$\overline{OE}$ (Output Enable):

Enables tristate outputs if $\overline{CE}$ is low and $\overline{WE}$ is high.

$\overline{WE}$ (Write Enable):

Enables Write function, if $\overline{CE}$ is low. $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be tristated and a Write will occur).

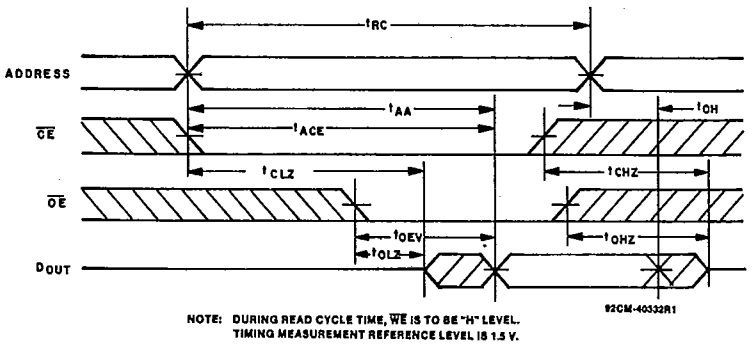
V_{DD}, V_{SS}:

Power supply connections.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55 to +125°C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 5 ns, Input Pulse Levels: 0 V to 3 V

CHARACTERISTIC		LIMITS				UNITS
		+25/-55°C		+125°C		
Read Cycle Times, See Fig. 2		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	100	—	120	—	ns
Address Access Time	t_{AA}	—	100	—	120	
Chip Enable Access Time	t_{ACE}	—	100	—	120	
Output Enable Access Time	t_{OEV}	—	50	—	60	
Chip Enable to Output Active	t_{CLZ}	10*	—	10*	—	
Chip Disable to Output "High Z"	t_{CHZ}	—	35*	—	40*	
Output Enable to Output Active	t_{OLZ}	5*	—	5*	—	
Output Disable to Output "High Z"	t_{OHZ}	—	35*	—	40*	
Output Hold from Address Change	t_{OH}	10*	—	10*	—	

* Guaranteed, not tested.



NOTE: DURING READ CYCLE TIME, $\overline{WE}$ IS TO BE "H" LEVEL.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

Fig. 2 - Read-cycle timing waveforms.

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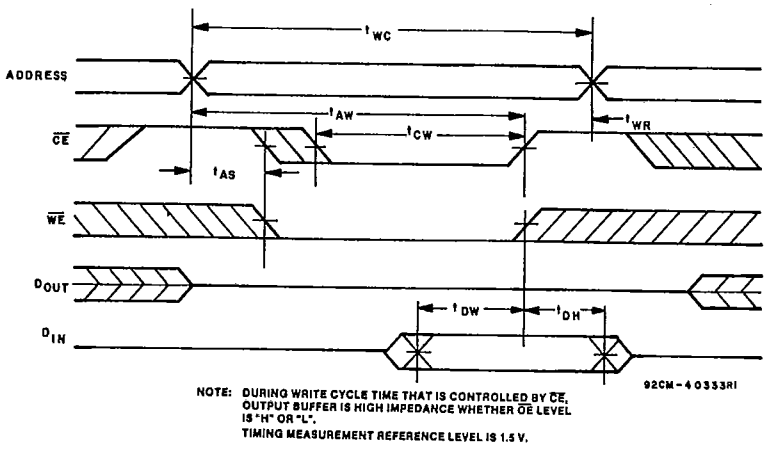
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -55 to +125°C, V_{DD} = 5 V ± 10%, Input t_r, $t_f \leq$ 10 ns; C_L = 50 pF, Input Pulse Levels: 0 V to 3 V

CHARACTERISTIC		LIMITS				UNITS
		+25°C/-55°C		+125°C		
Write Cycle Times, See Fig. 3 ($\overline{CE}$ and $\overline{WE}$ Control)		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	100	—	120	—	ns
Chip Enable to End of WRITE	t_{CW}	80	—	85	—	
Address Valid to End of WRITE	t_{AW}	80	—	85	—	
Address Setup Time	t_{AS}	0	—	0	—	
Write Pulse Width	t_{WP}	75	—	80	—	
Write Recovery Time	t_{WR}	0	—	0	—	
Input Data Set Time	t_{DW}	45	—	50	—	
Input Data Hold Time	t_{DH}	0	—	0	—	
Write to Output "High Z"	t_{WHZ}	—	35*	—	40*	
Output Active from End of WRITE	t_{OW}	10*	—	10*	—	

* Guaranteed, not tested.

WRITE CYCLE 1 ($\overline{CE}$ CONTROL)



NOTE: DURING WRITE CYCLE TIME THAT IS CONTROLLED BY $\overline{CE}$, OUTPUT BUFFER IS HIGH IMPEDANCE WHETHER $\overline{OE}$ LEVEL IS "H" OR "L".
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

Fig. 3 - Write-cycle timing waveforms.

WRITE CYCLE 2 ($\overline{WE}$ CONTROL)

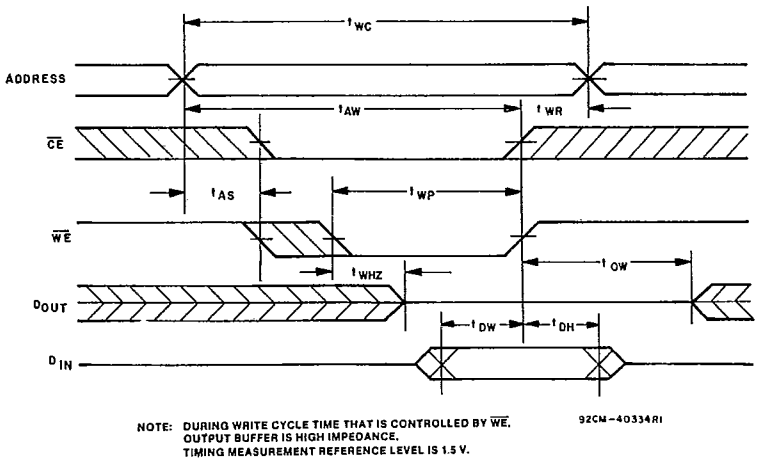


Fig. 3 - Write-cycle timing waveforms (continued).

DATA RETENTION CHARACTERISTICS at T_A = -55 to +125°C; See Fig. 4

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Data Retention Supply Voltage	V_{DDR}		2.5	5.5	V
Data Retention Current	I_{DDS2}	V_{DD} = 3 V, $\overline{CE} \geq V_{DD}$ -0.2 V	—	350	μA
Chip Select to Data Retention Time	t_{CDR}		0	—	ns
Operation Recovery Time	t_R*		t_{RC}*	—	

*t_{RC} = Read Cycle Time. Data Retention Time, t_{DR} = 500 ms.

DATA RETENTION TIMING WAVEFORMS

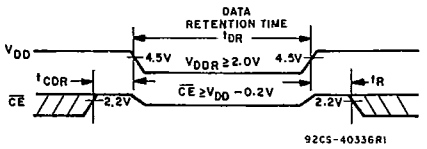
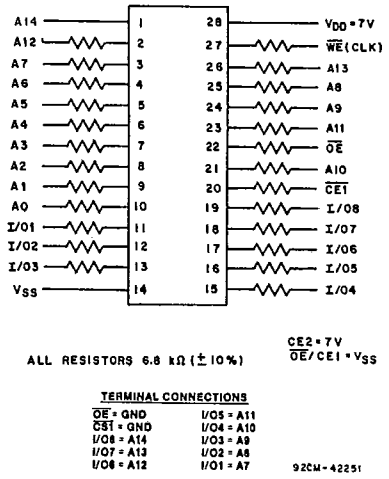
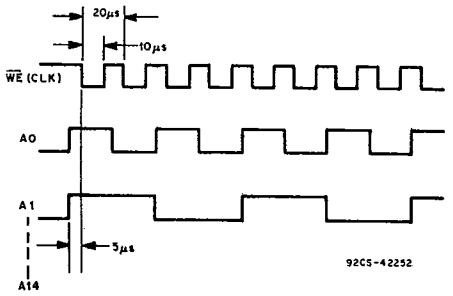


Fig. 4 - Low V_{DD} data-retention timing waveforms.



(a) Burn-in circuit for 28-lead package (D suffix).



(b) Burn-in circuits timing waveforms.

TYPE NO.	V_{DD}	TEMP.	TIME
CDM62256CD/3	7 V	+125°C	160 Hrs. Min.

Fig. 5 - Dynamic burn-in circuit and timing waveforms.