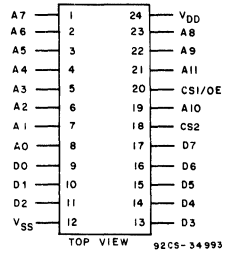
CDM5332, CDM5333



CDM5332
TERMINAL ASSIGNMENT

CMOS 4096-Word x 8-Bit Static Read-Only Memory

Features:

- *Low power replacement for NMOS ROMs*
- *Choice of two industry standard pinouts:*
  CDM5332 is pin compatible with INTEL 2732 and 2332A
  CDM5333 is pin compatible with Supertex CM3200, TI TMS 4732, Motorola MCM 68732 and MCM 68A332
- *Fast access time: 350 ns max.*
- *TTL input and output compatible*
- *Three state outputs*
- *Two programmable chip selects*

The RCA CDM5332 and CDM5333 are 32,768-bit mask-programmable CMOS Read-Only Memories organized as 4096 eight-bit words. They are designed to be used with a wide variety of general-purpose microprocessor systems, including RCA CDP1800- and CDP6805-series systems. Two inputs, CS1/OE and CS2, are provided for memory expansion and output buffer control. CS2 gates the address and output buffers and powers down the chip to the standby mode. CS1/OE controls the output buffers to eliminate bus contention. The active polarity for each chip select is user mask-programmable.

The CDM5332 and CDM5333 differ only in terminal assignments and are pin compatible with standard industry types. CDM5332 is pin compatible with Intel 2732 and 2332A. CDM5333 is pin compatible with Supertex CM3200, T.I. TMS4732, and Motorola MCM68732 and MCM68A332.

The CDM5332 and CDM5333 are supplied in 24-lead dual-in-line ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

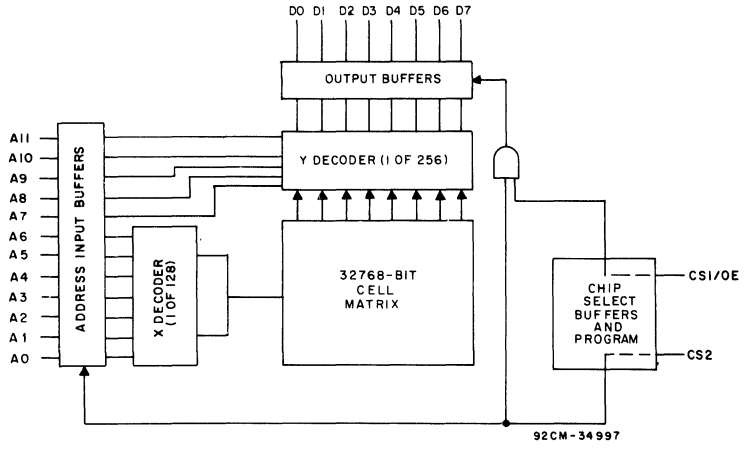
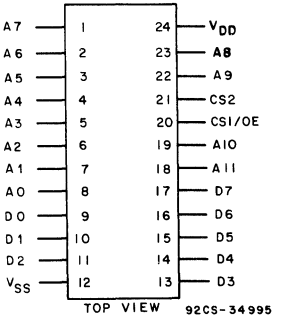


Fig. 1 - Functional block diagram.



CDM5333
TERMINAL ASSIGNMENT

6

File Number **1366**

CDM5332, CDM5333

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to VDD +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to 125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85° C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS		LIMITS ALL TYPES			UNITS
		Vo (V)	V_{IN} (V)	Min.	Typ.•	Max.	
Quiescent Device Current	I_{DD}Δ	—	0, V_{DD}	—	2	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, V_{DD}	2.4	4	—	mA
Output High Drive (Source) Current	I_{OH}	V_{DD} -0.4	0, V_{DD}	-1.2	-2	—	
Output Voltage Low-Level	V_{OL}	—	0, V_{DD}	—	0	0.1	V
Output Voltage High-Level	V_{OH}	—	0, V_{DD}	V_{DD} -0.1	V_{DD}	—	
Input Low Voltage	V_{IL}	0.5, V_{DD} -0.5	—	—	—	0.8	
Input High Voltage	V_{IH}	0.5, V_{DD} -0.5	—	2.4	—	—	
Input Leakage Current	I_{IN}	—	0, V_{DD}	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	0, V_{DD}	0, V_{DD}	—	—	±1	
Input Capacitance	C_{IN}	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	10	15	
Standby Device Current	I_{SBY}Δ	—	0.8 V,2.4 V	—	0.25	0.5	mA
Operating Device Current	I_{OPER}Δ	—	0.8 V,2.4 V	—	15	25	

ΔSee chart on page 3 for test conditions

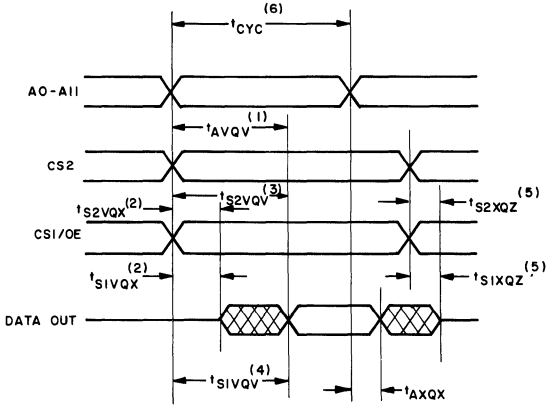
•Typical values are for T_A = 25° C and nominal V_{DD}.

ΔSTATIC CHARACTERISTIC Device Current Test Conditions:

CHARACTERISTIC	CHIP SELECT STATUS	ADDRESS INPUT TO TOGGLE FREQUENCY	OUTPUT LOADING
I_{DD} Quiescent Device Current	Any Chip Select Disabled	0	Open Circuit
I_{SBY} — Standby Device Current	CS2 Disabled at TTL Level	1 MHz	Open Circuit
I_{OPER} — Operating Device Current	CS2 Active CS1 Don't Care	1 MHz	Open Circuit

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Input t_r,t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V

CHARACTERISTIC		LIMITS		UNITS
		Min.	Max.	
Address Access Time	t_{AVQV}	—	350	ns
CS2 Enable to Output Active	t_{S2VQX}	10	—	
CS1/OE Enable to Output Active	t_{S1VQX}	0	—	
CS2 Enable Access	t_{S2VQV}	—	350	
CS1/OE Enable to Output Valid	t_{S1VQV}	—	150	
Data Hold After Address	t_{AXQX}	50	—	
CS2 Disable to Output High Z	t_{S2XQZ}	—	120	
CS1/OE Disable to Output High Z	t_{S1XQZ}	—	120	
Cycle Time	t_{CYC}	350	—	



NOTES:
(1) Assumes t_{S1VQV} and t_{S2VQV} are satisfied.
(2) Output Active requires both CS1/OE and CS2 Active.
(3) Assumes t_{AVQV} and t_{S1VQV} are satisfied.
(4) Assumes t_{AVQV} and t_{S2VQV} are satisfied.
(5) Either invalid CS1/OE or CS2 causes Output High Z.
(6) Generates 50-ns Valid Output Pulses (i.e., t_{CYC}-t_{AVQV}+t_{AXQX}).

NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

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Fig. 2 - Timing waveforms.

CDM5332, CDM5333

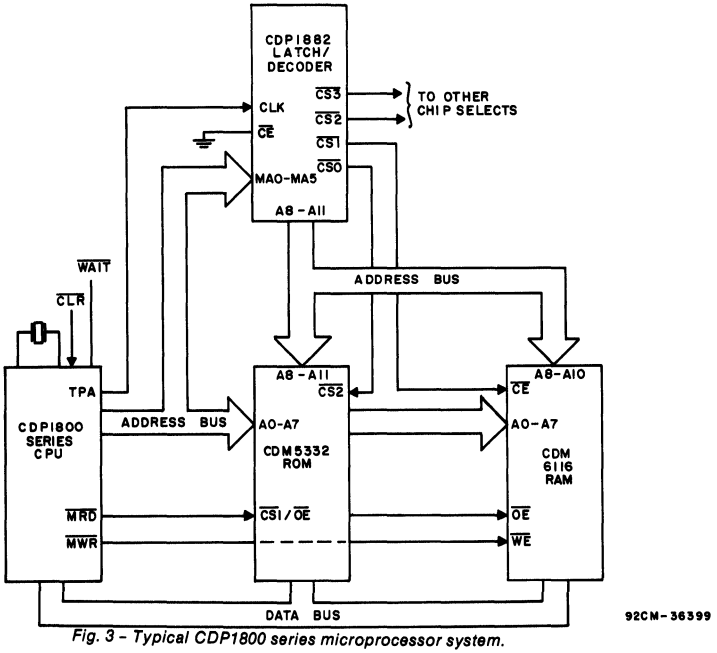

Fig. 3 - Typical CDP1800 series microprocessor system.