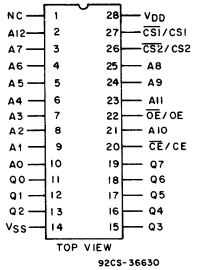
# CDM5365




**TERMINAL ASSIGNMENT**

# CMOS 8192-Word by 8-Bit LSI Static ROM

**Features:**

- *Asynchronous operation*
- *Fast access time - 250 ns max.*
- *Low standby and operating power - $I_{SBY2}$=2 μA typical $I_{OPER2}$=10 mA max. at $t_{cyc}$=1 μs; =30 mA max. at $t_{cyc}$=250 ns*
- *Automatic power-down*
- *Mask-programmable chip enable, chip selects, and output enable*
- *TTL input and output compatible*
- *28-pin JEDEC standard pin out: Pin compatible with the 2764 EPROM*

The RCA-CDM5365 is a 65,536-bit asynchronous mask-programmable CMOS READ-ONLY memory organized as 8192 eight-bit words. The CDM5365 is designed to be used with a wide range of general-purpose microprocessor systems, including the RCA CDP1800- and CDP6805-series systems. Two chip selects, one chip enable, and an output enable function are provided for memory expansion and output buffer control. The chip enable gates the address and output buffers and powers down the chip to the standby mode. The two chip selects and the output enable control only the output buffers. The polarities of the chip enable, chip selects, and the output enable are user mask-programmable.

The CDM5365 is supplied in 28-lead, hermetic, dual-in-line side-brazed ceramic (D suffix), and 28-lead dual-in-line plastic (E suffix) packages.

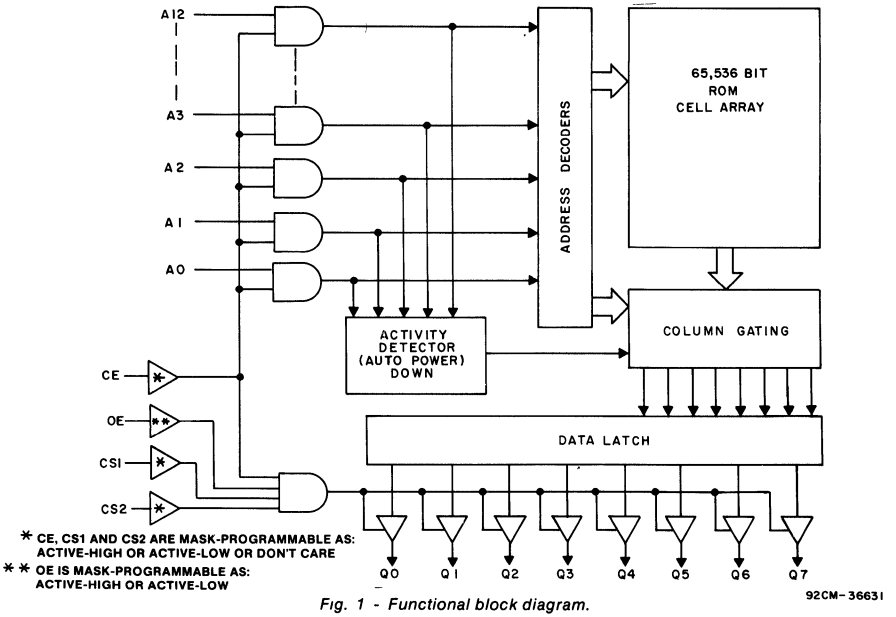



*Fig. 1 - Functional block diagram.*

File Number **1466**

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**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltage referenced to $V_{SS}$ terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to $V_{DD}$ +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A$ = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For $T_A$ = +100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 8 mW/°C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE-TEMPERATURE RANGE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C

**RECOMMENDED OPERATING CONDITIONS at $T_A$ = -40 to +85°C**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| DC Operating Voltage Range | 4 | 6 | V |
| Input Voltage Range | $V_{SS}$ | $V_{DD}$ | |

**STATIC ELECTRICAL CHARACTERISTICS at $T_A$ = -40 to +85°C, $V_{DD}$ = 5 V ± 10%, Except as noted**

| CHARACTERISTIC | | CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|
| | | | Min. | Typ.* | Max. | |
| Average Operating Device Current[a] | $I_{OPER1}$[d] | $V_{IN}$ = $V_{IL}$, $V_{IH}$; CE = $V_{IH}$; ($\overline{CE}$ = $V_{IL}$) $t_{cyc}$ = 1 µs | — | — | 15 | mA |
| | | $t_{cyc}$ = 250 ns | — | — | 35 | |
| | $I_{OPER2}$[e] | $V_{IN}$ = 0.2 V, $V_{DD}$ -0.2 V; CE = $V_{DD}$ -0.2 V; ($\overline{CE}$=0.2 V) $t_{cyc}$=1 µs | — | — | 10 | |
| | | $t_{cyc}$ = 250 ns | — | — | 30 | |
| DC Active Device Current[b] | $I_{ACT1}$[d] | $V_{IN}$=$V_{IL}$, $V_{IH}$; CE=$V_{IH}$; ($\overline{CE}$=$V_{IL}$) | — | — | 15 | mA |
| | $I_{ACT2}$[e] | $V_{IN}$=0.2 V, $V_{DD}$ -0.2 V; CE=$V_{DD}$ -0.2 V; ($\overline{CE}$=0.2 V) | — | — | 50 | µA |
| Standby Device Current[c] | $I_{SBY1}$[d] | $V_{IN}$=$V_{IL}$, $V_{IH}$; CE=$V_{IL}$; ($\overline{CE}$=$V_{IH}$) | — | — | 1.5 | mA |
| | $I_{SBY2}$[e] | $V_{IN}$=0.2 V, $V_{DD}$ -0.2 V; CE=0.2 V; ($\overline{CE}$=$V_{DD}$ -0.2 V) | — | 2 | 50 | µA |
| Output Voltage Low-Level | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | — | 0.4 | V |
| Output Voltage High-Level | $V_{OH}$ | $I_{OH}$ = -3.2 mA | 2.4 | — | — | |
| Input Low Voltage | $V_{IL}$ | — | — | — | 0.8 | |
| Input High Voltage | $V_{IH}$ | — | 2.2 | — | — | |
| Input Leakage Current (Any Input) | $I_{IN}$ | $V_{SS} \le V_{IN} \le V_{DD}$ | — | — | ±1 | µA |
| 3-State Output Leakage Current | $I_{OUT}$ | $V_{SS} \le V_{OUT} \le V_{DD}$ | — | — | ±1 | |
| Input Capacitance | $C_{IN}$ | f = 1 MHz, $T_A$ = 25°C | — | 5 | 10 | pF |
| Output Capacitance | $C_{OUT}$ | f = 1 MHz, $T_A$ = 25°C | — | 6 | 12 | |

*Typical values are for $T_A$=25°C and nominal $V_{DD}$.
[a]Address inputs toggling, chip enabled, outputs open circuit.
[b]Inputs stable, chip enabled, outputs open circuit.
[c]Independent of address input activity, chip disabled.
[d]TTL inputs.
[e]CMOS inputs.

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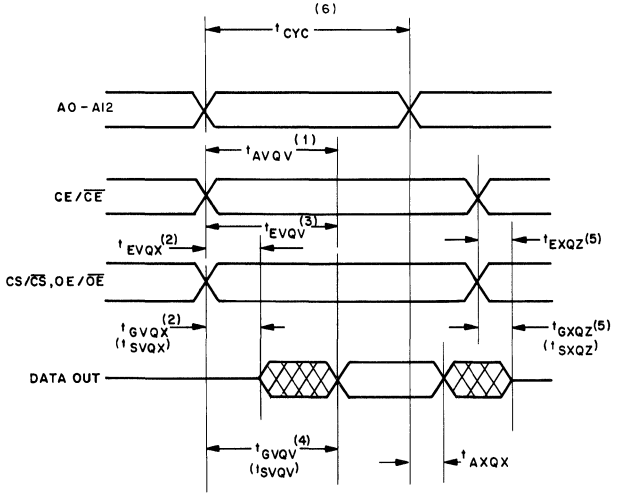
**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ = -40 to +85° C, $V_{DD}$ =5 V ± 10%, Input $t_r$, $t_f$ = 10 ns; $C_L$ = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V**

| CHARACTERISTIC | | LIMITS | | UNITS |
|---|---|---|---|---|
| | | Min. | Max. | |
| Address Access Time | $t_{AVQV}$ | — | 250 | ns |
| Chip Enable to Output Active | $t_{EVQX}$ | 0 | — | |
| Output Enable to Output Active | $t_{GVQX}$ | 0 | — | |
| Chip Select to Output Active | $t_{SVQX}$ | 0 | — | |
| Chip Enable Access | $t_{EVQV}$ | — | 250 | |
| Output Enable to Output Valid | $t_{GVQV}$ | — | 90 | |
| Chip Select to Output Valid | $t_{SVQV}$ | — | 90 | |
| Data Hold After Address | $t_{AXQX}$ | 10 | — | |
| Chip Disable to Output High Z | $t_{EXQZ}$ | — | 90 | |
| Output Disable to Output High Z | $t_{GXQZ}$ | — | 70 | |
| Chip Deselect to Output High Z | $t_{SXQZ}$ | — | 70 | |
| Cycle Time | $t_{CYC}$ | 250 | — | |




**NOTES:**
(1) **Assumes $t_{SVAV}$, $t_{GVAV}$, and $t_{EVAV}$ are satisfied**
(2) **Output Active requires Chip Enable, Output Enable and Chip Selects Active.**
(3) **Assumes $t_{AVAV}$, $t_{SVAV}$, and $t_{GVAV}$ are satisfied.**
(4) **Assumes $t_{AVAV}$ and $t_{EVAV}$ are satisfied.**
(5) **Either Invalid Chip Enable, Chip Select, or Output Enable causes Output High Z.**
(6) **Generates 10-ns Valid Output Pulses (i.e., $t_{CYC}$-$t_{AVQV}$+$t_{AXQX}$).**

**NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.**

*Fig. 2 - Timing waveforms.*

## APPLICATION INFORMATION

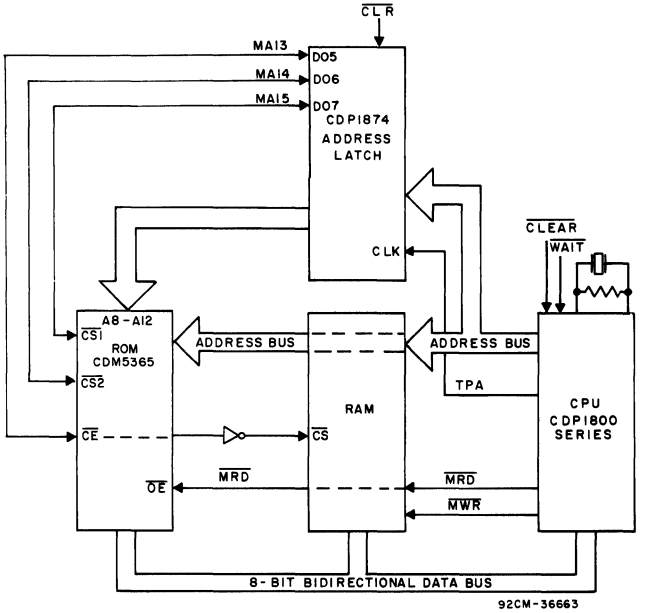



*Fig. 3 - Typical CDP1800 series microprocessor system.*

### Decoupling Capacitors

The CDM5365 operates with a low average dc power supply current that varies with cycle time. However, the CDM5365 is a large ROM with many internal nodes. Pre-charging of selected nodes during portions of the memory cycle results in short duration peak currents that can be much higher than the average dc value. The rise and fall times of the peak current pulses can have a value sufficient to generate unwanted system noise components. To minimize or eliminate the effects of the current spikes, a 0.1-$\mu$F ceramic decoupling capacitor is recommended between the $V_{DD}$ and $V_{SS}$ pins of every ROM device.

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