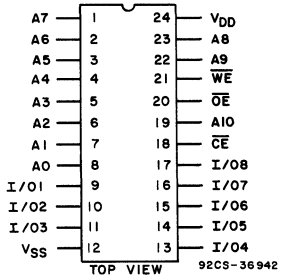
CDM6116A

Product Preview



TERMINAL ASSIGNMENT

CMOS 2048-Word by 8-Bit Static RAM

Features:

- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Industry standard 24-pin configuration*
- *Chip-enable gates address buffers for minimum standby current*
- *Data retention voltage: 2 V min.*

The RCA-CDM6116A is a CMOS 2048-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data inputs and data outputs and utilizes a single power supply of 4.5 V to 5.5 V. A chip-enable input and an output-enable input are provided for memory expansion and output buffer control.

The chip enable ($\overline{CE}$) gates the address and output buffers and powers down the chip to the low power standby mode.

The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM6116A-2 and CDM6116A-3 are supplied in a 24-lead dual-in-line plastic package (E suffix). The CDM-6116A-9 is supplied in a 24-lead dual-in-line plastic package (E suffix) and a 24-lead dual-in-line side-brazed ceramic package (D suffix).

	CDM6116A-2	CDM6116A-3	CDM6116A-9
Access Time (max.)	200 ns	150 ns	250 ns
Output Enable Time (max.)	120 ns	60 ns	150 ns
Operating Temperature	0° to +70° C		-40° to +85° C
Operating Current (max.)	35 mA	35 mA	40 mA
Standby Current I_{DDS1} (max.)	30 μA	50 μA	100 μA

OPERATING CONDITIONS at T_A = 0 to +70° C, (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9)
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES MIN.	LIMITS ALL TYPES MAX.	UNITS
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V_{IH}	2.2	V_{DD} + 0.3	V
	V_{IL}	-0.3	0.8	V
Input Signal Rise or Fall Time Δ	t_r, t_f	—	5	μs

Δ Input signal rise and fall times longer than the maximum value can cause loss of stored data in the selected mode.

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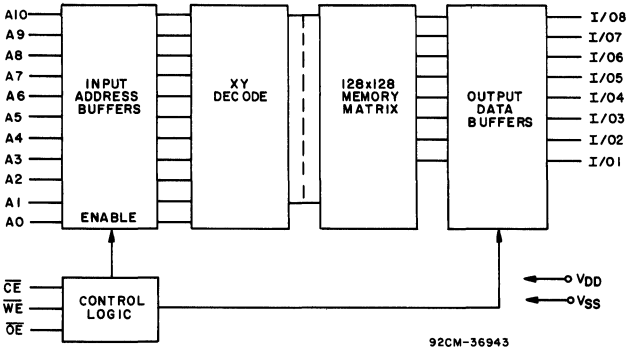

Fig. 1 - Functional block diagram.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 TO A10	MODE	I/01 TO I/08	DEVICE CURRENT
H	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	L	STABLE	WRITE	DATA IN	ACTIVE
L	L	L	STABLE	WRITE	DATA IN	ACTIVE

L = LOW H = HIGH X = H or L

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MAXIMUM RATINGS, *Absolute-Maximum Ratings*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(Voltage referenced to V_{SS} terminal) ..... -0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to +7 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40° to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60° to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40° to +85°C (PACKAGE TYPE D) ..... 500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
CDM6116A-2, CDM6116A-3 (PACKAGE TYPE E) ..... 0 to +70°C
CDM6116A-9 (PACKAGE TYPES D, E) ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

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STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9), V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS									UNITS
			CDM6116A-2			CDM6116A-3			CDM6116A-9			
			MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	
Standby Device Current	I_{DDS}	$\overline{CE}$ = V_{IH}	—	0.6	2	—	0.6	2	—	0.3	2	mA
	I_{DDS1}	$\overline{CE}$ = V_{DD}-0.2 V	—	1	30	—	1	50	—	1	100	μA
Output Voltage Low Level	V_{OL} Max.	I_{OL} = 2.1 mA	—	—	0.4	—	—	0.4	—	—	0.4	V
		I_{OL} = 1 μA	—	0.1	—	—	0.1	—	—	0.1	—	
Output Voltage High Level	V_{OH} Min.	I_{OH} = -1 mA	2.4	—	—	2.4	—	—	2.4	—	—	V
		I_{OH} = -1 μA	—	V_{DD}-0.1	—	—	V_{DD}-0.1	—	—	V_{DD}-0.1	—	
Input Leakage Current	I_{IN} Max.	V_{DD} = 5.5 V V_{IN} = 0 V to V_{DD}	—	±0.1	±2	—	±0.1	±2	—	±0.1	±2	μA
3-State Output Leakage Current	I_{OUT}	$\overline{CE}$ or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 V to V_{DD}	—	±0.5	±2	—	±0.5	±2	—	±0.5	±2	
Operating Device Current	I_{OPER}#	V_{IN} = V_{IL}, V_{IH}	—	20	35	—	20	35	—	28	40	mA
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25° C	—	4	6	—	4	6	—	4	6	pF
Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1 MHz, T_A = 25° C	—	6	8	—	6	8	—	6	8	

•Typical values are for T_A = 25° C and nominal V_{DD}.

#Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9), V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC		LIMITS						UNITS
		CDM6116A-2		CDM6116A-3		CDM6116A-9		
Read Cycle Times See Fig. 2		MIN.†	MAX.	MIN.†	MAX.	MIN.†	MAX.	
Read Cycle Time	t_{RC}	200	—	150	—	250	—	ns
Address Access Time	t_{AA}	—	200	—	150	—	250	
Chip Enable Access Time	t_{ACE}	—	200	—	150	—	250	
Chip Enable to Output Active	t_{CX}	15	—	15	—	15	—	
Output Enable to Output Valid	t_{OEV}	—	120	—	60	—	150	
Output Enable to Output Active	t_{OEX}	15	—	15	—	15	—	
Chip Disable to Output "High Z"	t_{CHZ}	0	60	0	50	0	80	
Output Disable to Output "High Z"	t_{OHZ}	0	60	0	50	0	80	
Output Hold from Address Change	t_{OH}	15	—	15	—	15	—	

†Time required by a limit device to allow for the indicated function.

SIGNAL DESCRIPTIONS

A0-A10 (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during read operations.

I/01-I/08: 8-bit tristate data bus.

$\overline{CE}$ (Chip Enable): Powers down chip, disables Read and Write functions, and gates off address inputs.

$\overline{OE}$ (Output Enable): Enables tristate outputs if $\overline{CE}$ is low and $\overline{WE}$ is high.

$\overline{WE}$ (Write Enable): Enables Write function, if $\overline{CE}$ is low. $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be tristated and a Write will occur).

V_{DD}, V_{SS}: Power supply connections.

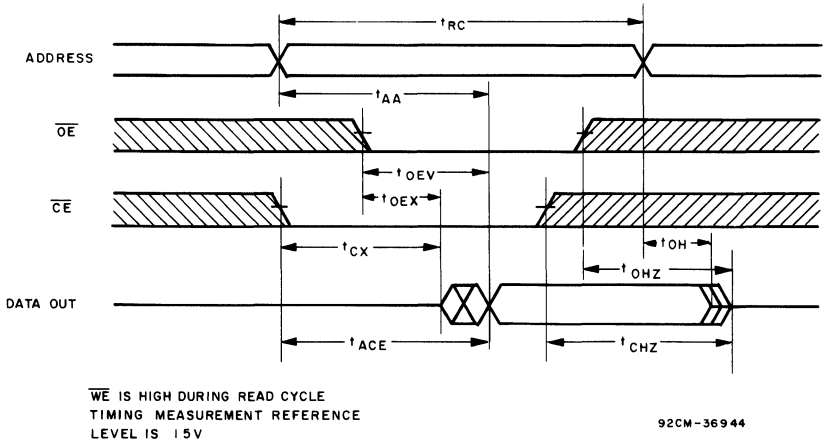

Fig. 2 - Read-cycle timing waveforms

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70° C (CDM6116A-2, CDM6116A-3); T_A = -40° to +85° C (CDM6116A-9), V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

CHARACTERISTIC		LIMITS						UNITS
		CDM6116A-2		CDM6116A-3		CDM6116A-9		
Write Cycle Times See Fig. 3		MIN.†	MAX.	MIN.†	MAX.	MIN.†	MAX.	
Write Cycle Time	t_{WC}	200	—	150	—	250	—	ns
Chip Enable to End of WRITE	t_{CW}	160	—	90	—	200	—	
Address Valid to End of WRITE	t_{AW}	160	—	90	—	200	—	
Address Setup Time	t_{AS}	0	—	0	—	0	—	
Write Pulse Width	t_{WP}	160	—	90	—	200	—	
Write Recovery Time	t_{WR}	10	—	0	—	10	—	
Output Disable to Output "High Z"	t_{OHZ}	0	60	0	50	0	80	
Write to Output "High Z"	t_{WHZ}	0	60	0	40	0	80	
Input Data Setup Time	t_{DW}	80	—	50	—	100	—	
Input Data Hold Time	t_{DH}	10	—	5	—	10	—	
Output Active from End of Write	t_{OW}	10	—	10	—	10	—	

†Time required by a limit device to allow for the indicated function.

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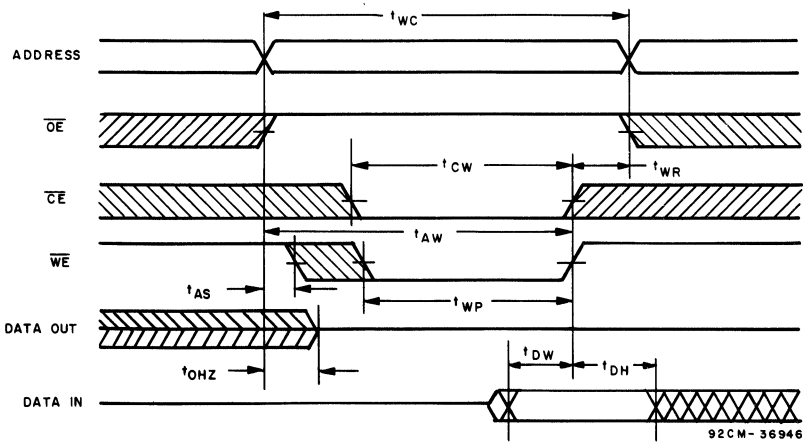
WRITE CYCLE 1



WRITE CYCLE 2 - $\overline{OE}$ = LOW

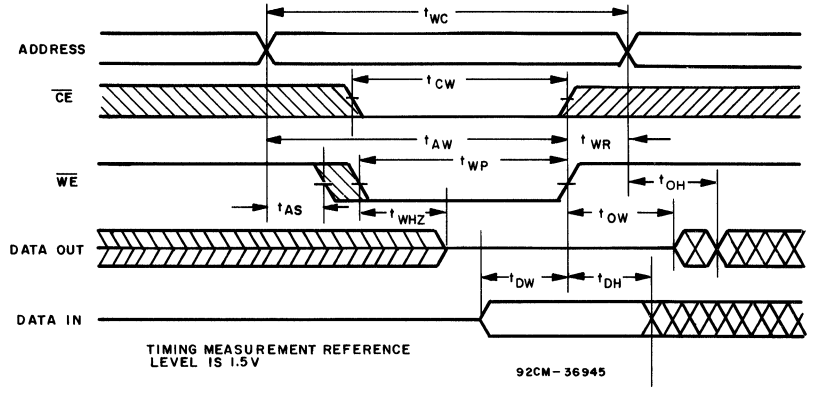


Fig. 3 - Write-cycle timing waveforms.

DATA RETENTION CHARACTERISTICS at T_A = 0 to 70° C (CDM6116A-2, CDM6116A-3); T_A = -40 to +85° C (CDM6116A-9), Unless otherwise noted, See Fig. 4.

CHARACTERISTIC		TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
Minimum Data Retention Voltage	V_{DR}				V
CDM6116A-2, CDM6116A-3		$\overline{CE} \geq V_{DD}$ - 0.2 V	2	—	
CDM6116A-9		T_A = -40 to 0° C	4.5	—	
		T_A = 0 to +85° C	2	—	
		$\overline{CE} \geq V_{DD}$ - 0.2 V			
Data Retention Quiescent Current	$I_{DD}DR$*				μA
CDM6116A-2		V_{DD} = 3 V, $\overline{CE} \geq$ 2.8 V	—	15	
CDM6116A-3		V_{DD} = 3 V, $\overline{CE} \geq$ 2.8 V	—	25	
CDM6116A-9		T_A = 0 to +85° C	—	50	
		V_{DD} = 3 V, $\overline{CE} \geq$ 2.8 V			
Chip Disable to Data Retention Time	t_{CDR}	See Fig. 4	0	—	ns
Recovery to Normal Operation Time	t_R	See Fig. 4	*t_{RC}	—	

*$I_{DD}DR$ = 7.5 μA max. at T_A = 0 to +40° C for CDM6116A-2 and CDM6116A-3.

*t_{RC} = Read Cycle Time.

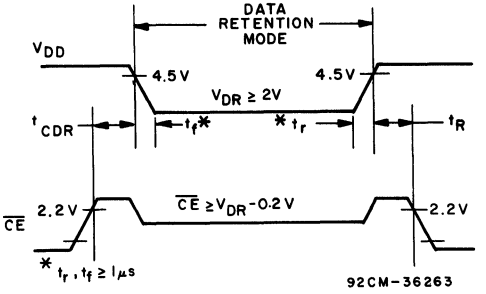


Fig. 4 - Low V_{DD} data retention timing waveforms.