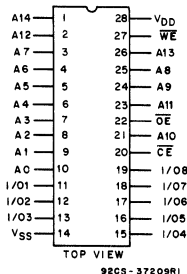


# CDM62256



### TERMINAL ASSIGNMENT

## CMOS 32,768-Word by 8-Bit LSI Static RAM

### Features:

- Fully static operation
- Single power supply: 4.5 V to 5.5 V
- All inputs and outputs directly TTL compatible
- Industry standard 28-pin configuration
- Input address buffers gated off with chip disable
- Low standby and operating power:  $I_{DDS1} = 2 \mu A$  typical,  $I_{DDA} = 70 mA$  maximum
- 3-state outputs
- Extended operating temperature range

The RCA-CDM62256 is a 32,768-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V. Chip Enable ( $\overline{CE}$ ) gates the address and output buffers and powers down the chip to the low power standby mode. The output enable ( $\overline{OE}$ ) controls the output buffers to eliminate bus contention.

The CDM62256-10 has an operating temperature range of 0° to +70° C. The CDM62256-10I and CDM62256-12I have an operating temperature range of -40° to +85° C.

The CDM62256 is supplied in 28-lead, hermetic, dual-in-line, side-brazed ceramic packages (D suffix), in 28-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

	CDM62256-10	CDM62256-10I	CDM62256-12I
Access Time (max.)	100 ns	100 ns	120 ns
Output Enable Time (max.)	50 ns	50 ns	60 ns
Operating Current (max.)	70 mA	70 mA	70 mA
Standby Current $I_{DDS1}$ (max.)	100 $\mu A$	200 $\mu A$	200 $\mu A$
Operating Temp. Range	0° to +70° C	-40° to +85° C	
Data Retention Voltage: 0° $\leq T_A \leq +70^\circ C$ 0° $\leq T_A \leq +85^\circ C$ -40° $\leq T_A < 0^\circ C$	2 V min. — —	— 2 V min. 4.5 V min.	— 2 V min. 4.5 V min.

**RECOMMENDED DC OPERATING CONDITIONS at  $T_A = 0$  to +70° C (CDM62256-10);  $T_A = -40^\circ$  to +85° C (CDM62256-10I, CDM62256-12I)** For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS			UNITS
		MIN.	TYP.	MAX.	
DC Operating Voltage Range	$V_{DD}$	4.5	5	5.5	V
Input Voltage Range	$V_{IH}$	2.2	3.5	$V_{DD} + 0.3$	
	$V_{IL}$	-0.3 $\Delta$	0	0.8	

$\Delta$  Min  $V_{IL} = -1.0 V$  for pulse width  $\leq 50 ns$

# CDM62256

## MAXIMUM RATINGS, Absolute-Maximum Values

- \* DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>): .....-0.5 to +7 V
- \* INPUT VOLTAGE RANGE, (V<sub>IN</sub>) ..... -0.5 \*\* to +7 V
- \* INPUT/OUTPUT VOLTAGE RANGE (V<sub>I/O</sub>) ..... -0.5 \*\* to V<sub>DD</sub> +0.3 V
- POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):
- For T<sub>A</sub> = -40° to +75° C (PACKAGE TYPE E) ..... 500 mW
- For T<sub>A</sub> = +75° to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 420 mW
- For T<sub>A</sub> = -40° to +85° C (PACKAGE TYPE D) ..... 500 mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- For T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
- OPERATING-TEMPERATURE RANGE (T<sub>A</sub>)
- CDM62256-10 (PACKAGE TYPES D AND E) ..... 0 to +70° C
- CDM62256-10I, 12I (PACKAGE TYPES D AND E) ..... -40° to +85° C
- STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -55° to +150° C
- LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265° C

\* (Voltage referenced to V<sub>SS</sub> terminal)  
 \*\* Min V<sub>IN</sub>, V<sub>I/O</sub> = -1 V for pulse width ≤ 50 ns

## TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	MODE	DEVICE CURRENT
H	X	X	X	Hi-Z	Standby	I <sub>DDS</sub>
L	X	L	Stable	D <sub>IN</sub>	Write	I <sub>DDA</sub>
L	L	H	Stable	D <sub>OUT</sub>	Read	I <sub>DDA</sub>
L	H	H	Stable	Hi-Z	Output disable	I <sub>DDA</sub>

L = Low, H = High, X = H or L

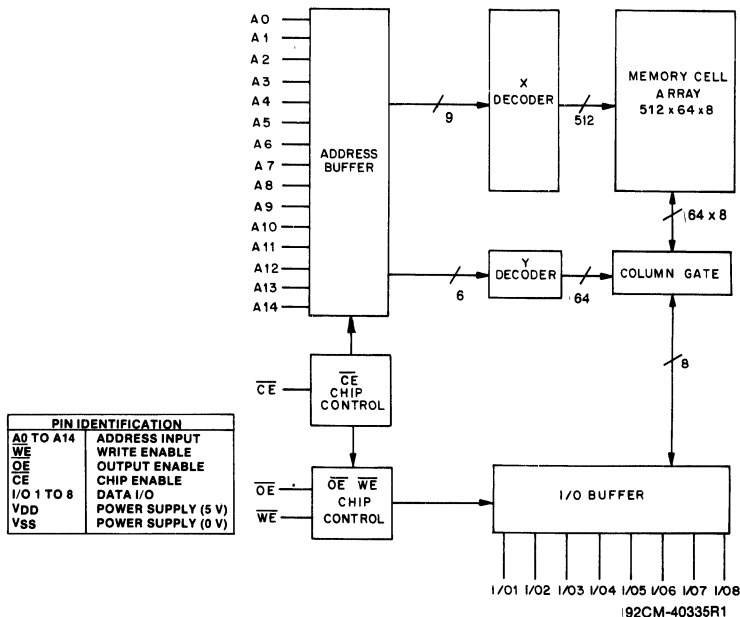


Fig. 1 - Functional block diagram.

# CDM62256

**ELECTRICAL CHARACTERISTICS** at  $T_A = 0^\circ$  to  $+70^\circ$  C (CDM62256-10);  $T_A = -40^\circ$  to  $+85^\circ$  C (CDM62256-10I, CDM62256-12I);  $V_{DD} = 5\text{ V} \pm 10\%$ , except as noted.

## DC Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS	
		CDM62256-10			CDM62256-10I			CDM62256-12I				
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.		
Input Leakage	$I_{LI}$	$V_i = 0$ to $V_{DD}$	-1	—	1	-1	—	1	-1	—	1	$\mu\text{A}$
Standby Supply	$I_{DDs}$	$\overline{CE} = V_{IH}$	—	1.5	3.0	—	1.5	3.0	—	1.5	3.0	mA
Current	$I_{DDs1}$	$\overline{CE} \geq V_{DD}-0.2\text{ V}$	—	2	100	—	2	200	—	2	200	$\mu\text{A}$
Average Operating	$I_{DDA}$	$V_i = V_{IL}, V_{IH}$ $I_{iO} = 0\text{ mA}$ $t_{cyc} = \text{Min}$	—	40	70	—	40	70	—	37	70	mA
Operating Supply	$I_{DDO}$	$V_i = V_{IL}, V_{IH}$ $I_{iO} = 0\text{ mA}$	—	35	65	—	35	65	—	35	65	mA
Output Leakage	$I_{LO}$	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{iO} = 0$ to $V_{DD}$	-1	—	1	-1	—	1	-1	—	1	$\mu\text{A}$
High Level Output	$V_{OH}$	$I_{OH} = -1.0\text{ mA}$	2.4	$V_{DD}-0.1$	—	2.4	$V_{DD}-0.1$	—	2.4	$V_{DD}-0.1$	—	V
Low Level Output	$V_{OL}$	$I_{OL} = 2.1\text{ mA}$	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	V

\* Typical values are measured at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 5.0\text{ V}$

## Terminal Capacitance ( $f = 1\text{ MHz}$ , $T_A = 25^\circ\text{C}$ )

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		MIN.	TYP.	MAX.		
Address Capacitance	$C_{ADD}$	$V_{ADD} = 0\text{ V}$	—	—	10	pF
Input Capacitance	$C_i$	$V_i = 0\text{ V}$	—	—	10	pF
I/O Terminal Capacitance	$C_{iO}$	$V_{iO} = 0\text{ V}$	—	—	10	pF

## SIGNAL DESCRIPTIONS

**A0-A14** (Address Inputs): These inputs must be stable prior to a write operation, but may change asynchronously during read operations.

**I/01-I/08**: 8-bit 3-state data bus.

**$\overline{CE}$**  (Chip Enable): Powers down chip, disables Read and Write functions, and gates off address inputs.

**$\overline{OE}$**  (Output Enable): Enables 3-state outputs if  $\overline{CE}$  is low and  $\overline{WE}$  is high.

**$\overline{WE}$**  (Write Enable): Enables Write function, if  $\overline{CE}$  is low  $\overline{WE}$  will dominate if both  $\overline{WE}$  and  $\overline{OE}$  are low (i.e., the bus will be 3-stated and a Write will occur).

**$V_{DD}$ ,  $V_{SS}$** : Power supply connections.

# CDM62256

AC ELECTRICAL CHARACTERISTICS at  $T_A = 0^\circ$  to  $+70^\circ$  C (CDM62256-10);  $T_A = -40^\circ$  to  $+85^\circ$  C (CDM62256-10I, CDM62256-12I);  $V_{DD} = 5\text{ V} \pm 10\%$

### Read Cycle

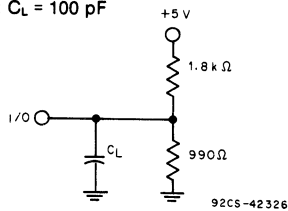
CHARACTERISTIC	A.C. TEST CONDITIONS	LIMITS				UNITS
		CDM62256-10 CDM62256-10I		CDM62256-12I		
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time $t_{RC}$	1	100	—	120	—	ns
Address Access Time $t_{AA}$		—	100	—	120	
Chip Enable Access Time $t_{ACE}$		—	100	—	120	
Output Enable Access Time $t_{OEV}$		—	50	—	60	
Chip Enable to Output Active $t_{CLZ}$	2	10	—	10	—	
Chip Disable to Output 'High Z' $t_{CHZ}$		—	35	—	40	
Output Enable to Output Active $t_{OLZ}$		5	—	5	—	
Output Disable to Output 'High Z' $t_{OHZ}$		—	35	—	40	
Output Hold From Address Change $t_{OH}$	1	10	—	10	—	

### Write Cycle

CHARACTERISTIC	A.C. TEST CONDITIONS	LIMITS				UNITS
		CDM62256-10 CDM62256-10I		CDM62256-12I		
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time $t_{WC}$	1	100	—	120	—	ns
Chip Enable to End of Write $t_{CW}$		80	—	85	—	
Address Valid to End of Write $t_{AW}$		80	—	85	—	
Address Setup Time $t_{AS}$		0	—	0	—	
Write Pulse Width $t_{WP}$		75	—	80	—	
Write Recovery Time $t_{WR}$		0	—	0	—	
Input Data Set Time $t_{DW}$		45	—	50	—	
Input Data Hold Time $t_{DH}$		0	—	0	—	
Write to Output 'High Z' $t_{WHZ}$		2	—	35	—	
Output Active From End of Write $t_{OW}$	10		—	10	—	

#### Test Condition: 1

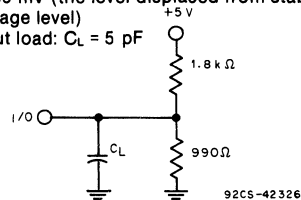
- Input pulse level: 0.6 V to 2.4 V
- $t_r, t_f = 5\text{ ns}$
- Input and output timing reference levels: 1.5 V
- Output load:  $C_L = 100\text{ pF}$



$C_L = 100\text{ pF}$  (Includes Jig Capacitance)

#### Test Condition: 2

- Input pulse level: 0.6 V to 2.4 V
- $t_r, t_f = 5\text{ ns}$
- Input timing reference levels: 1.5 V
- Output timing reference levels:  $\pm 200\text{ mV}$  (the level displaced from stable output voltage level)
- Output load:  $C_L = 5\text{ pF}$



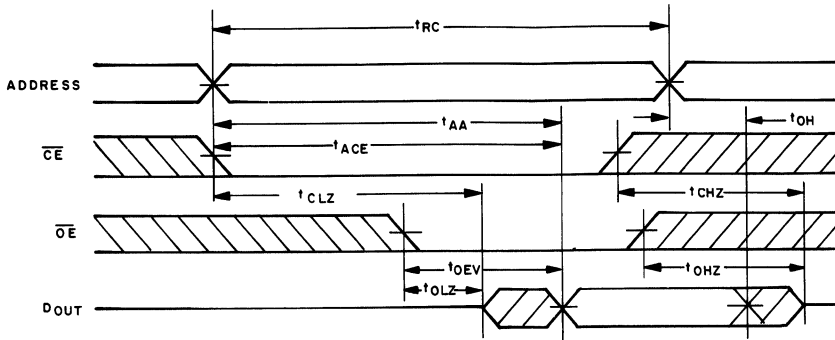
$C_L = 5\text{ pF}$  (Includes Jig Capacitance)

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# CDM62256

## TIMING CHARTS

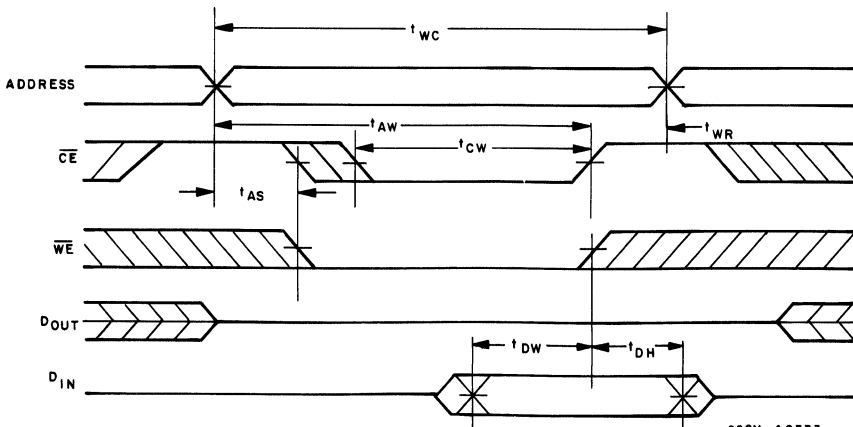
### Read Cycle



NOTE: DURING READ CYCLE TIME,  $\overline{WE}$  IS TO BE "H" LEVEL.

92CM-40332

### Write Cycle 1 ( $\overline{CE}$ Control)

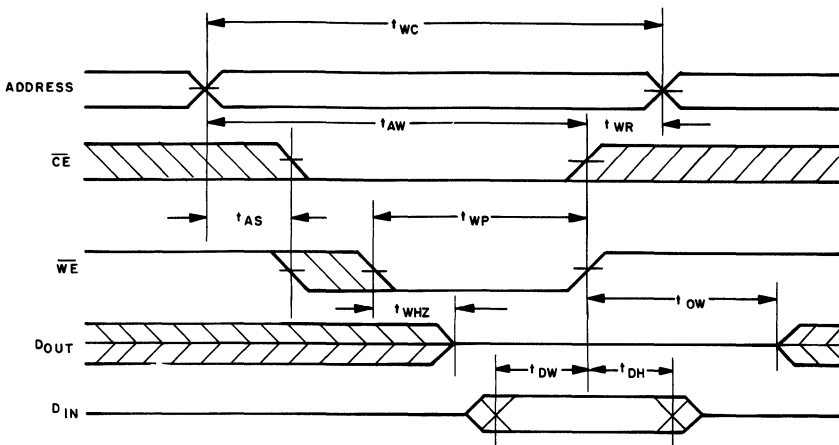


NOTE: DURING WRITE CYCLE TIME THAT IS CONTROLLED BY  $\overline{CE}$ , OUTPUT BUFFER IS HIGH IMPEDANCE WHETHER  $\overline{OE}$  LEVEL IS "H" OR "L".

92CM-40333

TIMING CHARTS (Continued)

Write Cycle 2 ( $\overline{WE}$  Control)



NOTE: DURING WRITE CYCLE TIME THAT IS CONTROLLED BY  $\overline{WE}$ , OUTPUT BUFFER IS HIGH IMPEDANCE.

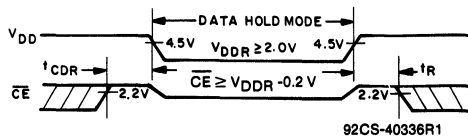
92CM-40334

DATA RETENTION CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		CDM62256-10		CDM62256-101 CDM62256-121		
		MIN.	MAX.	MIN.	MAX.	
Minimum Data Retention Voltage	$V_{DR}$ $\overline{CE} \geq V_{DD}-0.2 V$ , $0^\circ C \leq T_A \leq +70^\circ C$ $0^\circ C \leq T_A \leq +85^\circ C$ $-40^\circ C \leq T_A < 0^\circ C$	2	—	—	—	V
Data Retention Quiescent Current	$I_{DDDR}$ $\overline{CE} \geq V_{DD}-0.2 V$ , $V_{DD}=3 V, 0^\circ C \leq T_A \leq +70^\circ C$ $V_{DD}=3 V, 0^\circ C \leq T_A \leq +85^\circ C$ $V_{DD}=4.5 V, -40^\circ C \leq T_A < 0^\circ C$	—	50	—	—	$\mu A$
Chip Disable to Data Retention Time	$t_{CDR}$	0	—	0	—	ns
Recovery to Normal Operation Time	$t_R$	* $t_{RC}$	—	* $t_{RC}$	—	ns

\* $t_{RC}$  = Read Cycle Time.

DATA RETENTION TIMING



92CS-40336R1