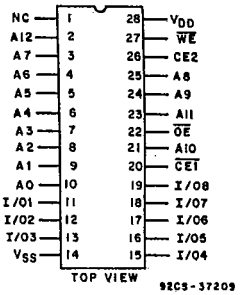
# CDM6264




TERMINAL ASSIGNMENT

# CMOS 8192-Word by 8-Bit LSI Static RAM

**Features:**

- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *Industry standard 28-pin configuration*
- *Input address buffers gated off with chip disable*
- *3-state outputs*

The RCA-CDM6264 is a 8192-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

Either chip enable ($\overline{CE1}$ or CE2), when not valid, will gate off the address and output buffers and power down the chip to minimum standby power with inputs toggling. The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM6264 is supplied in a 28-lead dual-in-line plastic (E suffix) package.

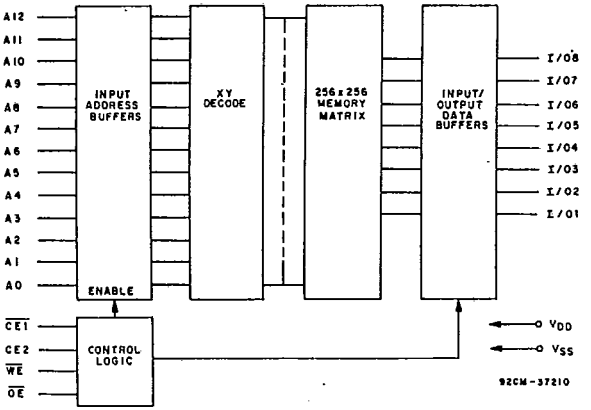



*Fig. 1 - Functional block diagram.*

| | CDM6264-3 | CDM6264-2I |
|---|---|---|
| Access Time (max.) | 150 ns | 200 ns |
| Output Enable Time (max.) | 70 ns | 70 ns |
| Operating Current (max.) | 45 mA | 45 mA |
| Standby Current $I_{DDS1}$ (max.) | 100 $\mu$A | 200 $\mu$A |
| Operating Temp. Range: | 0°C to +70°C | -40°C to +85°C |
| Data Retention Voltage: | | |
| $0°C \leq T_A \leq +70°C$ | 2 V min. | — |
| $0°C \leq T_A \leq +85°C$ | — | 2 V min. |
| $-40°C \leq T_A < 0°C$ | — | 4 V min. |

TRUTH TABLE

| $\overline{CE1}$ | CE2 | $\overline{OE}$ | $\overline{WE}$ | A0 TO A12 | MODE | DATA I/O | DEVICE CURRENT |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | NOT SELECTED | HIGH Z | STANDBY |
| X | L | X | X | X | NOT SELECTED | HIGH Z | STANDBY |
| L | H | L | H | STABLE | READ | DATA OUT | ACTIVE |
| L | H | X | L | STABLE | WRITE | DATA IN | ACTIVE |
| L | H | H | H | STABLE | OUTPUT DISABLE | HIGH Z | ACTIVE |

L = LOW H = HIGH X = H OR L

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$):
(Voltage referenced to $V_{SS}$ terminal) ..... -0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to +7 V
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -40° to +60°C ..... 500 mW
For $T_A$ = +60° to +85°C ..... Derate linearly at 8 mW/°C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For $T_A$ = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE ($T_A$):
CDM6264-3 ..... 0° to +70°C
CDM6264-2I ..... -40° to +85°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

**OPERATING CONDITIONS at $T_A$ = 0° to +70°C (CDM6264-3); $T_A$ = -40° to +85°C (CDM6264-2I)**
**For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | | LIMITS ALL TYPES MIN. | LIMITS ALL TYPES MAX. | UNITS |
|---|---|---|---|---|
| DC Operating Voltage Range | | 4.5 | 5.5 | V |
| Input Voltage Range | $V_{IH}$ | 2.2 | $V_{DD}$ + 0.3 | |
| | $V_{IL}$ | -0.3 | 0.8 | |
| Input Signal Rise or Fall Time△ | $t_r, t_f$ | — | 5 | μs |

△Input signal rise and fall times with a duration greater than the maximum value can cause loss of stored data in the selected mode.

**STATIC ELECTRICAL CHARACTERISTICS at $T_A$ = 0° to +70°C (CDM6264-3); $T_A$ = -40° to +85°C (CDM6264-2I), $V_{DD}$ = 5 V ± 10%, Except as noted**

| CHARACTERISTIC | | CONDITIONS | LIMITS CDM6264-3 Min. | CDM6264-3 Typ.* | CDM6264-3 Max. | CDM6264-2I Min. | CDM6264-2I Typ.* | CDM6264-2I Max. | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Standby Device Current | $I_{DDS}$ | $\overline{CE1}$=$V_{IH}$ or CE2=$V_{IL}$ | — | 1.5 | 3 | — | 2 | 4 | mA |
| | $I_{DDS1}$ | $\overline{CE1}$=CE2 ≥ $V_{DD}$-0.2 V or CE2 ≤ 0.2 V | — | 5 | 100 | — | 10 | 200 | μA |
| Output Voltage Low Level | $V_{OL}$ Max. | $I_{OL}$=2.1 mA | — | — | 0.4 | — | — | 0.4 | V |
| | | $I_{OL}$=1 μA | — | 0.1 | — | — | 0.1 | — | |
| Output Voltage High Level | $V_{OH}$ Min. | $I_{OH}$=-1 mA | 2.4 | — | — | 2.4 | — | — | |
| | | $I_{OH}$=-1 μA | — | $V_{DD}$-0.1 | — | — | $V_{DD}$-0.1 | — | |
| Input Leakage Current | $I_{IN}$ Max. | $V_{IN}$=0 V to $V_{DD}$ | — | ±0.1 | ±2 | — | ±0.1 | ±2 | μA |
| 3-State Output Leakage Current | $I_{OUT}$ | $V_{I/O}$=0 V to $V_{DD}$ | — | ±0.5 | ±2 | — | ±0.5 | ±2 | |
| Operating Device Current | $I_{OPER1}$# | $V_{IN}$=$V_{IL}$, $V_{IH}$ $t_{cyc}$=1 μs | — | 4.5 | 9 | — | 7.5 | 15 | mA |
| | | $t_{cyc}$=min. cycle time | — | 22.5 | 45 | — | 22.5 | 45 | |
| | $I_{OPER2}$# | $V_{IN}$=0.2 V, $V_{DD}$-0.2 V $t_{cyc}$=1 μs | — | 2 | 4 | — | 5 | 10 | |
| | | $t_{cyc}$=min. cycle time | — | 20 | 40 | — | 20 | 40 | |
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0 V, f=1 MHz, $T_A$=25°C | — | 4 | 6 | — | 4 | 6 | pF |
| Output Capacitance | $C_{I/O}$ | $V_{I/O}$=0 V, f=1 MHz, $T_A$=25°C | — | 6 | 8 | — | 6 | 8 | |

*Typical values are for $T_A$=25°C and nominal $V_{DD}$.
#Outputs open circuited.

## SIGNAL DESCRIPTIONS

**A0-A12 (Address Inputs):** These inputs must be stable prior to a write operation, but may change asynchronously during read functions.

**I/01-I/08:** 8-bit tristate data bus.

**$\overline{CE1}$, CE2 (Chip Enable):** Either chip enable, when not true, powers down the chip, disables Read and Write functions, and gates off address and output buffers.

**$\overline{OE}$ (Output Enable):** Enables tristate outputs if $\overline{CE1}$ and CE2 are valid and $\overline{WE}$ is high.

**$\overline{WE}$ (Write Enable):** Enables Write function, if $\overline{CE1}$ and CE2 are valid. $\overline{WE}$ will dominate if both $\overline{WE}$ and $\overline{OE}$ are low (i.e., the bus will be tristated and a Write will occur).

**$V_{DD}$, $V_{SS}$:** Power supply connections.

## DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ = 0° to +70° C (CDM6264-3); $T_A$ = -40° to +85° C (CDM6264-2I), $V_{DD}$ = 5 V ± 10%, Input $t_r$, $t_f$ = 10 ns; $C_L$ = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V

| CHARACTERISTIC | | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|
| | | CDM6264-3 | | CDM6264-2I | | |
| **Read Cycle Times, See Fig. 2** | | MIN.† | MAX. | MIN.† | MAX. | |
| Read Cycle Time | $t_{RC}$ | 150 | — | 200 | — | ns |
| Address Access Time | $t_{AA}$ | — | 150 | — | 200 | |
| Chip Enable Access Time | $t_{ACE1}$, $t_{ACE2}$ | — | 150 | — | 200 | |
| Chip Enable to Output Active | $t_{CLZ1}$, $t_{CLZ2}$ | 10 | — | 10 | — | |
| Output Enable to Output Valid | $t_{OEV}$ | — | 70 | — | 70 | |
| Output Enable to Output Active | $t_{OEX}$ | 5 | — | 5 | — | |
| Chip Disable to Output "High Z" | $t_{CHZ1}$, $t_{CHZ2}$ | 0 | 70 | 0 | 70 | |
| Output Disable to Output "High Z" | $t_{OHZ}$ | 0 | 60 | 0 | 60 | |
| Output Hold from Address Change | $t_{OH}$ | 30 | — | 30 | — | |

† Time required by a limit device to allow for the indicated function.

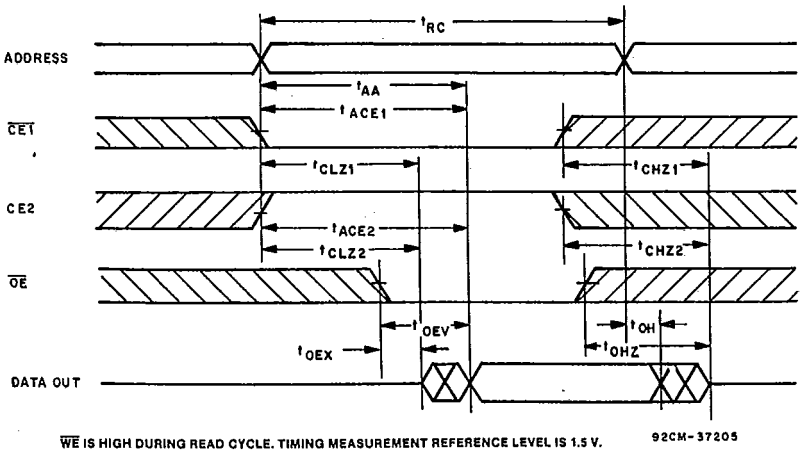



*Fig. 2 - Read-cycle timing waveforms.*

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ = 0° to +70°C (CDM6264-3); $T_A$ = -40° to +85°C (CDM6264-2I), $V_{DD}$ = 5 V ± 10%, Input $t_r$, $t_f$ = 10 ns; $C_L$ = 100 pF and 1 TTL Load, Input Pulse Levels: 0.8 V to 2.4 V**

| CHARACTERISTIC | | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|
| | | CDM6264-3 | | CDM6264-2I | | |
| **Write Cycle Times, See Fig. 3** | | MIN.† | MAX. | MIN.† | MAX. | |
| Write Cycle Time | $t_{WC}$ | 150 | — | 200 | — | ns |
| Chip Enable to End of WRITE | $t_{CW1}$, $t_{CW2}$ | 120 | — | 170 | — | |
| Address Valid to End of WRITE | $t_{AW}$ | 120 | — | 170 | — | |
| Address Setup Time | $t_{AS}$ | 0 | — | 0 | — | |
| Write Enable Width | $t_{WW}$ | 100 | — | 120 | — | |
| Write Recovery Time | $t_{WR}$ | 0 | — | 0 | — | |
| Write to Output "High Z" | $t_{WHZ}$ | — | 70 | — | 80 | |
| Input Data Setup Time | $t_{DW}$ | 60 | — | 80 | — | |
| Input Data Hold Time | $t_{DH}$ | 0 | — | 0 | — | |
| Output Active from End of Write | $t_{OW}$ | 10 | — | 10 | — | |

†Time required by a limit device to allow for the indicated function.

**WRITE CYCLE 1 ($\overline{CE1}$ CONTROL)**

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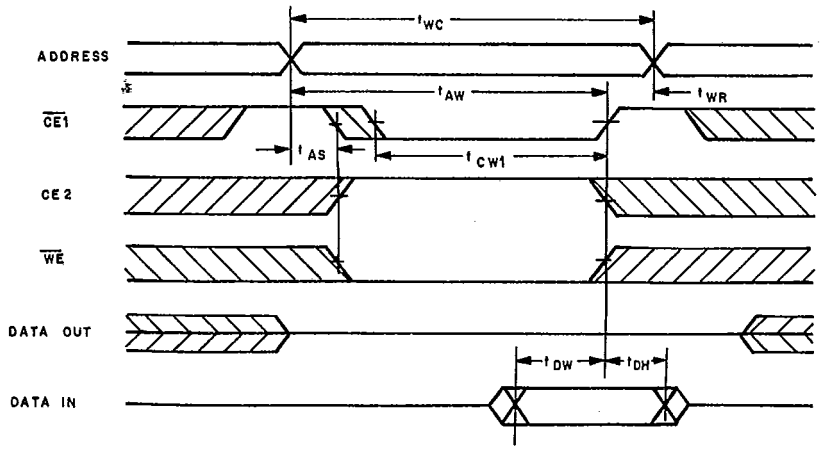
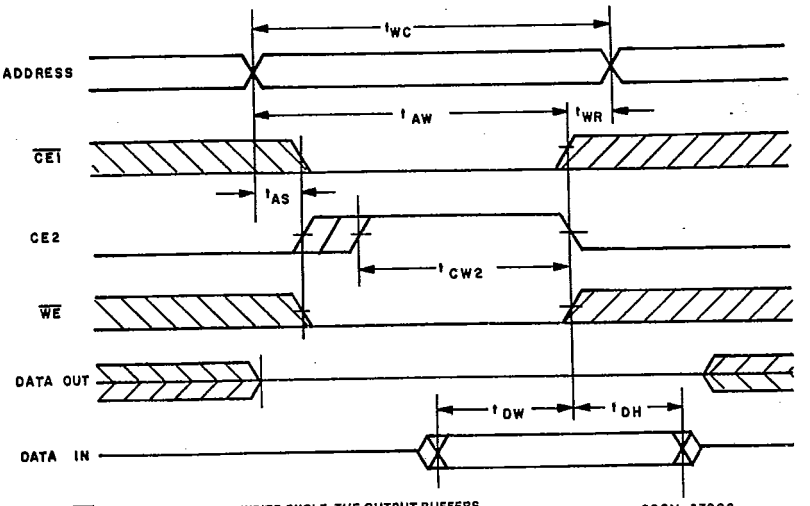


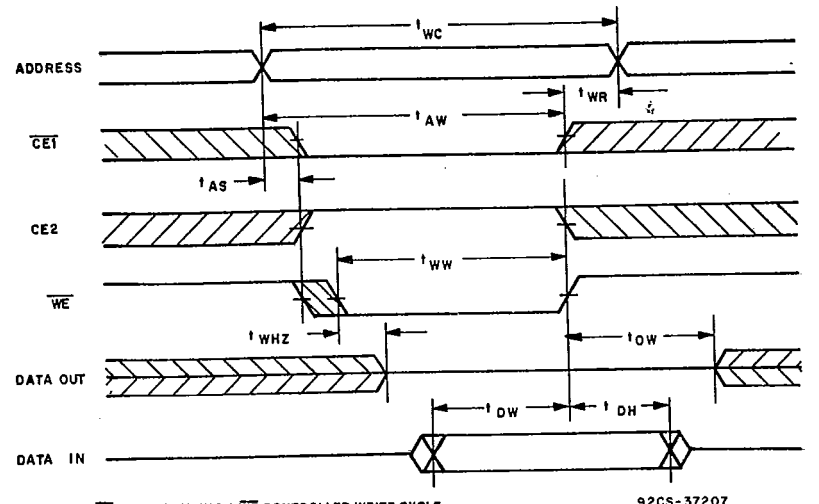

*Fig. 3 - Write-cycle timing waveforms.*

## WRITE CYCLE 2 (CE2 CONTROL)




IN A $\overline{CE1}$ OR CE2 CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE, WHETHER $\overline{OE}$ IS HIGH OR LOW.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

## WRITE CYCLE 3 ($\overline{WE}$ CONTROL)




IF $\overline{OE}$ IS HIGH DURING A $\overline{WE}$ CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE IN THIS PERIOD.
TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

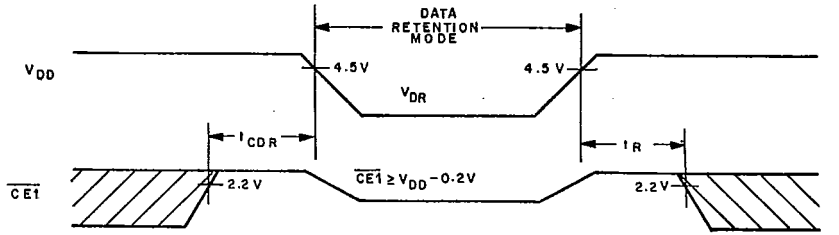
*Fig. 3 - Write-cycle timing waveforms (cont'd).*

**DATA RETENTION CHARACTERISTICS, See Fig. 4.**

| CHARACTERISTIC | | TEST CONDITIONS | LIMITS | | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | CDM6264-3 | | CDM6264-2I | | |
| | | | Min. | Max. | Min. | Max. | |
| Minimum Data Retention Voltage | $V_{DR}$ | $\overline{CE1} \geq V_{DD}-0.2$ V, or CE2 $\leq$ 0.2 V: | | | | | |
| | | 0°C $\leq T_A \leq$ +70°C | 2 | — | — | — | V |
| | | 0°C $\leq T_A \leq$ +85°C | — | — | 2 | — | |
| | | -40°C $\leq T_A <$ 0°C | — | — | 4 | — | |
| Data Retention Quiescent Current | $I_{DD}DR$ | $\overline{CE1}$, CE2 $\geq V_{DD}-0.2$ V, or CE2 $\leq$ 0.2 V: | | | | | |
| | | $V_{DD}$ = 3 V, 0°C $\leq T_A \leq$ +70°C | — | 50 | — | — | |
| | | $V_{DD}$ = 3 V, 0°C $\leq T_A \leq$ +85°C | — | — | — | 100 | μA |
| | | $V_{DD}$ = 4 V, -40°C $\leq T_A <$ 0°C | — | — | — | 100 | |
| Chip Disable to Data Retention Time | $t_{CDR}$ | See Fig. 4 | 0 | — | 0 | — | ns |
| Recovery to Normal Operation Time | $t_R$ | See Fig. 4 | *$t_{RC}$ | — | *$t_{RC}$ | — | |

*$t_{RC}$ = Read Cycle Time.

**DATA RETENTION WAVEFORM 1 ($\overline{CE1}$ CONTROL)**




**DATA RETENTION WAVEFORM 2 (CE2 CONTROL)**

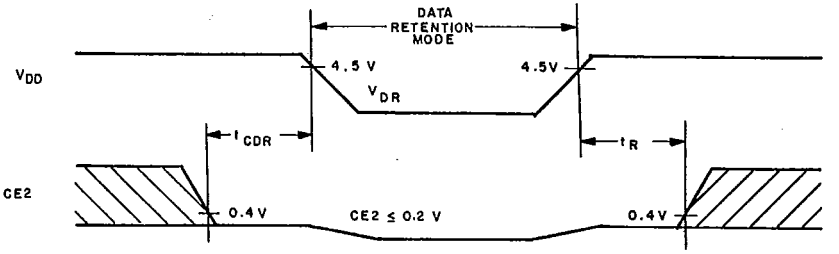



*Fig. 4 - Low $V_{DD}$ data-retention timing waveforms.* 92CM-37208