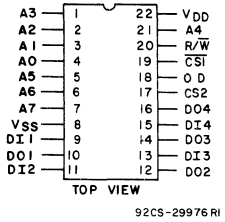
CDP1822, CDP1822C



CDP1822, CDP1822C TERMINAL ASSIGNMENTS

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- *Low operating current-8 mA at V_{DD}=5 V and cycle time=1 μs*
- *Industry standard pinout*
- *Two Chip-Select inputs-simple memory expansion*
- *Memory retention for standby battery voltage of 2 V min.*
- *Output-Disable for common I/O systems*
- *3-state data output for bus-oriented systems*
- *Separate data inputs and outputs*

The RCA-CDP1822 and CDP1822C are 256-word by 4-bit static random-access memories designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and a wide operating voltage range. Both types have separate data inputs and outputs and utilize single power supplies of 4 to 6.5 volts for the CDP1822C and 4 to 10.5 volts for the CDP1822.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAMs to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

The CDP1822 and CDP1822C types are supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix). The CDP1822C is also available in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	Chip Select 1 $\overline{CS_1}$	Chip Select 2 CS_2	Output Disable OD	Read/Write R/$\overline{W}$	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

File Number **1074**

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1822		CDP1822C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1822 ..... -0.5 to +11 V
CDP1822C ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A=-40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A=-55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A=+100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPE D ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in (1 59 ± 0 79 mm) from case for 10 s max ..... +265° C

5

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, Except as Noted

CHARACTERISTIC		TEST CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1822			CDP1822C			
					Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current,	I_{DD}	—	0, 5	5	—	—	500	—	—	500	μA
		—	0, 10	10	—	—	1000	—	—	—	
Output Voltage: Low-Level,	V_{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
High-Level,	V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage,	V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
		0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage,	V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
		0.5,9.5	—	10	7	—	—	—	—	—	
Output Low (Sink) Current,	I_{OL}	0.4	0, 5	5	2	4	—	2	4	—	mA
		0.5	0, 10	10	4.5	9	—	—	—	—	
Output High (Source) Current,	I_{OH}	4.6	0, 5	5	-1	-2	—	-1	-2	—	
		9.5	0, 10	10	-2.2	-4.4	—	—	—	—	
Input Current,	I_{IN}	—	0, 5	5	—	—	±5	—	—	±5	μA
		—	0, 10	10	—	—	±10	—	—	—	
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	—	±5	—	—	±5	
		0, 10	0, 10	10	—	—	±10	—	—	—	
Operating Current,	I_{DD1}†	—	0, 5	5	—	4	8	—	4	8	mA
		—	0, 10	10	—	8	16	—	—	—	
Input Capacitance,	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance,	C_{OUT}	—	—	—	—	10	15	—	10	15	

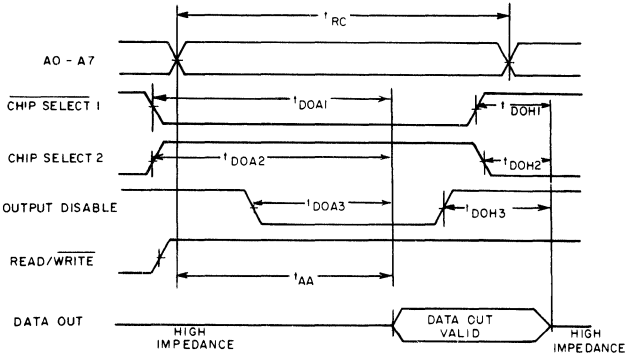
†Outputs open circuited, cycle time = 1 μs
*Typical values are for T_A = 25° C and nominal V_{DD}

CDP1822, CDP1822C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, Input t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
			CDP1822			CDP1822C			
			Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle Times (Fig. 1)									
Read Cycle	t_{RC}	5	450	—	—	450	—	—	ns
		10	250	—	—	—	—	—	
Access from Address	t_{AA}	5	—	250	450	—	250	450	
		10	—	150	250	—	—	—	
Output Valid from $\overline{\text{Chip-Select 1}}$	t_{DOA1}	5	—	250	450	—	250	450	
		10	—	150	250	—	—	—	
Output Valid from Chip-Select 2	t_{DOA2}	5	—	250	450	—	250	450	
		10	—	150	250	—	—	—	
Output Valid from Output Disable	t_{DOA3}	5	—	—	200	—	—	200	
		10	—	—	110	—	—	—	
Output Hold from $\overline{\text{Chip-Select 1}}$	t_{DOH1}	5	20	—	—	20	—	—	
		10	20	—	—	—	—	—	
Output Hold from Chip-Select 2	t_{DOH2}	5	20	—	—	20	—	—	
		10	20	—	—	—	—	—	
Output Hold from Output Disable	t_{DOH3}	5	20	—	—	20	—	—	
		10	20	—	—	—	—	—	

†Time required by a limit device to allow for indicated function
*Typical values are for T_A = 25°C and nominal V_{DD}



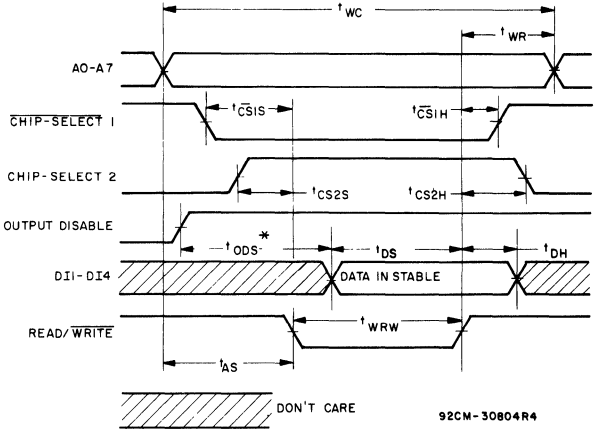
92CM-30244R4

Fig 1 - Read cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, Input t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
			CDP1822			CDP1822C			
			Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Write Cycle Times (Fig. 2)									
Write Cycle	t_{WC}	5	500	—	—	500	—	—	ns
		10	300	—	—	—	—	—	
Address Set-Up	t_{AS}	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	
Write Recovery	t_{WR}	5	50	—	—	50	—	—	
		10	40	—	—	—	—	—	
Write Width	t_{WRW}	5	250	—	—	250	—	—	
		10	150	—	—	—	—	—	
Input Data Set-Up Time	t_{DS}	5	250	—	—	250	—	—	
		10	150	—	—	—	—	—	
Data In Hold	t_{DH}	5	50	—	—	50	—	—	
		10	40	—	—	—	—	—	
$\overline{\text{Chip-Select}}$ 1 Set-Up	$t_{\overline{CS}1S}$	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	
Chip-Select 2 Set-Up	t_{CS2S}	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	
$\overline{\text{Chip-Select}}$ 1 Hold	$t_{\overline{CS}1H}$	5	0	—	—	0	—	—	
		10	0	—	—	0	—	—	
Chip-Select 2 Hold	t_{CS2H}	5	0	—	—	0	—	—	
		10	0	—	—	0	—	—	
Output Disable Set-Up	t_{ODS}	5	200	—	—	200	—	—	
		10	110	—	—	—	—	—	

†Time required by a limit device to allow for indicated function.
*Typical values are for T_A = 25°C and nominal V_{DD}



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY, FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE

Fig. 2 - Write cycle timing waveforms.

CDP1822, CDP1822C

DATA RETENTION CHARACTERISTICS at T_A = -40 to +85° C, see Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	V_{DR} (V)	V_{DD} (V)	CDP1822			CDP1822C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	600	—	—	
	—	10	300	—	—	—	—	—	
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f	2	5	1	—	—	1	—	—	μs

*Typical values are for T_A = 25° C and nominal V_{DD}

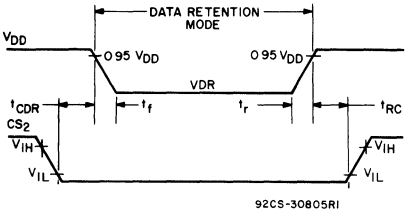


Fig. 3 - Low V_{DD} data retention timing waveforms

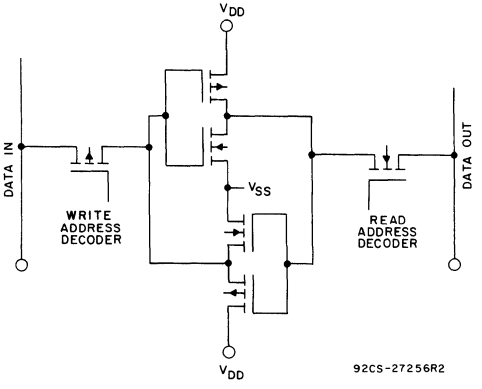


Fig. 4 - Memory cell configuration.

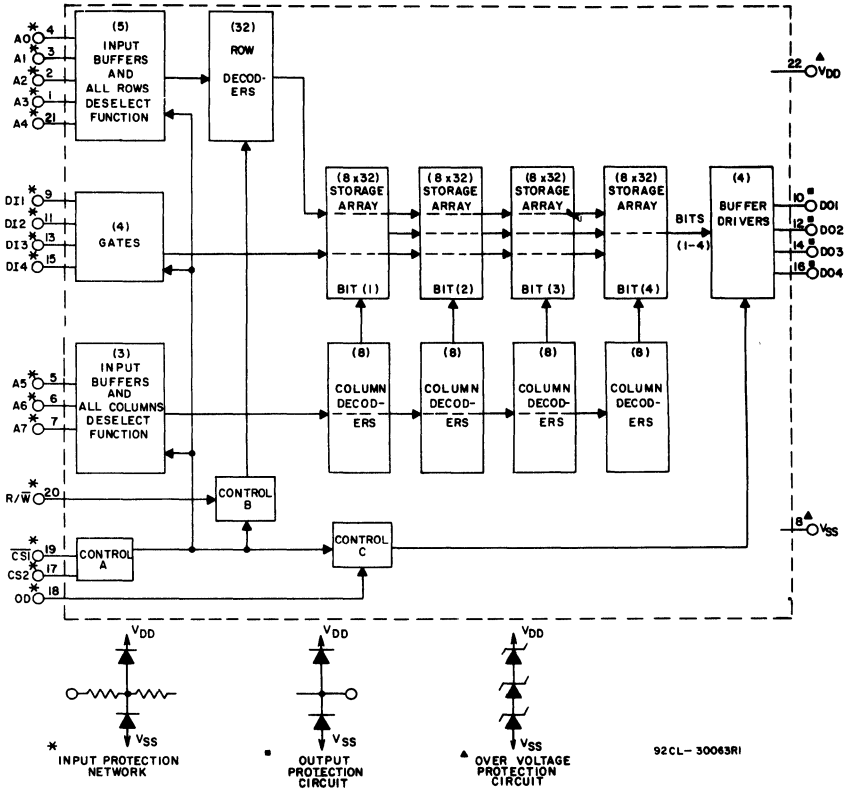


Fig. 5 - Functional block diagram for CDP1822 and CDP1822C.

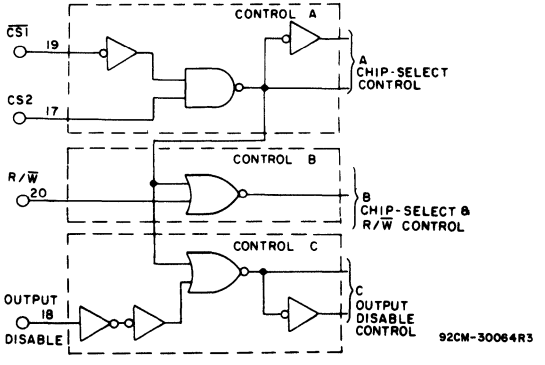


Fig. 6 - Logic diagram of controls for CDP1822 and CDP1822C.