CDP1822C/3

High-Reliability CMOS 256-Word x 4-Bit LSI Static RAM

March 1997

Features

- **For Applications in Aerospace, Military, and Critical Industrial Equipment**
- **Interfaces Directly with CDP1802 Microprocessor**
- **Very Low Operating Current**
  - **At V_{DD} = 5V and Cycle Time = 1μs . . . . . 4mA (Typ)**
- **Static CMOS Silicon-On-Sapphire Circuitry**
  - **CD4000 Series Compatible**
- **Industry Standard Pinout**
- **Two Chip Select Inputs - Simple Memory Expansion**
- **Memory Retention for Standby. . . . . 2V (Min) Battery Voltage**
- **Single Power Supply Operation . . . . . 4V to 6.5V**
- **High Noise Immunity 30% of V_{DD}. . . . . 4V to 6.5V**
- **Output Disable for Common I/O Systems**
- **Three-State Data Output for Bus Oriented Systems**
- **Separate Data Inputs and Outputs**
- **Latch-Up-Free Transient Radiation Tolerance**

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
SBDIP	-55°C to +125°C	CDP1822CD3	D22.4A

Description

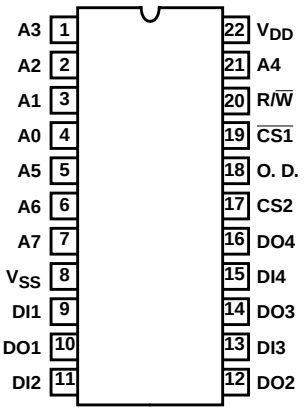
The CDP1822C/3 is a 256 word by 4-bit random access memory designed for use in memory systems where high speed, low operating current, and simplicity in use are desirable. The CDP1822 features high speed and excellent noise immunity. It has separate data inputs and outputs and utilizes a single power supply of 4V to 6.5V.

Two Chip Select inputs simplify system expansion. An output Disable control provides Wire-OR-capability and is also useful in common Input/Output systems. The Output Disable input allows this RAM to be used in common data Input/Output systems by forcing the output into a high impedance state during a write operation independent of the Chip Select input condition. The output assumes a high impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

Pinout

CDP1822C/3 (SBDIP)
TOP VIEW



OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	$\overline{\text{CHIP SELECT 1}}$ ($\overline{CS1}$)	CHIP SELECT 2 (CS2)	OUTPUT DISABLE (OD)	READ/$\overline{\text{WRITE}}$ (R/$\overline{W}$)	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

Logic 1 = High, Logic 0 = Low, X = Don't Care

File Number **2981.1**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1822C/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
Operating Temperature Range (T_A) . . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SBDIP Package	80	21

Maximum Storage Temperature Range (T_{STG}) . . . -65^oC to $+150^oC$
Maximum Lead Temperature (During Soldering) . . . . . $+265^oC$
Maximum Junction Temperature . . . . . $+150^oC$

Recommended Operating Conditions

At T_A = Full Package Temperature Range.For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS		UNITS
	MIN	MAX	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V

Static Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS			LIMITS				UNITS
					-55^oC, $+25^oC$		$+125^oC$		
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	-	0, 5	5	-	390	-	1000	µA
Output Low (Sink) Current (Note 1)	I_{OL}	0.4	0, 5	5	2.6	-	1.6	-	mA
Output High (Source) Current (Note 1)	I_{OH}	4.6	0, 5	5	-	-1.2	-	-0.8	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0.1	-	0.5	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	V_{DD} - 0.1	-	V_{DD} - 0.5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	0.3 V_{DD}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	0.7 V_{DD}	-	0.7 V_{DD}	-	V
Input Leakage Current (Note 1)	I_{IN}	-	0, 5	5	-	±3.2	-	±10	µA
Operating Current (Note 1)	I_{DD1}	-	0, 5	5	-	6.5	-	10	mA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	±3.2	-	± 19	µA
Input Capacitance	C_{IN}	-	-	-	-	7.5	-	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	7.5	-	7.5	pF

NOTE:

1. Limits designate 100% testing, all other limits are designer's parameters under given test conditions and do not represent 100% testing.

Read Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			MIN	MAX	MIN	MAX	
Read Cycle (Note 1)	t_{RC}	5	370	-	500	-	ns
Access from Address (Note 1)	t_{ADA}	5	-	370	-	500	ns
Output Valid from $\overline{\text{Chip}}$ $\overline{\text{Select}}$ 1 (Note 1)	t_{DOA1}	5	-	370	-	500	ns
Output Valid from Chip Select 2 (Note 1)	t_{DOA2}	5	-	370	-	500	ns
Output Active from Output Disable (Note 1)	t_{DOA3}	5	-	170	-	225	ns
Output Hold from $\overline{\text{Chip}}$ $\overline{\text{Select}}$ 1	t_{DOH1}	5	10	-	20	-	ns
Output Hold from Chip Select 2	t_{DOH2}	5	10	-	20	-	ns
Output Hold from Output Disable	t_{DOH3}	5	10	-	20	-	ns

NOTE:

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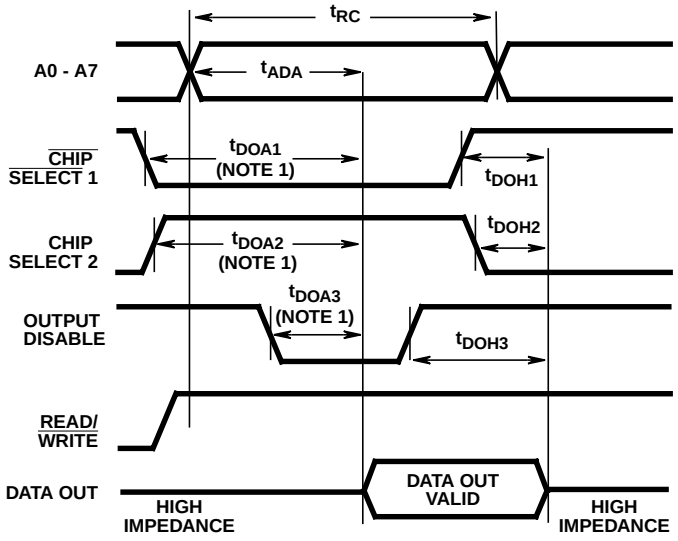


NOTE: Minimum timing for valid data output. Longer times will initiate an earlier but invalid output.

FIGURE 1. READ CYCLE WAVEFORMS AND TIMING DIAGRAM

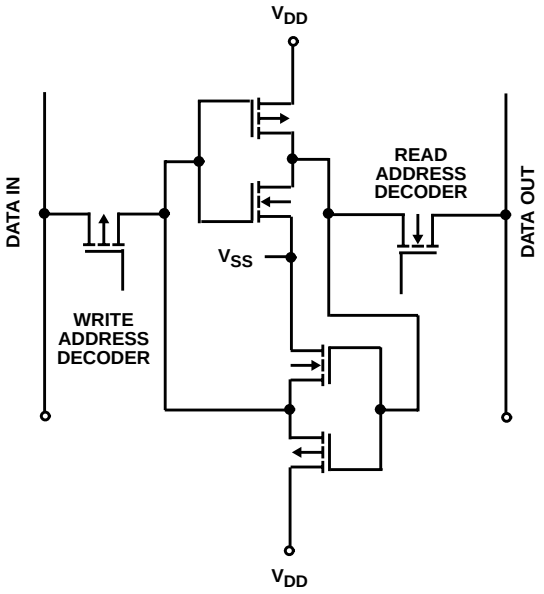


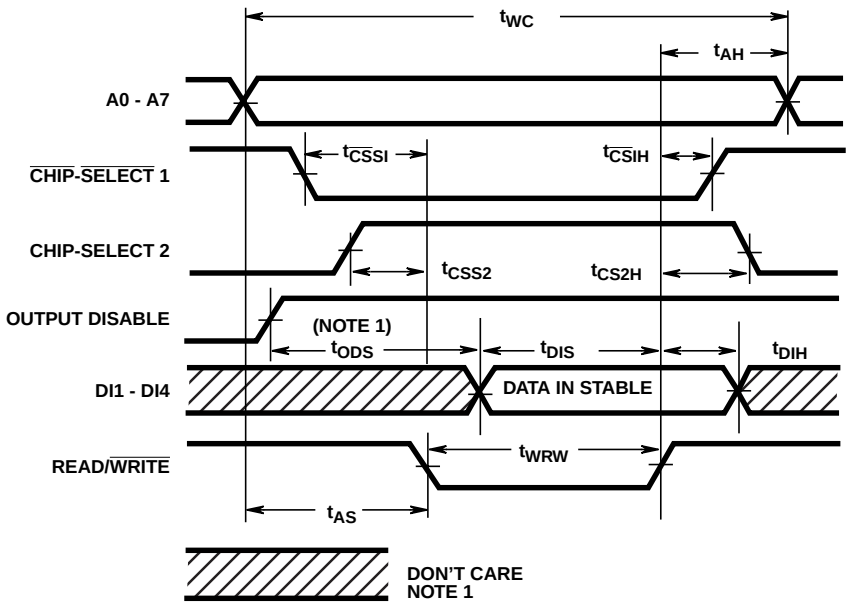
FIGURE 2. MEMORY CELL CONFIGURATION

Write Cycle Dynamic Electrical Specifications t_R, t_F = 10ns, C_L = 50pF

PARAMETER	SYMBOL	V_{DD} (V)	LIMITS				UNITS
			+25°C, -55°C		+125°C		
			MIN	MAX	MIN	MAX	
Write Cycle (Note 1)	t_{WC}	5	400	-	560	-	ns
Address Setup (Note 1)	t_{AS}	5	160	-	225	-	ns
Address Hold (Note 1)	t_{AH}	5	40	-	55	-	ns
Write Pulse Width (Note 1)	t_{WRW}	5	200	-	280	-	ns
Data in Setup (Note 1)	t_{DIS}	5	200	-	280	-	ns
Data in Hold (Note 1)	t_{DIH}	5	40	-	55	-	ns
$\overline{\text{Chip Select}}$ 1 Setup	$t_{\overline{CS}S1}$	5	200	-	280	-	ns
Chip Select 2 Setup	t_{CSS2}	5	200	-	280	-	ns
Output Disable Setup	t_{ODS}	5	140	-	225	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing



NOTE:

1. t_{ODS} is required for common I/O operation only; for separate I/O operations, output disable is don't care.

FIGURE 3. WRITE CYCLE TIMING WAVEFORMS

Data Retention Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_{DR} (V)	TEST CONDITIONS V_{DD} (V)	LIMITS +25°C, -55°C MIN	LIMITS +25°C, -55°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Minimum Data Retention Voltage (Note 1)	V_{DR}	-	-	-	2	-	2.5	V
Data Retention Quiescent Current (Note 1)	I_{DD}	2	-	-	70	-	380	µA
Chip Deselect to Data Retention Time	t_{CDR}	-	5	450	-	650	-	ns
		-	10					
Recovery to Normal Operation Time	t_{RC}	5	5	450	-	650	-	ns

NOTE:

1. Limits designate 100% testing. All other limits are designer's parameters under given test conditions and do not represent 100% testing.

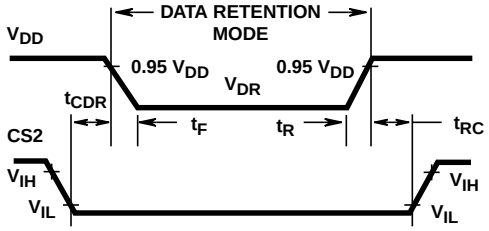
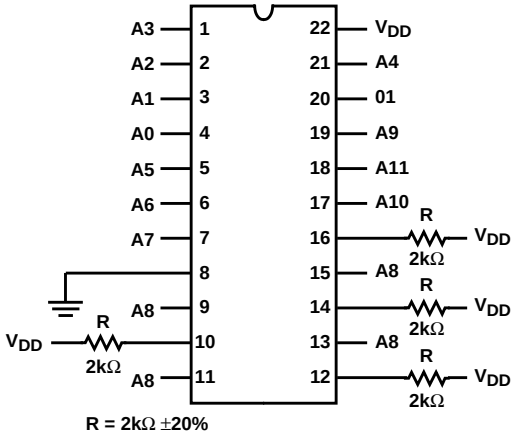


FIGURE 4. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS



PACKAGE	TEMPERATURE	DURATION	V_{DD}
D	125°C	160 Hrs	7V

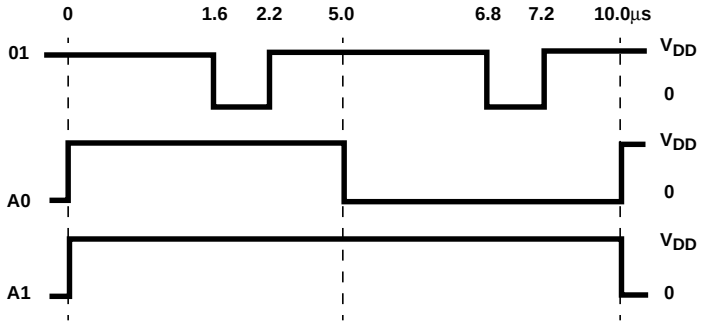


FIGURE 5. DYNAMIC/OPERATING BURN-IN CIRCUIT AND TIMING DIAGRAM

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.