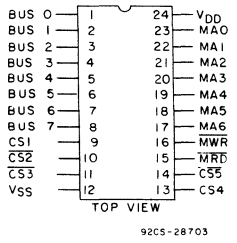
CDP1823, CDP1823C



TERMINAL ASSIGNMENT

128-Word x 8-Bit Static Random-Access Memory

Features:

- *Fast access time:*
  450 ns at V_{DD}= 5 V;
  250 ns at V_{DD} = 10 V
- *Common data inputs and outputs*
- *Multiple-chip select inputs to simplify memory system expansion*

The RCA-CDP1823 and CDP1823C are 128-word by 8-bit CMOS SOS static random-access memories. These memories are compatible with general-purpose microprocessors. The two memories are functionally identical. They differ in that the CDP1823 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1823C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1823 memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823, the chip-select inputs $\overline{CS2}$, $\overline{CS3}$, and $\overline{CS5}$ require a low input signal, and the chip-select inputs CS1 and CS4 require a high input signal.

The $\overline{MRD}$ signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the $\overline{MRD}$ signal goes high, the device is deselected, or t_{AA} (access time) after address changes.

The CDP1823 and CDP1823C are supplied in hermetic 24-lead dual-in-line ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).

OPERATIONAL MODES

Function	$\overline{MRD}$	$\overline{MWR}$	CS1	$\overline{CS2}$	$\overline{CS3}$	CS4	$\overline{CS5}$	Bus Terminal State
READ	0	X	1	0	0	1	0	Storage State of Addressed Word
WRITE	1	0	1	0	0	1	0	Input High-Impedance
STAND-BY (ACTIVE)	1	1	1	0	0	1	0	High-Impedance
NOT SELECTED	X	X	0	X	X	X	X	High-Impedance
	X	X	X	1	X	X	X	
	X	X	X	X	1	X	X	
	X	X	X	X	X	0	X	
	X	X	X	X	X	X	1	

Logic 1 = High Logic 0 = Low X = Don't Care

File Number **1198**

CDP1823, CDP1823C

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1823D		CDP1823CD		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltage values referenced to V_{SS} terminal)
CDP1823 ..... −0.5 to +11 V
CDP1823C ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
OPERATING-TEMPERATURE RANGE (T_A):
CERAMIC PACKAGES (D SUFFIX TYPES) ..... −55 to +125 °C
PLASTIC PACKAGES (E SUFFIX TYPES) ..... −40 to +85 °C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265 °C

STATIC ELECTRICAL CHARACTERISTICS at T_A = −40 to + 85° C, Except as noted

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	V_O	V_{IN}	V_{DD}	CDP1823			CDP1823C			
	(V)	(V)	(V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device —	—	0,5	5	—	—	500	—	—	500	μA
Current, I_{DD}	—	0,10	10	—	—	1000	—	—	—	
Output Voltage:	—	0,5	5	—	0	0.1	—	0	0.1	V
Low-Level, V_{OL}	—	0,10	10	—	0	0.1	—	—	—	
High-Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	
Output Low (Sink)	0.4	0,5	5	2	4	—	2	4	—	mA
Current, I_{OL}	0.5	0,10	10	4.5	9	—	—	—	—	
Output High (Source)	4.6	0,5	5	−1	−2	—	−1	−2	—	
Current, I_{OH}	9.5	0,10	10	−2.2	−4.4	—	—	—	—	
Input Current, I_{IN}	Any	0,5	5	—	—	±5	—	—	±5	μA
	Input	0,10	10	—	—	±10	—	—	—	
3-State Output	0,5	0,5	5	—	—	±5	—	—	±5	
Leakage Current, I_{OUT}	0,10	0,10	10	—	—	±10	—	—	—	
Operating Current, I_{DD1}†	—	0,5	5	—	4	8	—	4	8	mA
	—	0,10	10	—	8	16	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	

†Outputs open circuited; cycle time = 1 μs.
*Typical values are for T_A = 25° C and nominal V_{DD}.

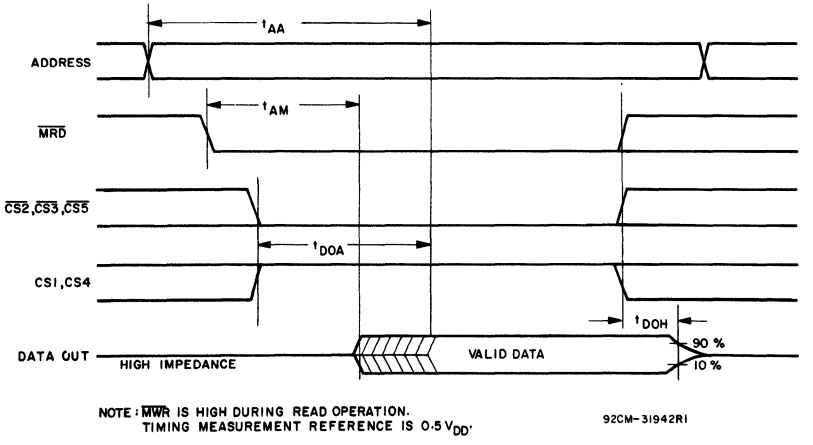
CDP1823, CDP1823C

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} \pm 5\%$, $t_r, t_f = 20$ ns, $C_L = 100$ pF.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle (See Fig. 1)								
Access Time From Address Change, t_{AA}	5	—	275	450	—	275	450	ns
	10	—	150	250	—	—	—	
Access Time From Chip Select, t_{DOA}	5	—	150	250	—	150	250	
	10	—	100	150	—	—	—	
$\overline{MRD}$ to Output Active, t_{AM}	5	—	150	250	—	150	250	
	10	—	100	150	—	—	—	
Data Hold Time After Read, t_{DOH}	5	25	50	75	25	50	75	
	10	15	25	40	—	—	—	

*Typical values are at $T_A = 25°C$ and nominal voltage.

†Time required by a limit device to allow for the indicated function.



NOTE: $\overline{MWR}$ IS HIGH DURING READ OPERATION.
TIMING MEASUREMENT REFERENCE IS $0.5 V_{DD}$.

92CM-31942R1

Fig, 1 - Read cycle timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85 °C, V_{DD} ± 5%, t_r,t_f = 20 ns, C_L = 100 pF.

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Write Cycle (See Fig. 2)								
Write Recovery, tWR	5	75	—	—	75	—	—	ns
	10	50	—	—	—	—	—	
Write Cycle, t_{WC}	5	400	—	—	400	—	—	
	10	225	—	—	—	—	—	
Write Pulse Width, tWRW	5	200	—	—	200	—	—	
	10	100	—	—	—	—	—	
Address Setup Time, tAS	5	125	—	—	125	—	—	
	10	75	—	—	—	—	—	
Data Setup Time, tDS	5	100	—	—	100	—	—	
	10	75	—	—	—	—	—	
Data Hold Time From $\overline{MWR}$, t_{DH}	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	

*Typical values are at T_A = 25 °C and nominal voltage.

†Time required by a limit device to allow for the indicated function.

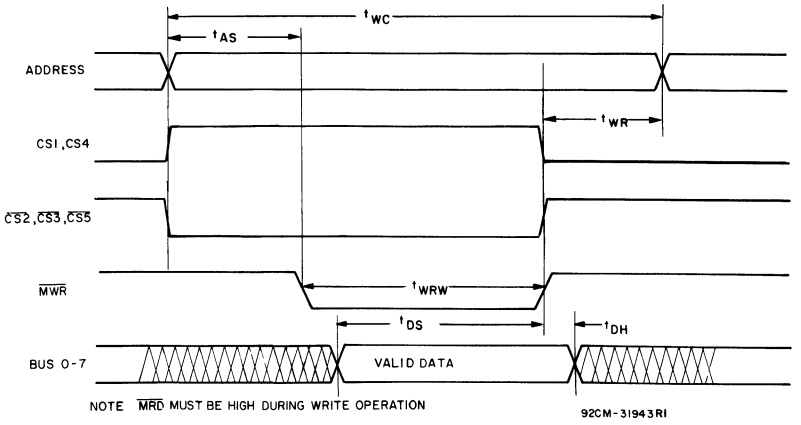


Fig. 2 - Write cycle timing diagram.

CDP1823, CDP1823C

DATA RETENTION CHARACTERISTICS at T_A = −40 to +85°C; see Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			CDP1823			CDP1823C			
	V_{DR} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min. Data Retention Voltage, V_{DR}	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	2	—	—	30	100	—	30	100	μA
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	600	—	—	
	—	10	300	—	—	—	—	—	
V_{DD} to V_{DR} Rise and Fall Time t_r, t_f	2	5	1	—	—	1	—	—	μs

*Typical values are for T_A = 25°C and nominal V_{DD}.

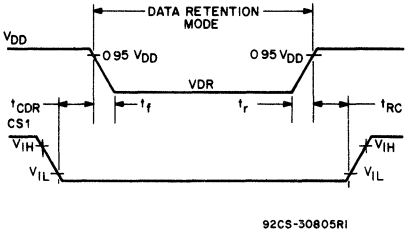
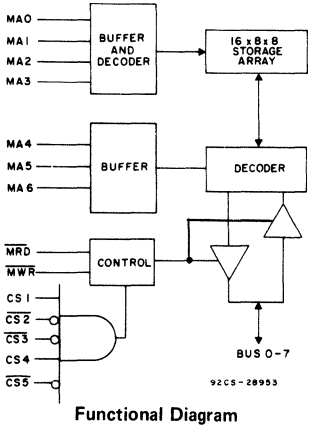


Fig. 3 - Low V_{DD} data retention timing waveforms.



Functional Diagram

Fig. 4 - Functional diagram.

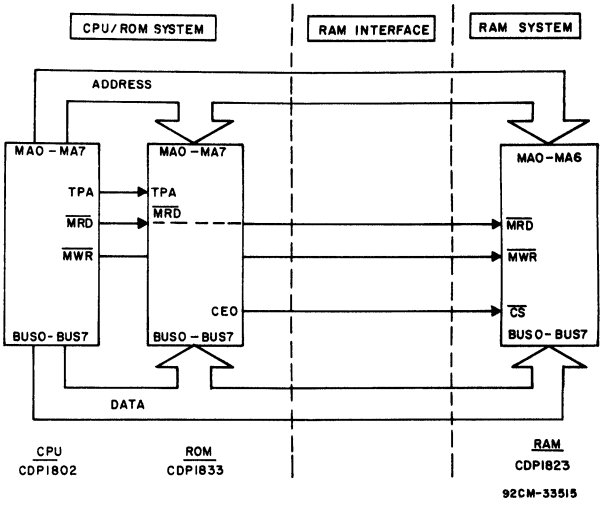


Fig. 5 - CDP1823 (128 x 8) minimum system (128 x 8)

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