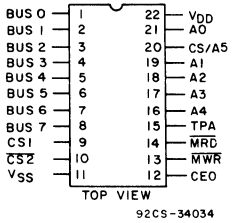
# CDP1826C




**TERMINAL ASSIGNMENT**

## CMOS 64-Word x 8-Bit Static Random-Access Memory

**Features:**

- *Ideal for small, low-power RAM Memory requirements in microprocessor and microcomputer applications*
- *Interfaces with CDP1800-series microprocessors without additional address decoding*
- *Daisy chain feature to further reduce external decoding needs*
- *Multiple chip-select inputs for versatility*
- *Single voltage supply*
- *No clock or precharge required*

The RCA CDP1826C is a general-purpose, fully static, 64-word x 8-bit random-access memory, for use in CDP1800 series or other microprocessor systems where minimum component count and/or price performance and simplicity in use are desirable.

The CDP1826C has 8 common data input and data-output terminals with 3-state capability for direct connection to a standard bi-directional data bus Two chip-select inputs — CS1 and $\overline{CS2}$ — are provided to simplify memory-system expansion. An additional select pin, CS/A5, is provided to enable the CDP1826C to be selected directly from the CDP1800 multiplexed address bus without additional latching or decoding In an 1800 system, the CS/A5 pin can be tied to any MA address line from the CDP1800 processor. A TPA input is provided to latch the high-order bit of this address line as a chip-select for the CDP1826C. If this CS/A5 input is latched high, and if CS = 1 and $\overline{CS2}$ = 0 at the appropriate time in the memory cycle, the CDP1826C will be enabled for writing or reading. In a non-1800 system, the TPA pin can be tied high, and the CS/A5 pin can be used as a normal address input

The six input-address buffers are gated with the chip-select function to reduce standby current when the device is deselected, as well as to provide for a simplified power down mode by reducing address buffer sensitivity to long fall times from address drivers which are being powered down

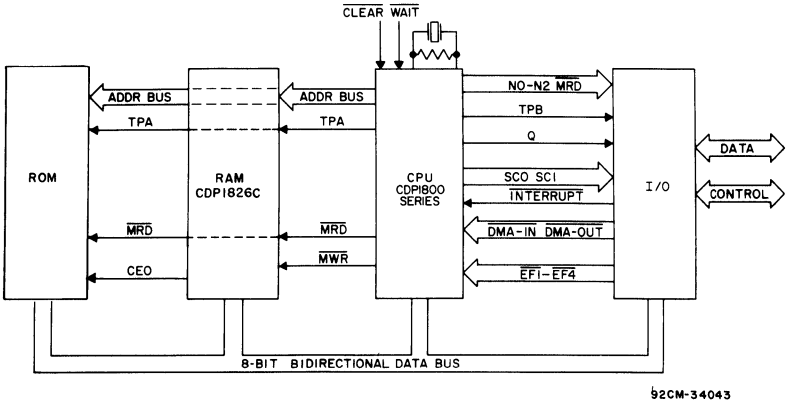



*Fig 1 - Typical CDP1802 microcprocessor system*

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File Number **1311**

# CDP1826C

Two memory control signals, $\overline{MRD}$ and $\overline{MWR}$, are provided for reading from and writing to the CDP1826C. The logic is designed so that $\overline{MWR}$ overrides $\overline{MRD}$, allowing the chip to be controlled from a single R/$\overline{W}$ line.

For such an interface, the $\overline{MRD}$ line can be tied to $V_{SS}$, with the $\overline{MWR}$ line connected to R/$\overline{W}$.

A CHIP ENABLE OUTPUT is provided for daisy-chaining to additional memories or I/O devices. This output is high whenever the chip-select function selects the CDP1826C, which deselects any other chip which has its $\overline{CS}$ input connected to the CDP1826C CEO output. The connected chip is selected when the CDP1826C is de-selected and the $\overline{MRD}$ input is low. Thus, the CEO is only active for a read cycle and can be set up so that a CEO of another device can feed the $\overline{MRD}$ of the CDP1826C, which in turn selects a third chip in the daisy chain.

The CDP1826C has a recommended operating voltage of 4.5 to 5.5 V and is supplied in 22-lead hermetic dual-in-line side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix). The CDP1826C is also available in chip form (H suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to $V_{DD}$ +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE ($P_D$)
For $T_A$ = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For $T_A$ = −55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE ($T_A$)
PACKAGE TYPE D ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1 59 ± 0 79 mm) from case for 10 s max ..... +265°C

**RECOMMENDED OPERATING CONDITIONS** *at $T_A$ = Full Package Temperature Range.*
*For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:*

| CHARACTERISTIC | | LIMITS CDP1826C MIN. | LIMITS CDP1826C MAX. | UNITS |
|---|---|---|---|---|
| DC Operating Voltage Range | | 4.5 | 6.5 | V |
| Input Voltage Range | | $V_{SS}$ | $V_{DD}$ | |
| Input Signal Rise or Fall Time<br>$V_{DD}$ = 5 V | $t_r$, $t_f$ | — | 10 | μs |

**STATIC ELECTRICAL CHARACTERISTICS** *at $T_A = -40$ to $+85°C$, $V_{DD} = 5V \pm 5\%$ except as noted*

| CHARACTERISTIC | | | CONDITIONS | | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | $V_O$ (V) | $V_{IN}$ (V) | CDP1826C | | | |
| | | | | | MIN. | TYP.• | MAX. | |
| Quiescent Device Current | | $I_{DD}$ | — | 0,$V_{DD}$ | — | 5 | 50 | μA |
| Output Low Drive (Sink) Current | $I_{OL}$ | BUS | 0.4 | 0,$V_{DD}$ | 1.6 | 3.2 | — | mA |
| | | CEO | | | 0.8 | 1.6 | — | |
| Output High Drive (Sink) Current | $I_{OH}$ | BUS | $V_{DD}$-0.4 | 0,$V_{DD}$ | -1.0 | -1.5 | — | |
| | | CEO | | | -0.6 | -1.0 | — | |
| Output Voltage Low Level | | $V_{OL}$ | — | 0,$V_{DD}$ | — | 0 | 0.1 | V |
| Output Voltage High Level | | $V_{OH}$ | — | 0,$V_{DD}$ | $V_{DD}$-0.1 | $V_{DD}$ | — | |
| Input Low Voltage | | $V_{IL}$ | | — | — | — | 1.5 | |
| Input High Voltage | | $V_{IH}$ | | — | 3.5 | — | — | |
| Input Leakage Current | | $I_{IN}$ | Any Input | 0,$V_{DD}$ | — | ±0.1 | ±1 | μA |
| 3-State Output Leakage Current | | $I_{OUT}$ | 0,$V_{DD}$ | 0,$V_{DD}$ | — | ±0.1 | ±1 | |
| Operating Device Current | | $I_{OPER}$† | — | 0,$V_{DD}$ | — | 5 | 10 | mA |
| Input Capacitance | | $C_{IN}$ | — | — | — | 5 | 7.5 | pF |
| Output Capacitance | | $C_{OUT}$ | — | 0,$V_{DD}$ | — | 10 | 15 | |

•Typical values are for $T_A = 25°C$ and nominal $V_{DD}$.
†Outputs open circuited, cycle times = 1 μs

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**Signal Descriptions**

**A0-A4, CS/A5 (Address Inputs):**

These inputs must be stable prior to a write operation, but may change asynchronously during Read operations.

In an 1800 system, the multiplexed high-order address bit at pin CS/A5 can be latched at the end of TPA A high level will provide a valid chip select for the CDP1826C. The low-order address bit which appears after TPA is used for data word selection. In non-1800 systems, TPA can be tied high to disable the latch and allow the CS/A5 pin to function as a normal address input.

**BUS 0 — BUS 7:** 8-bit 3-state common input/output data bus.

**TPA:** High-order address strobe input. The high-order address bit at input CS/A5 is latched on the high-to-low transition of the TPA input. Tie TPA high to disable the CS/A5 latch feature.

**CS1, $\overline{CS2}$ (Chip Selector):**

Either chip select (CS1 or $\overline{CS2}$), when not valid, powers down the chip, disables READ and WRITE functions, and gates off the address and output buffers.

**$\overline{MRD}$, $\overline{MWR}$:** Read and Write control signals. $\overline{MWR}$ overides $\overline{MRD}$, allowing the CDP1826C to be controlled from a single R/$\overline{W}$ line.

**CEO (Chip Enable Output):**

Allows daisy chaining to additional memories. CEO is high whenever the CDP1826C is selected. CEO is only active (low) for a Read cycle with the CDP1826C deselected and the $\overline{MRD}$ input low.

**$V_{DD}$, $V_{SS}$:** Power supply connections.

# CDP1826C

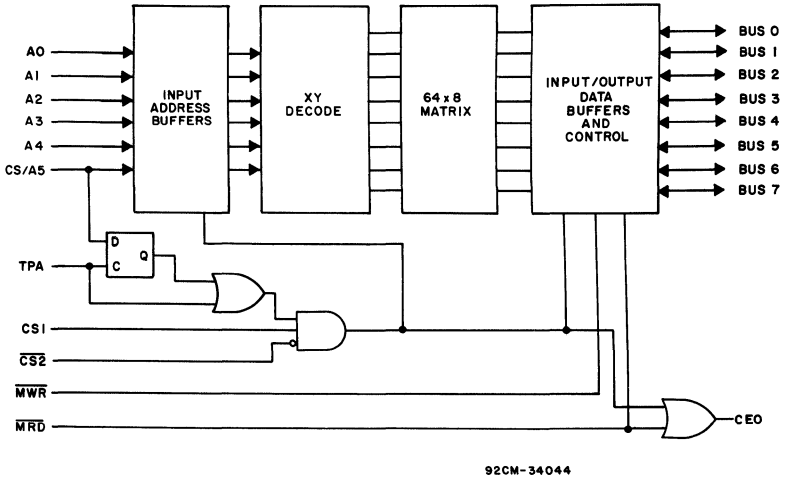
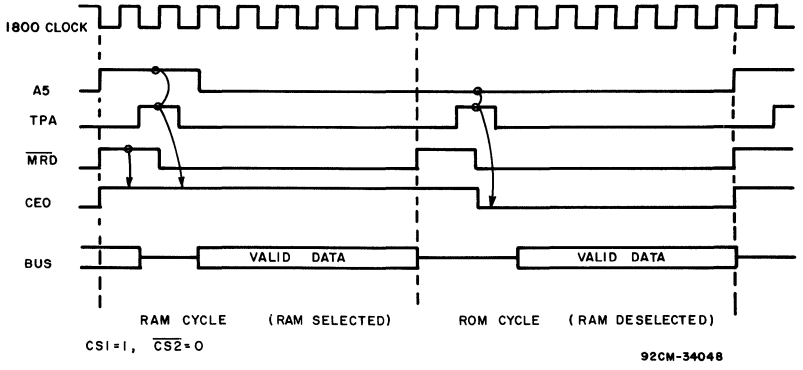



*Fig. 2 - Functional diagram*




OPERATING MODES

| | FUNCTION | $\overline{MRD}$ | $\overline{MWR}$ | CS1·$\overline{CS2}$ | TPA | CS/A5# | CEO |
|---|---|---|---|---|---|---|---|
| CDP1800 MODE | WRITE | X | 0 | 1 | ⊓↓ | 1 | 1 |
| | READ | 0 | 1 | 1 | ⊓↓ | 1 | 1 |
| | DESELECT | 1 | 1 | 1 | ⊓↓ | 1 | 1 |
| | DESELECT | 1 | X | 0 | X | X | 1 |
| | DESELECT | 0 | X | 0 | X | X | 0 |
| | DESELECT | 1 | X | X | ⊓↓ | 0 | 1 |
| | DESELECT | 0 | X | X | ⊓↓ | 0 | 0 |
| NON-CDP1800 MODE | WRITE | X | 0 | 1 | 1 | X | 1 |
| | READ | 0 | 1 | 1 | 1 | X | 1 |
| | DESELECT | 1 | 1 | 1 | 1 | X | 1 |
| | DESELECT | 1 | X | 0 | 1 | X | 1 |
| | DESELECT | 0 | X | 0 | 1 | X | 0 |

# FOR CDP1800 MODE, REFERS TO HIGH ORDER MEMORY ADDRESS BIT LEVEL AT TIME WHEN TPA ↓ TRANSITION TAKES PLACE

*Fig 3 - Chip Enable Output timing waveforms for CDP1800-based systems.*

**DYNAMIC ELECTRICAL CHARACTERISTICS** *at $T_A = -40$ to $+85°C$, $V_{DD} = 5\ V \pm 5\%$, Input $t_r, t_f = 10$ ns; $C_L = 50$ pF and 1 TTL Load*

| CHARACTERISTIC | LIMITS CDP1826C MIN.† | TYP.• | MAX. | UNITS |
|---|---|---|---|---|
| **Read — Cycle Times (Figs. 4 and 5)** | | | | |
| Address to TPA Setup $t_{ASH}$ | 100 | — | — | ns |
| Address to TPA Hold $t_{AH}$ | 100 | — | — | |
| Access from Address Change $T_{AA}$ | — | 500 | 1000 | |
| TPA Pulse Width $t_{PAW}$ | 200 | — | — | |
| Output Valid from $\overline{MRD}$ $t_{AM}$ | — | 500 | 1000 | |
| Access from Chip Select $t_{AC}$ | — | 500 | 1000 | |
| CEO Delay from TPA ↘ Edge $t_{CA}$ | — | 150 | 300 | |
| $\overline{MRD}$ to CEO Delay $t_{MC}$ | 75 | — | — | |
| Output High Z from Invalid $\overline{MRD}$ $t_{RHZ}$ | — | — | 125 | |
| Output High Z from Chip Deselect $t_{SHZ}$ | — | — | 225 | |

†Time required by a limit device to allow for the indicated function
•Typical values are for $T_A = 25°C$ and nominal $V_{DD}$.

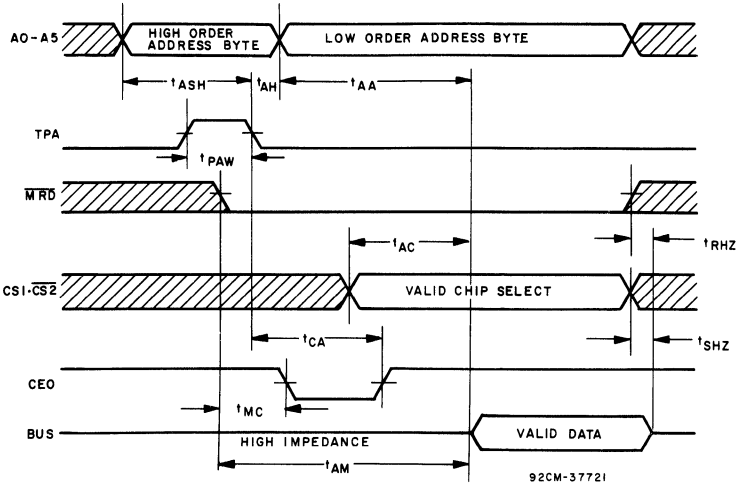



*Fig. 4 - Timing waveforms for Read-cycle 1.*

# CDP1826C

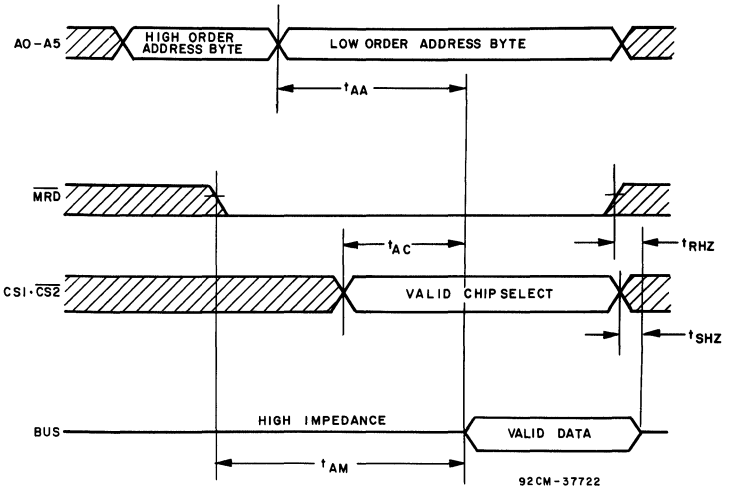



*Fig. 5 - Timing waveforms for Read-cycle 2 [TPA-High].*

**DYNAMIC ELECTRICAL CHARACTERISTICS** *at $T_A = -40$ to $+85°C$, $V_{DD} = 5\ V \pm 5\%$, Input $t_r, t_f = 10$ ns; $C_L = 50$ pF and 1 TTL Load*

| CHARACTERISTIC | LIMITS CDP1826C MIN.† | TYP.• | MAX. | UNITS |
|---|---|---|---|---|
| **Write-Cycle Times (Figs. 6 and 7)** | | | | |
| Address to TPA Setup, High Byte $t_{ASH}$ | 100 | — | — | ns |
| Address to TPA Hold $t_{AH}$ | 100 | — | — | |
| Address Setup Low Byte $t_{ASL}$ | 500 | 250 | — | |
| TPA Pulse Width $t_{PAW}$ | 200 | — | — | |
| Chip Select Setup $t_{CS}$ | 700 | 350 | — | |
| Write Pulse Width $t_{WW}$ | 300 | 200 | — | |
| Write Recovery $t_{WR}$ | 100 | — | — | |
| Data Setup $t_{DS}$ | 400 | 200 | — | |
| Data Hold from End of $\overline{MWR}$ $t_{DH1}$ | 100 | 50 | — | |
| Data Hold from End of Chip Select $t_{DH2}$ | 125 | 50 | — | |

†Time required by a limit device to allow for the indicated function.
•Typical values are for $T_A = 25°C$ and nominal $V_{DD}$.

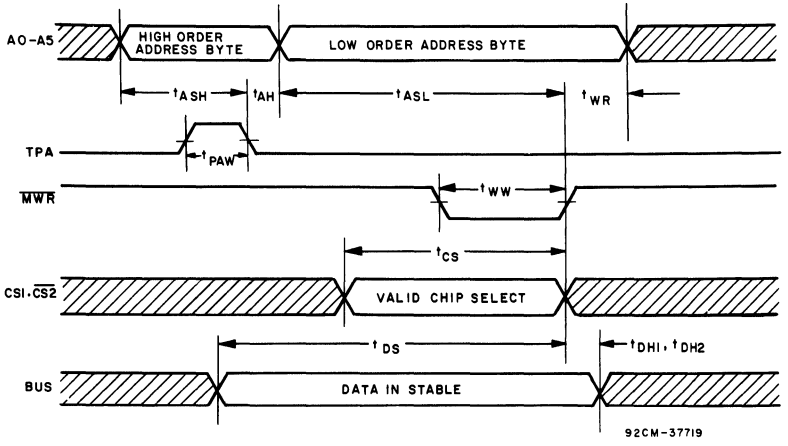



*Fig. 6 - Timing waveforms for Write-cycle 1*



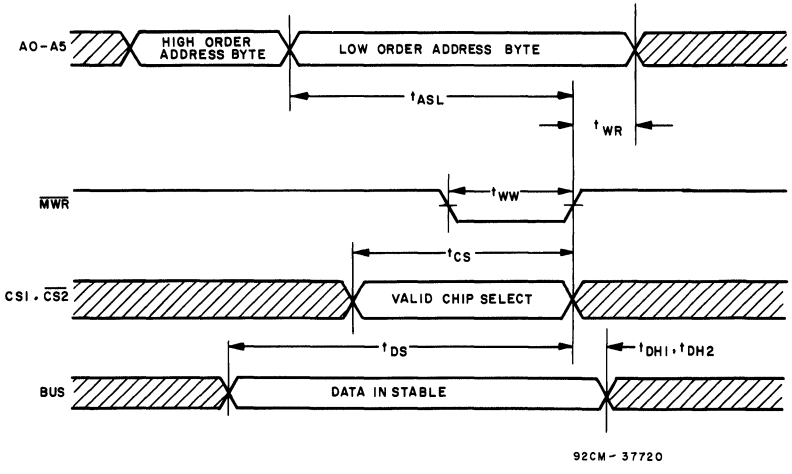



*Fig. 7 - Timing waveforms for Write-cycle 2 [TPA=High].*

# CDP1826C

**DATA RETENTION CHARACTERISTICS** *at $T_A$ = −40 to +85°C; see Fig. 8*

| CHARACTERISTIC | TEST CONDITIONS | | LIMITS CDP1826C | | | UNITS |
|---|---|---|---|---|---|---|
| | $V_{DR}$ (V) | $V_{DD}$ (V) | MIN. | TYP.• | MAX. | |
| Min. Data Retention Voltage $V_{DR}$ | — | — | — | 2 | 2.5 | V |
| Data Retention Quiescent Current $I_{DD}$ | 2.5 | — | — | 5 | 25 | μA |
| Chip Deselect to Data Retention Time $t_{CDR}$ | — | 5 | 600 | — | — | ns |
| Recovery to Normal Operation Time $t_{RC}$ | — | 5 | 600 | — | — | ns |
| $V_{DD}$ to $V_{DR}$ Rise and Fall Time $t_r, t_f$ | 2.5 | 5 | 1 | — | — | μs |

•Typical values are for $T_A$ = 25°C and nominal $V_{DD}$

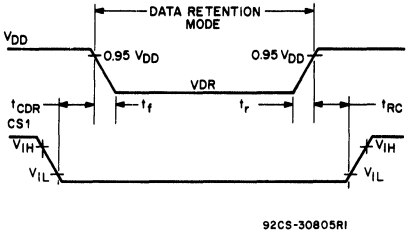



*Fig. 8 - Low $V_{DD}$ data retention timing waveforms.*