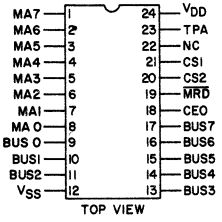
# CDP1831, CDP1831C

**Product Preview**




**Terminal Assignment**

## 512-Word x 8-Bit Static Read-Only Memory

**Features:**

- *Compatible with CDP1800 and CD4000-series devices*
- *On-chip address latch*
- *Interfaces with CDP1802 microprocessor without additional components*
- *Optional programmable location within 64K memory space*
- *Three-state outputs*

The RCA-CDP 1831 and CDP1831C types are 4096-bit mask-programmable CMOS read-only memories organized as 512 words x 8 bits and are completely static; no clocks required. They will directly interface with CDP1800-series micro-processors without additional components.

The CDP1831 and CDP1831C respond to 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 512-word block within 64K memory space. The polarity of the high address strobe (TPA), and CS1 and CS2 are user mask-programmable.

The Chip-Enable output signal (CEO) goes "high" when the device is selected, and is intended for use an an output disable control for RAM memory in a microprocessor system.

The CDP 1831C is functionally identical to the CDP1831. The CDP1831 has an operating voltage range of 4 to 10.5 volts, and the CDP1831C has an operating voltage range of 4 to 6.5 volts.

The CDP1831 and CDP1831C types are supplied in 24-lead hermetic dual-in-line, side-brazed ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1831C is also available in chip form (H suffix).

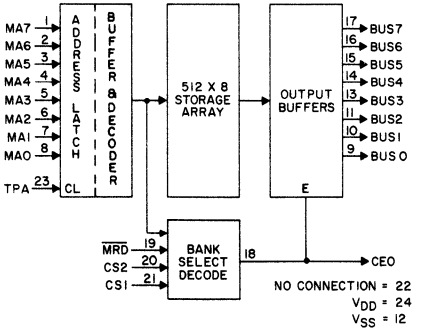



*Fig. 1 - Functional diagram.*

File Number **1104**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(All voltage values referenced to $V_{SS}$ terminal)
CDP1831 ..... −0.5 to +11 V
CDP1831C ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to $V_{DD}$ +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For $T_A$ = −55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For $T_A$ = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE ($T_A$)
PACKAGE TYPE D ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C

**OPERATING CONDITIONS** at $T_A$ = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | | | UNITS |
|---|---|---|---|---|---|
| | CDP1831 | | CDP1831C | | |
| | Min. | Max. | Min. | Max. | |
| DC Operating Voltage Range | 4 | 10.5 | 4 | 6.5 | V |
| Input Voltage Range | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | $V_{DD}$ | |

**STATIC ELECTRICAL CHARACTERISTICS** at $T_A$ = −40 to +85°C, Except as noted

| CHARACTERISTIC | CONDITIONS | | | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | CDP1831 | | | CDP1831C | | | |
| | | | | Min. | Typ.* | Max. | Min. | Typ.* | Max. | |
| Quiescent Device Current, $I_{DD}$ | — | 5 | 5 | — | 0.01 | 50 | — | 0.02 | 200 | μA |
| | — | 10 | 10 | — | 1 | 200 | — | — | — | |
| Output Low Drive (Sink) Current, $I_{OL}$ | 0.4 | 0,5 | 5 | 0.55 | — | — | 0.55 | — | — | mA |
| | 0.5 | 0,10 | 10 | 1.30 | — | — | — | — | — | |
| Output High Drive (Source) Current, $I_{OH}$ | 4.6 | 0,5 | 5 | −0.35 | — | — | −0.35 | — | — | |
| | 9.5 | 0,10 | 10 | −0.65 | — | — | — | — | — | |
| Output Voltage Low-Level, $V_{OL}$ | — | 0,5 | 5 | — | 0 | 0.1 | — | 0 | 0.1 | V |
| | — | 0,10 | 10 | — | 0 | 0.1 | — | — | — | |
| Output Voltage High Level, $V_{OH}$ | — | 0,5 | 5 | 4.9 | 5 | — | 4.9 | 5 | — | |
| | — | 0,10 | 10 | 9.9 | 10 | — | — | — | — | |
| Input Low Voltage, $V_{IL}$ | 0.5,4.5 | — | 5 | — | — | 1.5 | — | — | 1.5 | |
| | 1,9 | — | 10 | — | — | 3 | — | — | — | |
| Input High Voltage, $V_{IH}$ | 0.5,4.5 | — | 5 | 3.5 | — | — | 3.5 | — | — | |
| | 1,9 | — | 10 | 7 | — | — | — | — | — | |
| Input Leakage Current, $I_{IN}$ | Any | 0,5 | 5 | — | $\pm10^{-4}$ | ±1 | — | — | ±1 | mA |
| | Input | 0,10 | 10 | — | $\pm10^{-4}$ | ±2 | — | — | — | |
| 3-State Output Leakage Current, $I_{OUT}$ | 0,5 | 0,5 | 5 | — | $\pm10^{-4}$ | ±1 | — | — | ±1 | |
| | 0,10 | 0,10 | 10 | — | $\pm10^{-4}$ | ±2 | — | — | — | |
| Input Capacitance, $C_{in}$ | — | — | — | — | 5 | 7.5 | — | 5 | 7.5 | pF |
| Output Capacitance, $C_{out}$ | — | — | — | — | 10 | 15 | — | 10 | 15 | |
| Operating Current, $I_{DD1}$† | — | 0,5 | 5 | — | 5 | 10 | — | 5 | 10 | mA |
| | — | 0,10 | 10 | — | 10 | 20 | — | — | — | |

*Typical values are for "one" $T_A$ = 25°C and nominal $V_{DD}$

†Outputs open-circuited, cycle time = 2.5 μs

# CDP1831, CDP1831C

**DYNAMIC ELECTRICAL CHARACTERISTICS** at $T_A = -40$ to $+85°C$, $V_{DD} \pm 5\%$, Input $t_r$, $t_f$ = 10 ns, $C_L$ = 50 pF, $R_L$ = 200kΩ

| CHARACTERISTIC | TEST CONDITIONS $V_{DD}$ (V) | LIMITS CDP1831 Min.† | CDP1831 Typ.* | CDP1831 Max. | CDP1831C Min.† | CDP1831C Typ.* | CDP1831C Max. | UNITS |
|---|---|---|---|---|---|---|---|---|
| Access Time from Address Change, $t_{AA}$ | 5 | — | 850 | 1000 | — | 850 | 1000 | ns |
| | 10 | — | 350 | 400 | — | — | — | |
| Access Time from Chip Select, $t_{ACS}$ | 5 | — | 700 | 800 | — | 700 | 800 | |
| | 10 | — | 250 | 300 | — | — | — | |
| Chip Select Delay, $t_{CS}$ | 5 | — | 600 | — | — | 600 | — | |
| | 10 | — | 200 | 300 | — | — | — | |
| Address Setup Time, $t_{AS}$ | 5 | 50 | — | — | 50 | — | — | |
| | 10 | 25 | — | — | — | — | — | |
| Address Hold Time, $t_{AH}$ | 5 | 150 | — | — | 150 | — | — | |
| | 10 | 75 | — | — | — | — | — | |
| Read Delay, $t_{\overline{MRD}}$ | 5 | — | 300 | 500 | — | 300 | 500 | |
| | 10 | — | 100 | 150 | — | — | — | |
| Chip Enable Output Delay from Address, $t_{CA}$ | 5 | — | 500 | 600 | — | 500 | 600 | |
| | 10 | — | 200 | 250 | — | — | — | |
| Bus Contention Delay, $t_D$ | 5 | — | 200 | 350 | — | 200 | 350 | |
| | 10 | — | 100 | 150 | — | — | — | |
| TPA Pulse Width, $t_{PAW}$ | 5 | 200 | — | — | 200 | — | — | |
| | 10 | 70 | — | — | — | — | — | |

†Time required by a limit device to allow for the indicated function.
*Time required by a typical device to allow for the indicated function. Typical values are for $T_A = 25°C$ and nominal $V_{DD}$

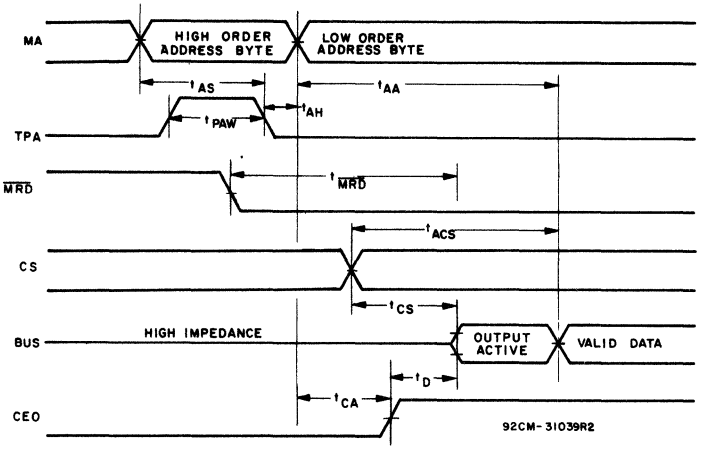



*Fig. 2 - Timing waveforms.*

**Note:**
The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1831. When used directly with a CDP1800-series microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1831 is used with a CDP1800-series microprocessor:

$t_{AH} = 0.5\ t_c$
$t_{PAW} = 1\ t_c$

$\overline{MRD}$ occurs one clock period ($t_c$) earlier than the address bits MA0-MA7.

where $t_c = \frac{1}{\text{CPU clock frequency}}$