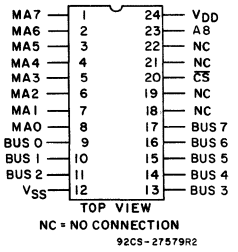
CDP1832, CDP1832C

Product Preview

TERMINAL ASSIGNMENT



512-Word x 8-Bit Static Read-Only Memory

Features:

- *Compatible with CDP1800 and CD4000-series devices*
- *Functional replacement for industry type 2704 512 x 8 EPROM*
- *Three-state outputs*

The RCA CDP1832 and CDP1832C types are 4096-bit mask-programmable CMOS read-only memories organized as 512 words x 8 bits and designed for use in CDP1800-series microprocessor systems.

The CDP1832 ROMs are completely static; no clocks are required.

A Chip-Select input ($\overline{CS}$) is provided for memory expansion. Outputs are enabled when $\overline{CS}$=0.

The CDP1832 is a pin-for-pin compatible replacement for the industry types 2704 EPROM.

The CDP1832C is functionally identical to the CDP1832. The CDP1832 has an operating voltage range of 4 to 10.5 volts, and the CDP1832C has an operating voltage range of 4 to 6.5 volts.

The CDP1832 and CDP1832C are supplied in 24-lead, hermetic, dual-in-line, side-brazed, ceramic packages (D suffix) and in 24-lead dual-in-line plastic packages (E suffix). The CDP1832C is also available in chip form (H suffix).

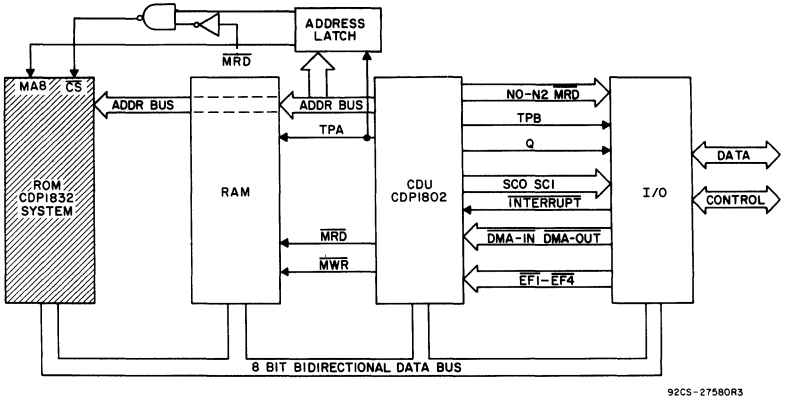


Fig. 1 - Typical CDP1802 microprocessor system.

File Number **1145**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal)
- CDP1832 ..... -0.5 to +11 V
- CDP1832C ..... -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
- For T_A=-40 to +60°C (PACKAGE TYPE E) ..... 500 mW
- For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mV/°C to 200 mW
- For T_A=-55 to +100°C (PACKAGE TYPE D) ..... 500 mW
- For T_A=+100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
- PACKAGE TYPE D ..... -55 to +125°C
- PACKAGE TYPE E ..... -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1832		CDP1832C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

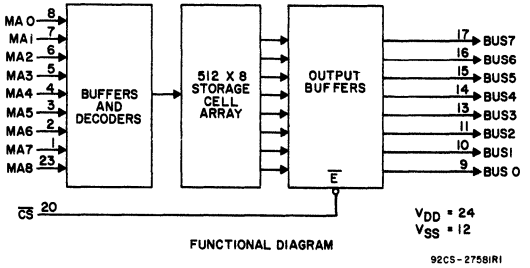


Fig. 2 - Functional diagram.

CDP1832, CDP1832C

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1832			CDP1832C			
	V_O (V) *	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current, I_{DD}	—	5	5	—	0.01	50	—	0.02	200	μA
	—	10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0, 5	5	0.55	—	—	0.55	—	—	mA
	0.5	0, 10	10	1.30	—	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.6	0, 5	5	-0.35	—	—	-0.35	—	—	
	9.5	0, 10	10	-0.65	—	—	—	—	—	
Output Voltage Low-Level, V_{OL}	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current, I_{IN}	Any	0, 5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	μA
	Input	0, 10	10	—	$\pm 10^{-4}$	±2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0, 5	0, 5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	
	0, 10	0, 10	10	—	$\pm 10^{-4}$	±2	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current, I_{DD}†	—	0, 5	5	—	5	10	—	5	10	mA
	—	0, 10	10	—	10	20	—	—	—	

*Typical values are for T_A=25°C and nominal V_{DD}.

†Outputs open-circuited; cycle time=2.5 μs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85°C, V_{DD} ±5%, Input t_r,t_f=10 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1832			CDP1832C			
		Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Access Time From Address Change, t_{AA}	5	—	850	1000	—	850	1000	ns
	10	—	400	500	—	—	—	
Access Time From Chip Select, t_{ACS}	5	—	400	550	—	400	550	
	10	—	200	250	—	—	—	
Chip Select Delay, t_{CS}	5	—	200	250	—	200	250	
	10	—	100	130	—	—	—	

* Time required by a typical device to allow for the indicated function. Typical values are for T_A=25°C and nominal V_{DD}.

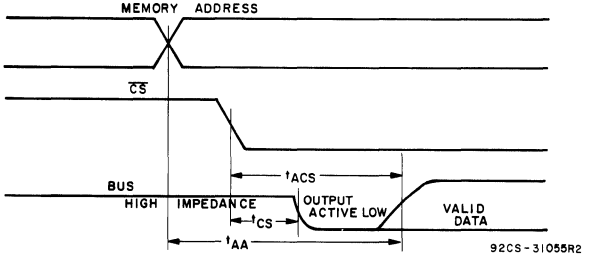


Fig. 3 - Timing waveforms.

6