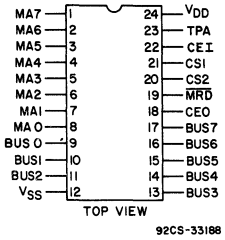
CDP1835C



TERMINAL ASSIGNMENT

CMOS 2048-Word x 8-Bit Static Read-Only Memory

Features:

- *Interfaces with CDP1800-series microprocessors ($f_{clock} \leq 5$ MHz) without additional components*
- *On-chip address latch*
- *On-chip address decoder provides programmable location within 64K memory space*
- *Three-state outputs*

The RCA-CDP1835C is a 16384-bit mask-programmable CMOS read-only memory, organized as 2048 words x 8 bits and is completely static: no clocks required. It will directly interface with CDP1800-series microprocessors that have clock frequencies up to 5 MHz without additional components.

The CDP1835C responds to a 16-bit address multiplexed on 8 address lines. Address latches are provided on-chip to store the 8 most significant bits of the 16-bit address. By mask option, this ROM can be programmed to operate in any 2048-word block of 64K memory space. The polarity of the high address strobe (TPA), $\overline{MRD}$, CEI, CS1, and CS2 are user mask-programmable.

The Chip-Enable output signal (CEO) is "high" when the device is selected. Terminals CEO and CEI can be connected in a daisy chain to control selection of RAM memory in a microprocessor system without additional components.

The CDP1835C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1835C is supplied in 24-lead heremetic dual-in-line side-brazed ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

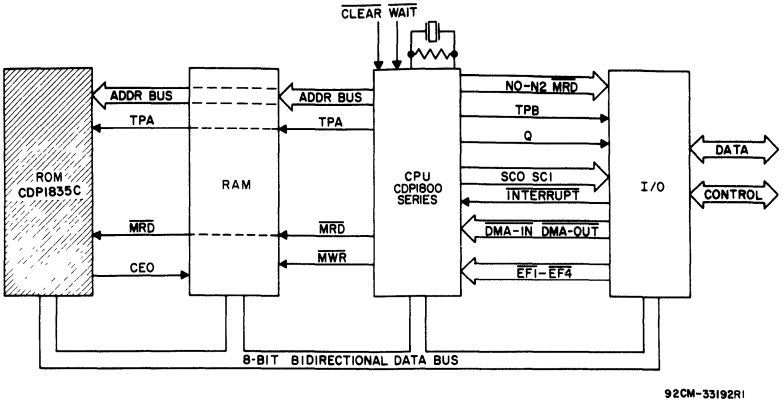


Fig. 1 - Typical CDP1800 Series microprocessor system.

File Number **1267**

MAXIMUM RATING, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(All voltages referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C

OPERATING CONDITIONS at T_A = FULL PACKAGE-TEMPERATURE RANGE

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS CDP1835C		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

6

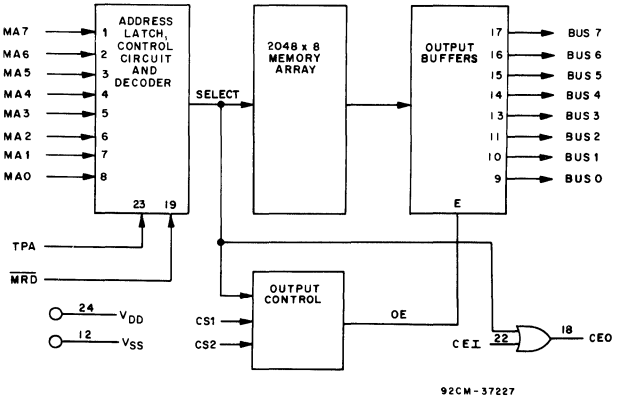


Fig. 2 - Functional block diagram.

CDP1835C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 5%, except as noted

CHARACTERISTIC		CONDITIONS		LIMITS			UNITS
				CDP1835C			
		V_O (V)	V_{IN} (V)	Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	—	0, V_{DD}	—	5	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, V_{DD}	0.8	1.6	—	mA
Output High Drive (Source) Current	I_{OH}	V_{DD} -0.4	0, V_{DD}	-0.8	-1.6	—	
Output Voltage Low-Level	V_{OL}	—	0, V_{DD}	—	0	0.1	V
Output Voltage High-Level	V_{OH}	—	0, V_{DD}	V_{DD} -0.1	V_{DD}	—	
Input Low Voltage	V_{IL}	V_{DD} -0.5	—	—	—	1.5	
Input High Voltage	V_{IH}	V_{DD} -0.5	—	3.5	—	—	
Input Leakage Current (Any Input)	I_{IN}	—	0, V_{DD}	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	0, V_{DD}	0, V_{DD}	—	—	±2	
Operating Device Current	I_{OPER}•	—	0, V_{DD}	—	5	10	mA
Input Capacitance	C_{IN}	—	—	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	10	15	

*Typical values are for T_A = 25° C and nominal V_{DD}.

•Outputs open circuited; cycle time 1 μs.

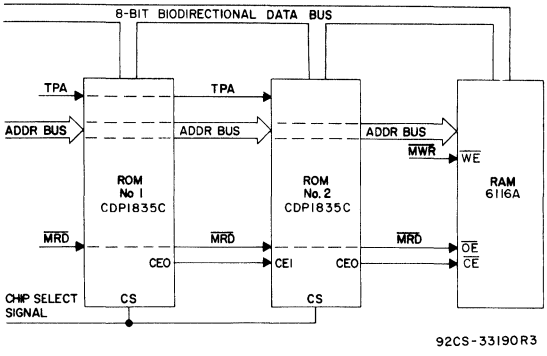


Fig 3 - Typical use of daisy chaining feature of the CDP1835C.

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the above configuration, if ROM No. 1 was masked-programmed for memory locations 0000-07FF$_{16}$ and ROM No. 2 masked-programmed for memory locations 0800$_{16}$-0FFF$_{16}$, for addresses from 0000-0FFF$_{16}$, the RAM would be disabled and one of the ROMs enabled. For locations above 0FFF$_{16}$, the ROM's would be disabled and the RAM enabled.

Signal Descriptions

MA0-MA7: 16-bit multiplexed address inputs. The high-byte address bits are strobed into the on-chip address lath with the trailing edge of TPA. High-byte bits A11, A12, A13, A14 and A15 are polarity mask-programmable for use as chip enable inputs for memory expansion.

$\overline{MRD}$: Memory read input. Controls the output buffers and Chip Enable Output (CEO), and powers down the ROM. $\overline{MRD}$ must be valid on or before the trailing edge of TPA. When $\overline{MRD}$ is not valid, the output buffers are tri-stated. The active polarity of $\overline{MRD}$ is mask-programmable.

CS1, CS2: Mask-programmable chip-select inputs. The chip-select inputs control the data output buffers only (not CEO). The output buffers will be tri-stated when either CS1 or CS2 is not valid

TPA: The trailing edge of TPA is used to latch the high-byte of the 16-bit multiplexed address. The ROM is enabled after the trailing edge of TPA ($\overline{MRD}$ active). The active polarity of TPA is mask-programmable.

CEI, CEO: The Chip Enable Input (CEI), in conjunction with the Chip Enable Output (CEO) can be used in a "Daisy Chain" configuration to avoid memory conflicts between ROM and RAM. CEO is high when the ROM is enabled (i.e., $\overline{MRD}$ is low, TPA toggled) or CEI is active. The active polarity of CEI is mask-programmable.

BUS0-BUS7: 8-Bit Tri-State data bus.

VDD, VSS: Power supply connections

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5V ± 5%
Input t_r, t_f = 10 ns, C_L = 100 pF, and 1 TTL Load

CHARACTERISTIC		LIMITS CDP1835C		UNITS
		Min.	Max.	
Access Time from Address Change	t_{AVQV}	—	500	ns
Chip Select to Output Active	t_{SVQX}	0	200	
Address Setup Time	t_{AS}	50	—	
Address Hold Time	t_{AH}	50	—	
$\overline{MRD}$ Setup Time *	t_{RSU}	0	—	
Chip Enable Output Delay from TPA	t_{CA}	—	125	
Output Delay from TPA	t_D	—	200	
TPA Pulse Width	t_{PAW}	125	—	
Chip Enable In to Chip Enable Out Delay	t_{CEIO}	—	100	
Chip Select to Output Valid	t_{SVQV}	—	200	
Chip Deselect to Output High Z	t_{SXQZ}	—	200	
$\overline{MRD}$ to CEO Low	t_{RXCL}	—	150	
$\overline{MRD}$ to Output High Z	t_{RXQZ}	—	200	

* $\overline{MRD}$ must be valid on or before the trailing edge of TPA. (Output will be tri-stated and the ROM powered down when $\overline{MRD}$ is not valid.)

CDP1835C

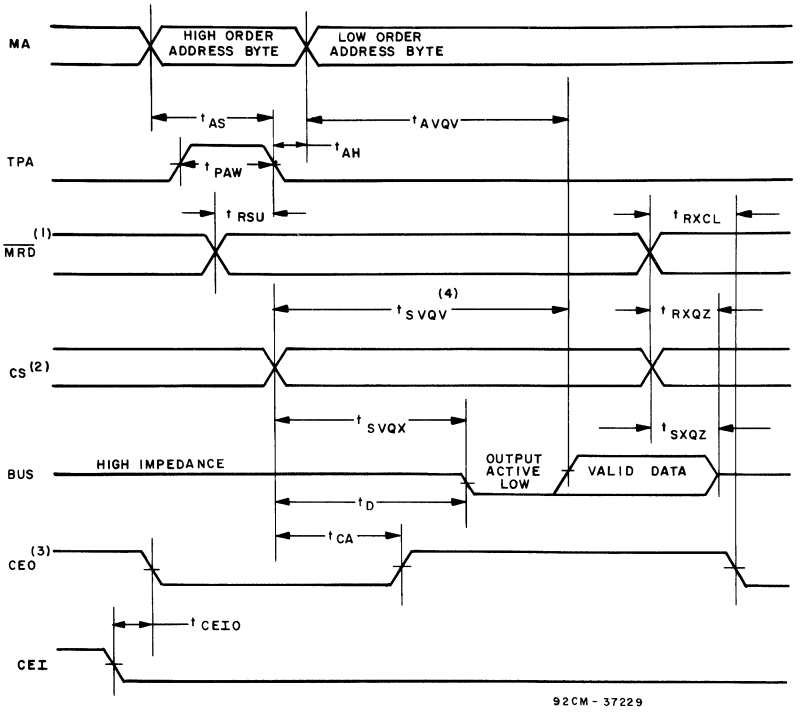


Fig 4 - Timing diagram.

Notes:

(1) $\overline{MRD}$ must be valid on or before the trailing edge of TPA. (Output will be tri-stated and the ROM powered down when $\overline{MRD}$ is not valid.

(2) CS (CS1 and CS2) controls the output buffers only. Output will be tri-stated when either CS1 or CS2 is not valid.

(3) CEO is high when ROM is enabled.

(4) Provided t_{AVQV} is satisfied.