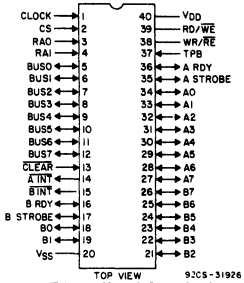
CDP1851, CDP1851C

TERMINAL ASSIGNMENT



40-LEAD DIL PACKAGES

CMOS Programmable I/O Interface

Features:

- *20 Programmable I/O Lines*
- *Programmable for Operation in Four Modes:*
  - *Input*
  - *Output*
  - *Bidirectional*
  - *Bit-programmable*
- *Operates in Either I/O or Memory Space*

The RCA CDP1851 and CDP1851C are CMOS programmable two-port I/Os designed for use as general-purpose I/O devices. They are directly compatible with CDP1800 series microprocessors functioning at maximum clock frequency. Each port can be programmed in either byte-I/O or bit-programmable modes for interfacing with peripheral devices such as printers and keyboards.

Both ports A and B can be separately programmed to be 8 bit input or output ports with handshaking control lines, RDY and STROBE. Only port A can be programmed to be a bidirectional port. This configuration provides a means for communicating with a peripheral device or microprocessor system on a single 8 bit bus for both transmitting and receiving data. Handshaking signals are provided to maintain proper bus access control. Port A handshaking lines are used for input control and port B handshaking lines are used for output; therefore port B must be in the bit-programmable mode where handshaking is not used.

Ports A and B can be separately bit programmed so that each individual line can be designated as an input or output line. The handshaking lines may also be individually programmed as input or output when port A is not in bidirectional mode.

The CDP1851 has a supply-voltage range of 4 to 10.5 V, and the CDP1851C has a range of 4 to 6.5 V Both types are supplied in 40-lead dual-in-line plastic (E suffix) or hermetic ceramic (D suffix) packages. The CDP1851C is also available in chip form (H suffix).

4

CDP1851 Programming Modes

Mode	(8) Port A Data Pins	(2) Port A Handshaking Pins	(8) Port B Data Pins	(2) Port B Handshaking Pins
Input	Accept input data	READY, STROBE	Accept input data	READY, STROBE
Output	Output data	READY, STROBE	Output data	READY, STROBE
Bidirectional (Port A only)	Transfer input/ output data	Input handshaking for Port A	Must be previously set to bit-programmable mode	Output handshaking for Port A
Bit-Programmable	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs	Programmed individually as inputs or outputs

File Number **1056**

CDP1851, CDP1851C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1851 ..... -0.5 to +11 V
CDP1851C ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Lineary at 12 mW/°C to 200 mW
For T_A = -55 to 100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Lineary at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Type) ..... 40 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1851		CDP1851C		
	MIN.	MAX.	MIN.	MAX.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

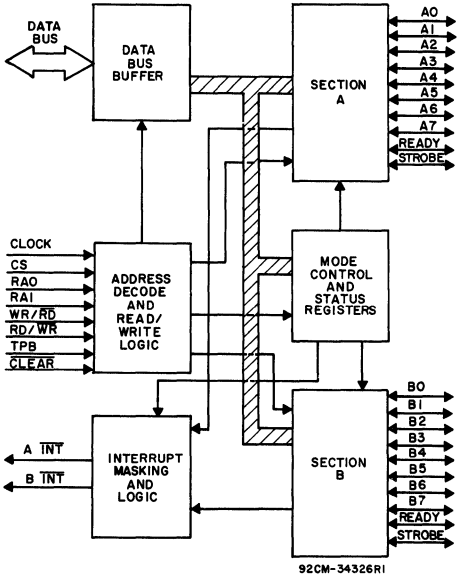


Fig. 1 - Functional diagram for CDP1851 and CDP1851C.

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1851			CDP1851C			
					Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
		—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
		0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	—	-1.15	-2.3	—	
		9.5	0, 10	10	-2.6	-5.2	—	—	—	—	
Output Voltage Low-Level	V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	—	—	1.5	
		0.5, 9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V_{IH}	0.5, 4.5	—	5	3.5	—	—	3.5	—	—	
		0.5, 9.5	—	10	7	—	—	—	—	—	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
			0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	—	±1	—	—	±1	
		0, 10	0, 10	10	—	—	±1	—	—	—	
Operating Current	I_{DD1}Δ	—	0, 5	5	—	1.5	3	—	1.5	3	mA
		—	0, 10	10	—	6	12	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	

•Typical values are for T_A = 25° C and nominal V_{DD}.

‡I_{OL} = I_{OH} = 1 μA.

ΔOperating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

FUNCTIONAL DESCRIPTION

The CDP1851 has four modes of operation: input, output, bidirectional, and bit-programmable. Port A is programmable in all modes; port B is programmable in all but the bidirectional mode. A control byte must be loaded into the control register to program the ports. In the input and output modes, each port has two handshaking signals, STROBE and RDY. In the bidirectional mode, port A has four handshaking signals: A RDY and A STROBE for input, B RDY and B STROBE for output. If port A is programmed in the bidirectional mode, port B must be programmed in the bit-programmable mode. Each terminal of port A or B may be individually programmed for input or output in the bit-programmable mode. Since handshaking is not used in this mode, the RDY and STROBE lines may also be used for bit-programming if port A is not in the bidirectional mode.

Input Mode

When a peripheral device has data to input, it sends a STROBE pulse to the PIO. The leading edge of this pulse clears the RDY line, inhibiting further transmission from the peripheral. The trailing edge of the STROBE pulse latches the data into the PIO buffer register and also activates the $\overline{INT}$ line to signal the CPU to read this data. The $\overline{INT}$ pin can be wired to the $\overline{INT}$ pin of the CPU or the $\overline{EF}$ lines for polling. The CPU then executes an input or a load instruction, depending on the mapping technique used. In either case the proper code must be asserted on the RAO, RA1, and CS lines to read the buffer register (see Table VI).

The $\overline{INT}$ line is deactivated on the leading edge of TPB. The trailing edge of TPB sets the RDY line to signal the peripheral that the port is ready to be loaded with new data. If RDY is low when the input mode is entered (i.e. after a reset), a "dummy" read must be done to set RDY high and signal the peripheral device that the port is ready to be loaded.

CDP1851, CDP1851C

FUNCTIONAL DESCRIPTION (Cont'd)

Output Mode

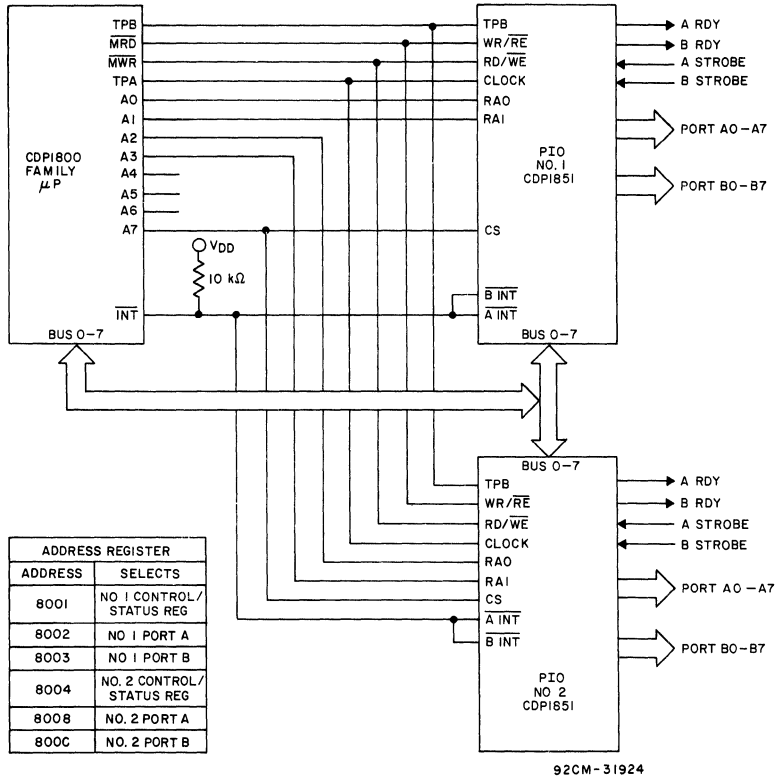
A peripheral STROBE pulse sent to the PIO generates an interrupt to signal the CPU that the peripheral device is ready for data. The CPU executes the proper output or store instruction. Data are than read from memory and placed on the bus. The data are latched into the port buffer at the end of the window when RE/$\overline{WE}$ = 0 and WR/$\overline{RE}$ = 1. The RDY line is also set at this time, indicating to the peripheral that there is data in the port buffer. The $\overline{INT}$ line is deactivated at the beginning of the window. After the peripheral reads valid port data, it can send another STROBE pulse, clearing the RDY line and activating the $\overline{INT}$ line as in the input mode.

Bidirectional Mode

This mode programs port A to function as both an input and output port. The bidirectional feature allows the peripheral to control port direction by using both sets of handshake signals. The port A handshaking pins are used to control input data from peripheral to PIO, while the port B handshaking pins are used to control output data from PIO to peripheral. Data are transferred in the same manner as the input and output modes. Since $\overline{A\ INT}$ is used for both input and output, the status register must be read to determine what condition caused $\overline{A\ INT}$ to be activated (see Table V).

Bit—Programmable Mode

This mode allows individual bits of port A or port B to be programmed as inputs or outputs. To output data to bits programmed as outputs, the CPU loads a data byte into the 8 bit port as in the output mode (no handshaking). Only bits programmed for outputs latch this data. Data must be stable when reading from bits programmed as inputs, since the input bits do not latch. When the CDP1851 inputs data to the CPU the CPU also reads the output bits latched during the last output cycle. The RDY and STROBE lines may be used for I/O by using the STROBE/RDY I/O control byte in table II. An additional feature available in the bit-programmable mode is the ability to generate interrupts based on input/output byte combinations. These interrupts can be programmed to occur on logic conditions (AND, OR, NAND, and NOR) generated by the eight I/O lines of each port (The STROBE and RDY lines cannot generate interrupts).



ADDRESS REGISTER	
ADDRESS	SELECTS
8001	NO 1 CONTROL/ STATUS REG
8002	NO 1 PORT A
8003	NO 1 PORT B
8004	NO. 2 CONTROL/ STATUS REG
8008	NO. 2 PORT A
800C	NO. 2 PORT B

Fig. 2 - Memory space I/O. This configuration allows up to four CDP1851s to occupy memory space 8XXX with no additional hardware (A4 - A5 and A6 - A7 are used as RA0 and RA1 on the third and fourth PIO's).

PROGRAMMING

1. Initialization and Controls

The CDP1851 PIO must be cleared by a low on the CLEAR input during power-on to set it for programming. Once programmed, modes can be changed without clearing except when exiting the bit-programmable mode. A low on the CLEAR input sets both ports to the input modes, disables interrupts, unmasks all bit-programmed interrupt bits, and resets the status register, A RDY, and B RDY.

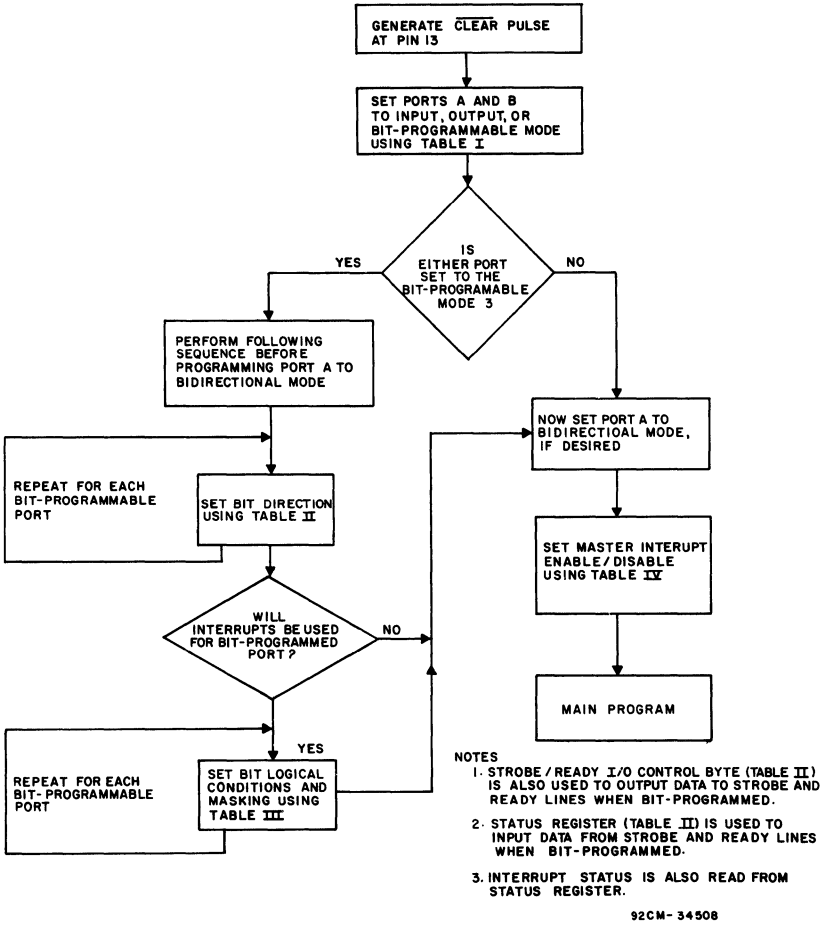
2. Mode Setting

The control register must be sequentially loaded with the appropriate mode set control bytes in order as shown in table I (i.e. input mode then output mode, etc.). Port A is set with the SET A bit = 1 and port B is set with the SET B bit = 1. If a port is set to the bit-programmable mode, the bit-programming control byte from table II must be loaded. A bit is programmed for output with the I/O bit = 1 and for input with the I/O bit = 0. The STROBE and RDY lines may be programmed for input or output with the STROBE/RDY control byte of table II. Input data on the STROBE and RDY lines is detected by reading the status register. When using the STROBE or RDY lines for output, the control byte must be loaded every time output data is to be changed. To program logical conditions that will generate an interrupt, the interrupt control byte of table III must be loaded. An interrupt mask of the eight I/O lines may be loaded next, if bit D4 (mask follows) of the interrupt control byte = 1. The I/O lines are masked if the corresponding bit of the interrupt mask register is 1, otherwise it is monitored. Any combination of masked bits are permissable, except all bits masked (mask = FF).

3. $\overline{\text{INT}}$ Enable/Disable

To enable or disable the $\overline{\text{INT}}$ line in all modes, the interrupt ENABLE/DISABLE byte must be loaded (see Table IV). Interrupts can also be detected by reading the status register see table V. All interrupts should be disabled when programming or false interrupts may occur. The $\overline{\text{INT}}$ outputs are open drain NMOS devices that allow wired ORing (use 10K pull-up registers).

A FLOW CHART GUIDE TO CDP1851 MODE PROGRAMMING



CDP1851, CDP1851C

TABLE I [RA1=0, RA0=1]

MODE SET *	7	6	5	4	3	2	1	0
Input	0	0	X	Set B	Set A	X	1	1
Output	0	1	X	Set B	Set A	X	1	1
Bit-Programmable	1	1	X	Set B	Set A	X	1	1
Bidirectional	1	0	X	X	Set A	X	1	1

* Modes should be set in order as shown in Table I

If either port is set for bit-programmable mode, the two following control bytes should immediately follow:

TABLE II [RA1=0, RA0=1]

Bit-Programming	7	6	5	4	3	2	1	0
	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
STROBE/RDY I/O Control$^{\Delta}$	D7	D6	D5	D4	D3	D2	D1	D0

$^{\Delta}$Output = 1

$^{\Delta}$Input = 0

(D1) 0 = Port A, 1 = Port B

(D2) 0 = No change to RDY line function, 1 = Change per bit (D6)

(D3) 0 = No change to STROBE line function, 1 = Change per bit (D7)

(D4) RDY line output data

(D5) STROBE line output data

(D6) RDY line used as:
Output = 1
Input = 0

(D7) STROBE line used as:
Output = 1
Input = 0

If interrupts will be used for either bit-programmed port, the following control bytes should be loaded:

TABLE III [RA1=0, RA0=1]

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Logical Conditions and Mask	0	D6	D5	D4	D3	1	0	1

(D3) 0 = Port A, 1 = Port B

(D4) 0 = No change in mask, 1 = Mask follows (See TABLE IIIa)

(D5) (D6) 0, 0 = NAND; 1, 0 = OR; 0, 1 = NOR; 1, 1 = AND

TABLE IIIa [RA1=0, RA0=1]

INTERRUPT CONTROL	7	6	5	4	3	2	1	0
Mask Register (If D4 = 1)	B7 Mask	B6 Mask	B5 Mask	B4 Mask	B3 Mask	B2 Mask	B1 Mask	B0 Mask

If Bn Mask = 1 then mask Bit (for n = 0 to 7)

TABLE IV **[RA1=0, RA0=1]**

	7	6	5	4	3	2	1	0
Interrupt Enable/Disable	$\overline{INT}$ Enable	X	X	X	A/B	0	0	1

$\overline{INT}$ Enable = 1, $\overline{INT}$ Enabled
= 0, $\overline{INT}$ Disabled

A/B = 0, Port A
= 1, Port B

TABLE V **[RA1=0, RA0=1]**

	7	6	5	4	3	2	1	0
Status Register	D7	D6	D5	D4	D3	D2	D1	D0

(D0) $\overline{B\ INT}$ status (1 means set) } All Modes
(D1) $\overline{A\ INT}$ status (1 means set) }

(D2) 1 = $\overline{A\ INT}$ was caused by A STROBE } Bidirectional Mode Only
(D3) 1 = $\overline{A\ INT}$ was caused by B STROBE }

(D4) A RDY input data }
(D5) A STROBE input data } Bit-Programmable Mode
(D6) B RDY input data }
(D7) B STROBE input data }

TABLE VI — CPU CONTROLS

CS *	RA1	RA0	RD/$\overline{WE}$	WR/$\overline{RE}$	Action
0	X	X	X	X	No-op bus 3-stated
X	0	0	X	X	No-op bus 3-stated
X	X	X	0	0	No-op bus 3-stated
X	X	X	1	1	No-op bus 3-stated
X	X	X	1	1	No-op bus 3-stated
1	0	1	1	0	Read * status register
1	0	1	0	1	Load control register
1	1	0	1	0	Read * port A
1	1	0	0	1	Load port A
1	1	1	1	0	Read * port B
1	1	1	0	1	Load port B

* Read = RD/$\overline{WE}$ = 1 and WR/$\overline{RE}$ = 0 is latched on trailing edge of CLOCK.

TABLE VII — MEMORY I/O USE

	RD/$\overline{WE}$ Input	WR/$\overline{RE}$ Input	TPB Input	
I/O Space	$\overline{MRD}$	TPB	TPB	PIO Terminals
Memory Space	$\overline{MWR}$	$\overline{MRD}$	TPB	CPU Terminals

FUNCTION PIN DEFINITION

CLOCK (Input):

Positive input pulse that latches READ and CS on its trailing edge.

CS — CHIP SELECT (Input)

A high-level voltage at this input selects the CDP1851 PIO.

RA0 — REGISTER ADDRESS 0 (Input):

This input and RA1 are used to select either the ports or the control/status registers.

RA1 — REGISTER ADDRESS 1 (Input):

See RA0

BUS 0 — BUS 7:

Bidirectional CPU data bus.

$\overline{CLEAR}$ (Input)

A low-level voltage at this input resets both ports to the input mode, and also resets the status register. A RDY, B RDY, and interrupt enable (disabling interrupts).

$\overline{A\ INT}$ — $\overline{A\ INTERRUPT}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table III. This output is an open-drain NMOS device (to allow wired ORing) and must be tied to a pullup resistor, normally 10 kΩ.

CDP1851, CDP1851C

FUNCTION PIN DEFINITION (Cont'd)

$\overline{\text{B INT}}$ — $\overline{\text{B INTERRUPT}}$ (Output):

A low-level voltage at this output indicates the presence of one of the interrupt conditions listed in Table III. This output is also an open-drain NMOS device and must be tied to a pullup resistor.

B RDY — B READY (Output):

This output is a handshaking or data bit I/O line in the bit-programmable mode.

B STROBE (Input):

An input handshaking line for port B in the input and output modes, and for port A when it is in the bidirectional mode. It can be used as a data bit I/O line in the bit-programmable mode except when port A is not programmed as bidirectional.

B 0 — B 7:

Data input or output lines for port B.

V_{SS}:

Ground

A 0 — A 7:

Data input or output lines for port A.

A STROBE (Input):

An input handshaking line for port A in the input, output, and bidirectional modes. It can also be used as a data bit I/O line when port A is in the bit-programmable mode.

A RDY — A READY (Output):

A output handshaking line or data bit I/O line.

TPB (Input):

A positive input pulse used as a data load, set, or reset strobe.

WR/$\overline{\text{RE}}$ — WRITE/$\overline{\text{READ ENABLE}}$ (Input):

A positive input used to write data from the CDP1851 to the CPU bus.

RD/$\overline{\text{WE}}$ — READ/$\overline{\text{WRITE ENABLE}}$ (Input):

A positive input used to read data from the CPU bus to the CDP1851 bus.

V_{DD}:

Positive supply voltage.

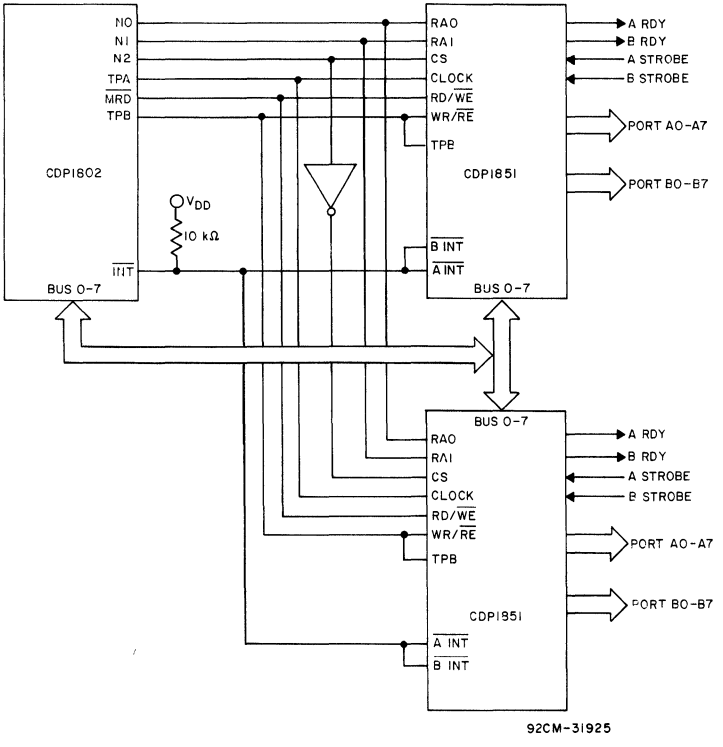


Fig. 3 - I/O space I/O.

CDP1851, CDP1851C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1851			CDP1851C			
			Min.	Typ.•	Max.+	Min.	Typ.•	Max.+	
Input Mode see Figs. 4 and 5									
Minimum Setup Times:		5	—	50	75	—	50	75	ns
Chip Select to CLOCK	t_{CSCL}	10	—	25	40	—	—	—	
		5	—	75	120	—	75	120	
RD/$\overline{WE}$ to CLOCK	t_{RWCL}	10	—	40	60	—	—	—	
		5	—	75	120	—	75	120	
WR/$\overline{RE}$ to CLOCK	t_{WRCL}	10	—	40	60	—	—	—	
		5	—	75	120	—	75	120	
Data in to STROBE	t_{DIST}	10	—	40	60	—	—	—	
Minimum Hold Times:		5	—	75	120	—	75	120	
Chip Select After CLOCK	t_{HCSCL}	10	—	40	60	—	—	—	
		5	—	-50	0	—	-50	0	
Address After TPB	T_{HATPB}	10	—	-25	0	—	—	—	
		5	—	50	75	—	50	75	
Data In After STROBE	t_{HSTDI}	10	—	25	40	—	—	—	
		5	50	325	500	50	325	500	
Data Bus Out After Address	t_{HADOH}	10	25	165	250	—	—	—	
Propagation Delay Times:		5	—	200	300	—	200	300	
TPB to $\overline{INT}$	t_{PINT}	10	—	100	150	—	—	—	
		5	—	200	300	—	200	300	
STROBE to $\overline{INT}$	t_{STINT}	10	—	100	150	—	—	—	
		5	—	250	375	—	250	375	
TPB to RDY	t_{TPRDY}	10	—	125	200	—	—	—	
		5	—	260	400	—	260	400	
STROBE to RDY	t_{STRDY}	10	—	130	200	—	—	—	
Minimum Pulse Widths:		5	—	75	120	—	75	120	
CLOCK	t_{WCL}	10	—	40	60	—	—	—	
		5	—	75	120	—	75	120	
TPB	t_{WTPB}	10	—	40	60	—	—	—	
		5	—	100	150	—	100	150	
STROBE	t_{WST}	10	—	50	75	—	—	—	
Access Time, Address to Data		5	—	325	500	—	325	500	
Bus Out	t_{ADA}	10	—	165	250	—	—	—	

•Typical values are for T_A = 25°C and nominal voltages.

+Maximum limits of minimum characteristics are the values above which all devices function.

CDP1851, CDP1851C

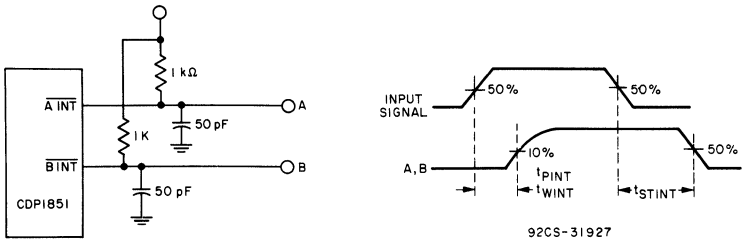


Fig. 4 - Interrupt signal propagation delay time test circuit and waveforms.

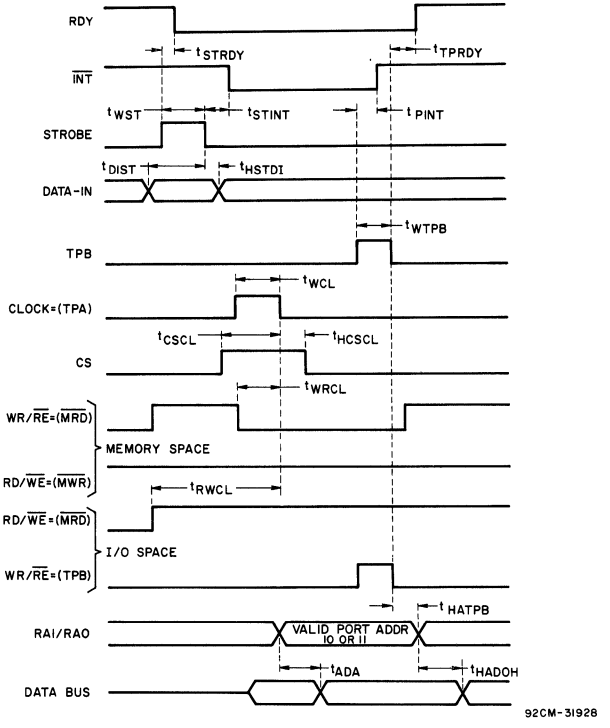


Fig. 5 - Input mode timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC		V_{DD} (V)	Min.	LIMITS CDP1851 Typ.•	CDP1851 Max.+	CDP1851C Min.	CDP1851C Typ.•	CDP1851C Max.+	UNITS
Output Mode see Figs. 4 and 6									
Minimum Setup Times:		5	—	50	75	—	50	75	ns
Chip Select to CLOCK	t_{CSCL}	10	—	25	40	—	—	—	
		5	—	75	120	—	75	120	
RD/$\overline{WE}$ to CLOCK	t_{RWCL}	10	—	40	60	—	—	—	
		5	—	75	120	—	75	120	
WR/$\overline{RE}$ to CLOCK	t_{WRCL}	10	—	40	60	—	—	—	
		5	—	50	75	—	50	75	
Address to WRITE *	t_{AW}	10	—	25	40	—	—	—	
		5	—	80	120	—	80	120	
Data Bus to WRITE *	t_{DW}	10	—	40	60	—	—	—	
Minimum Hold Times:		5	—	75	120	—	75	120	
Chip Select After CLOCK	t_{HCSCL}	10	—	40	60	—	—	—	
		5	—	50	75	—	50	75	
Address After WRITE *	t_{HAW}	10	—	25	40	—	—	—	
		5	—	50	75	—	50	75	
Data Bus After WRITE *	t_{HDW}	10	—	25	40	—	—	—	
Propagation Delay Times:		5	—	225	350	—	225	350	
WRITE * to Data Out	t_{WDO}	10	—	125	200	—	—	—	
		5	—	300	450	—	300	450	
WRITE * to $\overline{INT}$	t_{WINT}	10	—	150	225	—	—	—	
		5	—	350	525	—	350	525	
WRITE * to RDY	t_{WRDY}	10	—	175	275	—	—	—	
		5	—	200	300	—	200	300	
STROBE to $\overline{INT}$	t_{STINT}	10	—	100	150	—	—	—	
		5	—	260	400	—	260	400	
STROBE to RDY	t_{STRDY}	10	—	130	200	—	—	—	
Minimum Pulse Widths:		5	—	75	120	—	75	120	
CLOCK	t_{WCL}	10	—	40	60	—	—	—	
		5	—	100	150	—	100	150	
STROBE	t_{WST}	10	—	50	75	—	—	—	
		5	—	175	275	—	175	275	
WRITE *	t_{WW}	10	—	90	150	—	—	—	

* WRITE is the overlap of RD/$\overline{WE}$ = 0 and WR/$\overline{RE}$ = 1.

•Typical values are for T_A = 25° C and nominal voltages.

+Maximum limits of minimum characteristics are the values above which all devices function.

CDP1851, CDP1851C

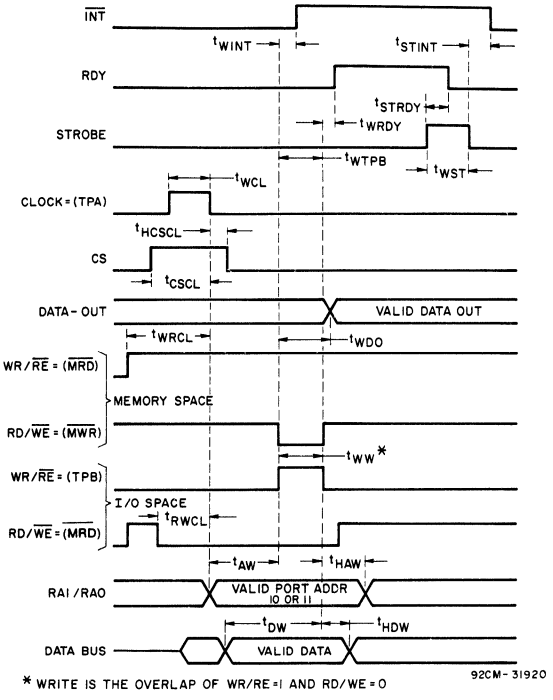


Fig. 6 - Output mode timing waveforms.