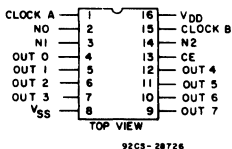


CDP1853, CDP1853C

TERMINAL ASSIGNMENT



N-Bit 1 of 8 Decoder

Features:

- Provides direct control of up to 7 input and 7 output devices
- CHIP ENABLE (CE) allows easy expansion for multi-level I/O systems

The RCA-CDP1853 and CDP1853C are 1 of 8 decoders designed for use in general purpose microprocessor systems. These devices, which are functionally identical, are specifically designed for use as gated N-bit decoders and interface directly with the 1800-series microprocessors without additional components. The CDP1853 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1853C has a recommended operating voltage range of 4 to 6.5 volts.

When CHIP ENABLE (CE) is high, the selected output will be true (high) from the trailing edge of CLOCK A (high-to-low transition) to the trailing edge of CLOCK B (high-to-low transition). All outputs will be low when the device is not

selected (CE=0) and during conditions of CLOCK A and CLOCK B as shown in Fig. 2. The CDP1853 inputs N0, N1, N2, CLOCK A, and CLOCK B are connected to an 1800 series microprocessor outputs N0, N1, N2, TPA, and TPB respectively, when used to decode I/O commands as shown in Fig. 5. The CHIP ENABLE (CE) input provides the capability for multiple levels of decoding as shown in Fig. 6.

The CDP1853 can also be used as a general 1 of 8 decoder for I/O and memory system applications as shown in Fig. 4.

The CDP1853 and CDP1853C are supplied in hermetic 16-lead dual-in-line ceramic (D suffix) and plastic (E suffix) packages.



TRUTH TABLE

CE	CL A	CL B	EN
1	0	0	Qn-1*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

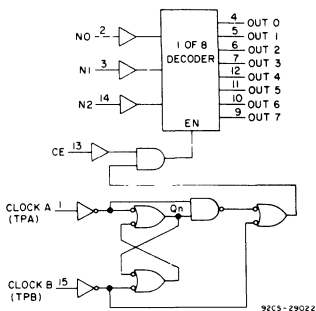


Fig. 1 - CDP1853 functional diagram.

N2	N1	N0	EN	0	1	2	3	4	5	6	7
0	0	0	1	1	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	0	0	0	0
1	0	0	1	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0	0

1 = High level 0 = Low level X = Don't care
 *Qn-1 = Enable remains in previous state.

CDP1853, CDP1853C

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 (All voltage values referenced to V_{SS} terminal)

CDP1853 -0.5 to +11 V
 CDP1853C -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} + 0.5 V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA†

OPERATING-TEMPERATURE RANGE (T_A):

CERAMIC PACKAGES (D SUFFIX TYPES) -55 to +125°C
 PLASTIC PACKAGES (E SUFFIX TYPES) -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
 At distance 1/16 ±1/32 inch (1.59±0.79 mm) from case for 10 s max. +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C. Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	CDP1853			CDP1853C			
				Min.	Typ. †	Max.	Min.	Typ. †	Max.	
Quiescent Device Current, I _L	-	-	5	-	1	10	-	5	50	μA
	-	-	10	-	10	100	-	-	-	
Output Low Drive (Sink) Current, I _{OL}	0.4	0.5	5	1.6	3.2	-	1.6	3.2	-	mA
	0.5	0,10	10	2.6	5.2	-	-	-	-	
Output High Drive (Source Current) I _{OH}	4.6	0.5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
	9.5	0,10	10	-2.6	-5.2	-	-	-	-	
Output Voltage Low-Level ▲ V _{OL}	-	0.5	5	-	0	0.1	-	0	0.1	V
	-	0,10	10	-	0	0.1	-	-	-	
Output Voltage High Level V _{OH}	-	0.5	5	4.9	5	-	4.9	5	-	V
	-	0,10	10	9.9	10	-	-	-	-	
Input Low Voltage V _{IL}	0.5,4.5	-	5	-	-	1.5	-	-	1.5	V
	1,9	-	10	-	-	3	-	-	-	
Input High Voltage V _{IH}	0.5,4.5	-	5	3.5	-	-	3.5	-	-	V
	1,9	-	10	7	-	-	-	-	-	
Input Leakage Current I _{IN}	Any	0.5	5	-	-	±1	-	-	±1	μA
	0,10	0,10	10	-	-	±1	-	-	-	
Operating Current I _{DD1} *	0.5	0.5	5	-	50	100	-	50	100	μA
	0,10	0,10	10	-	150	300	-	-	-	
Input Capacitance C _{IN}	-	-	-	-	5	7.5	-	5	7.5	ρF
Output Capacitance C _{OUT}	-	-	-	-	10	15	-	10	15	ρF

† Typical values are for T_A = 25°C and nominal voltage.

* Operating current measured in a CDP1802 system at 2MHz with outputs floating.

▲ I_{OL} = I_{OH} = 1 μA

CDP1853, CDP1853C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1853		CDP1853C		
	Min.	Max.	Min.	Max.	
Supply-Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	VSS	VDD	VSS	VDD	V

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} \pm 5\%$, $V_{IH} = 0.7 V_{DD}$, $V_{IL} = 0.3 V_{DD}$, $t_r, t_f = 20$ ns, $C_L = 100$ pF

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		CDP1853		CDP1853C		
		Typ.	Max.	Typ.	Max.	
Propagation Delay Time: CE to Output, t_{EOH} , t_{EOL}	5	175	275	175	275	ns
	10	90	150	—	—	
N to Outputs, t_{NOH} , t_{NOL}	5	225	350	225	350	ns
	10	120	200	—	—	
Clock A to Output, t_{AO}	5	200	300	200	300	ns
	10	100	150	—	—	
Clock B to Output, t_{BO}	5	175	275	175	275	ns
	10	90	150	—	—	
Minimum Pulse Widths: Clock A, t_{CACA}	5	50	75	50	75	ns
	10	25	50	—	—	
Clock B, t_{CBCB}	5	50	75	50	75	
	10	25	50	—	—	

Note 1: Maximum limits of minimum characteristics are the values above which all devices function.

Note 2: Typical values are for $T_A = 25^\circ\text{C}$ and nominal voltages.

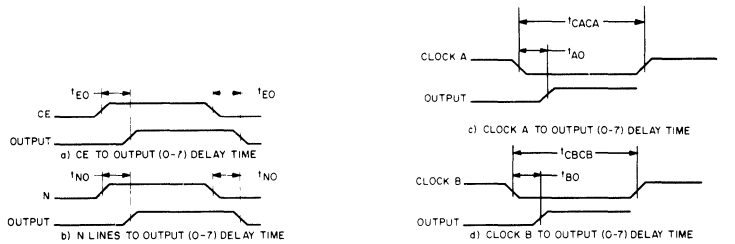
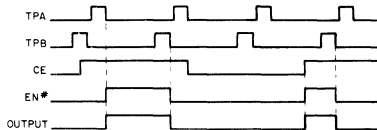


Fig 2 – Propagation delay time diagrams.



* OUTPUT ENABLED WHEN EN = HIGH
INTERNAL SIGNAL SHOWN FOR REFERENCE ONLY (SEE FIG 1)

Fig. 3 – Timing diagram.

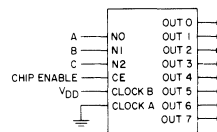


Fig. 4 – N-bit decoder used as a 1 of 8 decoder.

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CDP1853, CDP1853C

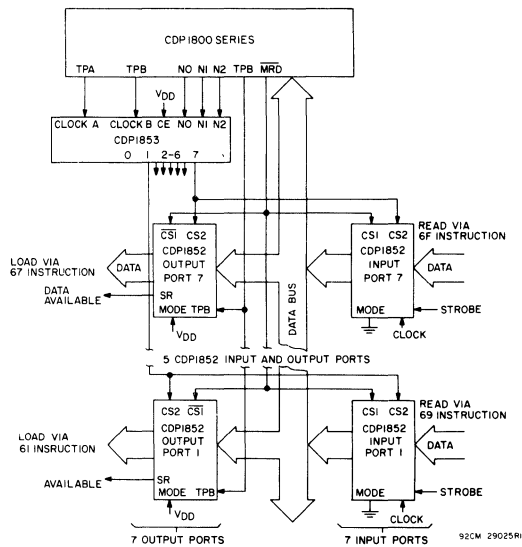


Fig. 5 - N-bit decoder in a one-level I/O system.

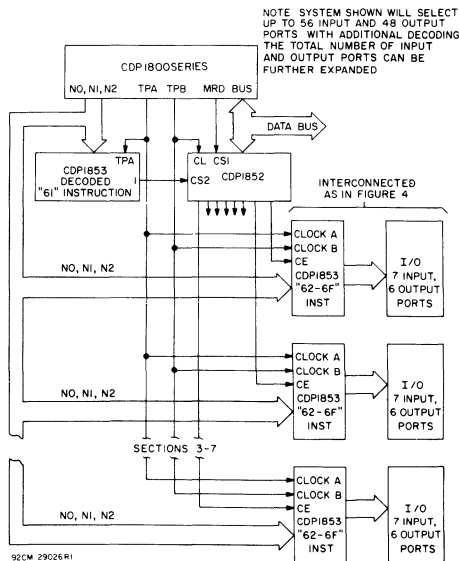


Fig. 6 - Two-level I/O using CDP1853 and CDP1852.