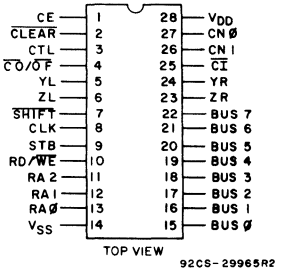
CDP1855, CDP1855C



8-Bit Programmable Multiply/Divide Unit

Features:

- *Cascadable up to 4 units for 32-bit by 32-bit multiply or 64 ÷ 32 bit divide*
- *8-bit by 8-bit multiply or 16 ÷ 18 bit divide in 5.6 μs at 5 V or 2.8 μs at 10 V*
- *Direct interface to CDP1800 series microprocessors*
- *Easy interface to other 8-bit microprocessors*
- *Significantly increases throughput of microprocessor used for arithmetic calculations*

TERMINAL ASSIGNMENT

The RCA-CDP1855 and CDP1855C are CMOS 8-bit multiply/divide units which can be used to greatly increase the capabilities of 8-bit microprocessors. They perform multiply and divide operations on unsigned, binary operators. In general, microprocessors do not contain multiple or divide instructions and even efficiently coded multiply or divide subroutines require considerable memory and execution time. These multiply/divide units directly interface to the CDP1800 series microprocessors via the N-lines and can easily be configured to fit in either the memory or I/O space of other 8-bit microprocessors.

The multiple/divide unit is based on a method of multiplying by add and shift right operations and dividing by subtract and shift left operations. The device is structured to permit cascading identical units to handle operands up to 32 bits.

The CDP1855 and CDP1855C are functionally identical. They differ in that the CDP1855 has a recommended operating voltage range of 4 - 10.5 volts, and the CDP1855C, a recommended operating voltage range of 4 - 6.5 volts.

The CDP1855 and CDP1855C types are supplied in a 28-lead hermetic dual-in-line ceramic package (D suffix) and in a 28-lead dual-in-line plastic package (E suffix). The CDP1855C is also available in chip form (H suffix).

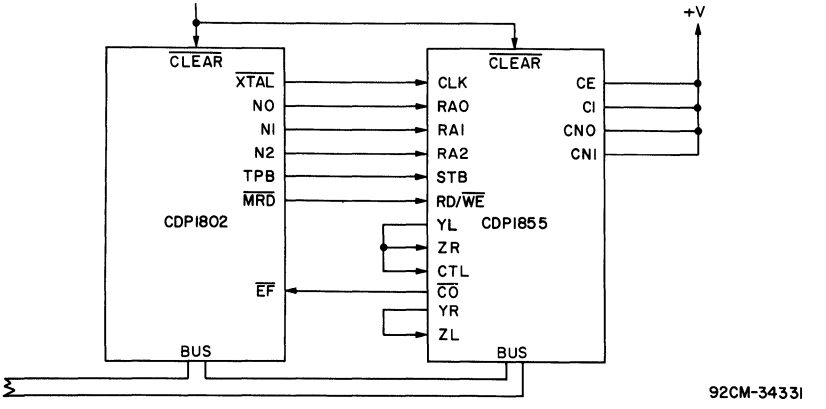


Fig. 1 - Circuit configuration for MDU addressed as an I/O device.

File Number **1053**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1855 ..... -0.5 to +11 V
CDP1855C ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Lineary at 12 mW/°C to 200 mW
For T_A = -55 to 100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE D) ..... Derate Lineary at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1855 Min.	LIMITS CDP1855 Typ.•	LIMITS CDP1855 Max.	LIMITS CDP1855C Min.	LIMITS CDP1855C Typ.•	LIMITS CDP1855C Max.	UNITS
Quiescent Device Current	I_{DD}	— —	0, 5 0, 10	5 10	— —	0.01 1	50 200	— —	0.02 —	200 —	μA
Output Low Drive (Sink) Current	I_{OL}	0.4 0.5	0, 5 0, 10	5 10	1.6 2.6	3.2 5.2	— —	1.6 —	3.2 —	— —	mA
Output High Drive (Source) Current	I_{OH}	4.6 9.5	0, 5 0, 10	5 10	-1.15 -2.6	-2.3 -5.2	— —	-1.15 —	-2.3 —	— —	mA
Output Voltage Low-Level	V_{OL}‡	— —	0, 5 0, 10	5 10	— —	0 0	0.1 0.1	— —	0 —	0.1 —	V
Output Voltage High Level	V_{OH}‡	— —	0, 5 0, 10	5 10	4.9 9.9	5 10	— —	4.9 —	5 —	— —	V
Input Low Voltage	V_{IL}	0.5, 4.5 0.5, 9.5	— —	5 10	— —	— —	1.5 3	— —	— —	1.5 —	V
Input High Voltage	V_{IH}	0.5, 4.5 0.5, 9.5	— —	5 10	3.5 7	— —	— —	3.5 —	— —	— —	V
Input Leakage Current	I_{IN}	— —	0, 5 0, 10	5 10	— —	— —	±1 ±1	— —	— —	±1 —	μA
3-State Output Leakage Current	I_{OUT}	0, 5 0, 10	0, 5 0, 10	5 10	— —	— —	±1 ±10	— —	— —	±1 —	μA
Operating Current	I_{DD1}#	— —	0, 5 0, 10	5 10	— —	1.5 6	— 12	— —	1.5 —	3 —	mA
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	pF

•Typical values are for T_A = 25°C and nominal V_{DD}.

#Operating current is measured at 3.2 MHz with open outputs.

‡I_{OL} = I_{OH} = 1 μA.

CDP1855, CDP1855C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS CDP1855 Min.	LIMITS CDP1855 Max.	LIMITS CDP1855C Min.	LIMITS CDP1855C Max.	UNITS
DC Operating Voltage Range	—	4	10.5	4	6.5	V
Input Voltage Range	—	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
Maximum Input Clock Frequency	5	3.2	—	3.2	—	MHz
	10	6.4	—	—	—	
Minimum 8 x 8 Multiply (16 ÷ 8 Divide) Time	5	—	5.6	—	5.6	μs
	10	—	2.8	—	—	

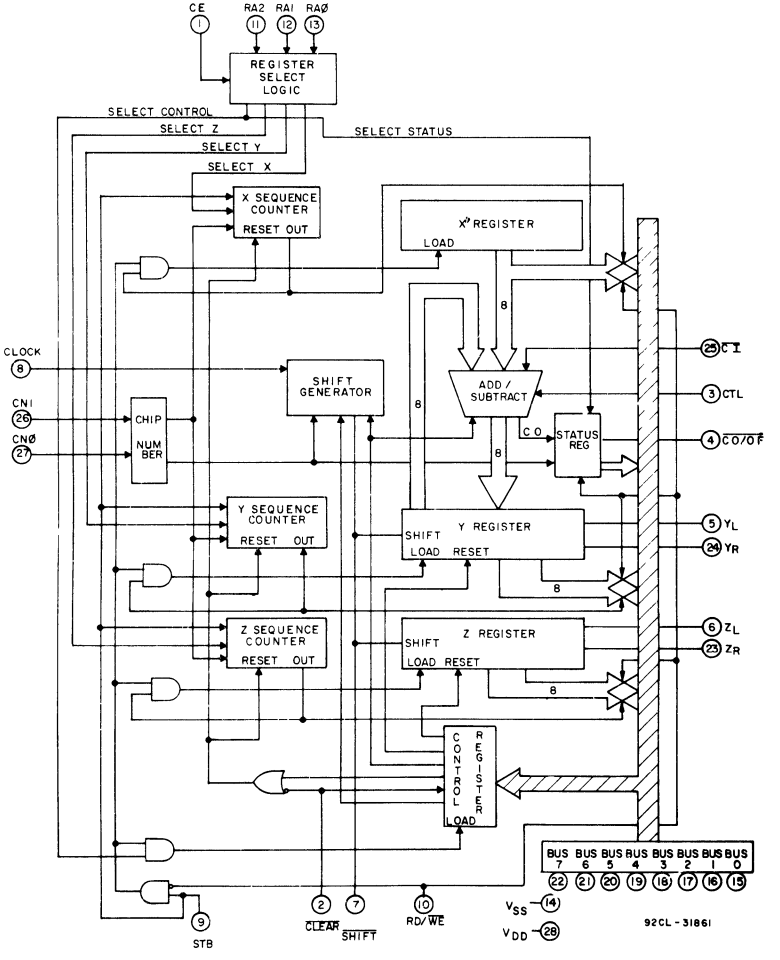


Fig. 2 - Block diagram of CDP1855 and CDP1855C.

FUNCTIONAL DESCRIPTION

The CDP1855 is a multiply-divide unit (MDU) designed to be compatible with CDP1800 series microprocessor systems. It can, in fact, be interfaced to most 8-bit microprocessors (see Fig. 5). The CDP1855 performs binary multiply or divide operations as directed by the microprocessor. It can do a 16N-bit by 8N-bit divide yielding an 8N-bit result plus and 8N-bit remainder. The multiply is an 8N-bit by 8N-bit operation with a 16N-bit result. The "N" represent the number of cascaded CDP1855's and can be 1, 2, 3 or 4. All operations require 8N + 1 shift pulses (See "DELAY NEEDED WITH AND WITHOUT PRESCALER" Pg. 7).

The CDP1855 contains three registers, X, Y, and Z, which are loaded with the operands prior to an operation and contain the results at the completion. In addition, the control register must be loaded to initiate a multiply or divide There is also a status register which contains an overflow flag as shown in the "CONTROL REGISTER BIT ASSIGNMENT TABLE" The register address lines (RA0-RA1) are used to select the appropriate register for loading or reading. The RD/$\overline{WE}$ and STB lines are used in conjunction with the RA lines to determine the exact MDU response (See "CONTROL TRUTH TABLE")

When multiple MDU's are cascaded, the loading of each register is done sequentially. For example, the first selection of register X for loading loads the most significant CDP1855, the second loads the next significant, and so on. Registers are also read out sequentially. This is accomplished by internal counters on each MDU which are decremented by STB during each register selection. When the counter matches the chip number (CN1, CN0 lines), the device is selected. These counters must be cleared with a clear on pin 2 or with bit 6 in the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE") in order to start each sequence of accesses with the most significant device.

The CDP1855 has a built in clock prescaler which can be selected via bit 7 in the control register. The prescaler may be necessary in cascaded systems operating at high frequencies or in systems where a suitable clock frequency is not readily available. Without the prescaler select, the shift frequency is equal to the clock input frequency. With the prescaler selected, the rate depends on the number of MDU's as defined by bits 4 and 5 of the control word (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

1. For one MDU, the clock frequency is divided by 2.
2. For two MDU's the clock frequency is divided by 4.
3. For 3 or 4 MDU's, the clock frequency is divided by 8.

OPERATION

1. Initialization and Controls

The CDP1855 must be cleared by a low on pin 2 during power-on which prevents bus contention problems at the Y_L, Y_R and Z_L, Z_R terminals and also resets the sequence counters and the shift pulse generator.

Prior to loading any other registers the control register must be loaded to specify the number of MDU's being used (See "CONTROL REGISTER BIT ASSIGNMENT TABLE").

Once the number of devices has been specified and the sequence counters cleared with a clear pulse or bit 6 of the control word, the X, Y, and Z registers can be loaded as defined in the "CONTROL TRUTH TABLE". All bytes of the X register can be loaded, then all bytes of the Y, and then all bytes of the Z, or they can be loaded randomly. Succcessive loads to a given register will always proceed sequentially from the most significant byte to the least significant byte, as previously described Resetting the sequence counters select the most significant MDU. In a four MDU system, loading all MDU's results in the sequence counter pointing to the first MDU again In all other configurations (1, 2, or 3 MDU's), the sequence counter must be reset prior to each series of register reads or writes.

2. Divide Operation

For the divide operation, the divisor is loaded in the X register The dividend is loaded in the Y and Z registers with the more significant half in the Y register and the less significant half in the Z register. These registers may be loaded in any order, and after loading is completed, a control word is loaded to specify a divide operation and the number of MDU's and also to reset the sequence counters and Y or Z register and select the clock option if desired. Clearing the sequence counters with bit 6 will set the MDU's up for reading the results.

The X register will be unaltered by the operation. The quotient will be in the Z register while the remainder will be in the Y register. An overflow will be indicated by the $\overline{CO/OF}$ of the most significant MDU and can also be determined by reading the status byte

While the CDP1855 is specified to perform 16 by 8-bit divides, if the quotient of a divide operation exceeds the size of the Z register(s) (8N-bits - where N is the number of cascaded CDP1855's) the overflow bit in the Status Register will be set. Neither the quotient in Z nor the remainder in Y will represent a valid answer This will always be the result of a division performed when the divisor (X) is equal to or less than the most significant 8N-bits of the dividend (Y)

The MDU can still be used for such computations if the divide is done in two steps The dividend is split into two parts—the more significant 8N-bits and the less significant 8N-bits—and a divide done on each part Each step yields an 8N-bit result for a total quotient of 16N-bits.

The first step consists of dividing the more significant 8N-bits by the divisor This is done by clearing the Y register(s), loading the Z register(s) with the more significant 8N-bits of the dividend, and loading the X register(s) with the divisor A division is performed and the resultant value in Z represents the more significant 8N-bits of the final quotient The Z register(s) value must be unloaded and saved by the processor

A second division is performed using the remainder from the first division (in Y) as the more significant 8N-bits of the dividend and the less significant half of the original dividend loaded into the Z register The divisor in X remains unaltered and is, by definition, larger than the remainder from the first division which is in Y The resulting value in Z becomes the less significant 8N-bits of the final quotient and the value in Y is, as usual, the remainder

Extending this technique to more steps allows division of any size number by an 8N-bit divisor

Note that division by zero is never permitted and must be tested for and handled in software

The following example illustrates the use of this algorithm

Example:
Assume three MDU's capable of a by 24-bit division The problem is to divide 00F273,491C06H by 0003B4H

Step 1	000000	,	00F273	/	0003B4	=	000041	R=0001BF	
	Y		Z(MS)		X		Z1	Y1	
Step 2	0001BF	,	491C06	/	0003B4	=	78C936	R=00000E	
	Y1		Z(LS)		X		Z2	Y2	
Result:	000041	,	78C936		R=00000E				
	Z1		Z2		Y2				

4

OPERATION (Cont'd)

The Z register can simply be reset using bit 2 of the control word and another divide can be done in order to further divide the remainder.

3. Multiply Operation

For a multiply operation the two numbers to be multiplied are loaded in the X and Z registers The result is in the Y and Z register with Y being the more significant half and Z the less significant half. The X register will be unchanged after the operation is completed

The original contents of the Y register are added to the product of X and Z Bit 3 of the control word will reset register Y to 0 if desired.

FUNCTIONAL DESCRIPTION OF CDP1855 TERMINALS

CE - CHIP ENABLE (Input):

A high on this pin enables the CDP1855 MDU to respond to the select lines. All cascaded MDU's must be enabled together. CE also controls the tristate $\overline{C.O./O.F.}$, output of the most significant MDU.

$\overline{CLEAR}$ (Input):

The CDP1855 MDU(s) must be cleared upon power-on with a low-on this pin. The clear signal resets the sequence counters, the shift pulse generator, and bits 0 and 1 of the control register.

CTL — CONTROL (Input):

This is an input pin. All CTL pins must be wired together and to the Y_L of the most significant CDP1855 MDU and to the Z_R of the least significant CDP1855 MDU. This signal is used to indicate whether the registers are to be operated on or only shifted.

$\overline{C.O./O.F.}$ — $\overline{CARRY\ OUT/OVER\ FLOW}$ (Output):

This is a tristate output pin. It is the CDP1855 $\overline{Carry\ Out}$ signal and is connected to $\overline{CI}$ ($\overline{CARRY\text{-}IN}$) of the next more significant CDP1855 MDU, except for on the most significant MDU. On that MDU it is an overflow indicator and is enabled when chip enables is true. A low on this pin indicates that an overflow has occured. The overflow signal is latched each time the control register is loaded, but is only meaningful after a divide command.

Y_L, Y_R — Y-LEFT, Y-RIGHT:

These are tristate bi-directional pins for data transfer between the Y registers of cascaded CDP1855 MDU's. The Y_R pin is an output and Y_L is an input during a multiply and the reverse is true at all other times. The Y_L pin must be connected to the Y_R pin of the next more significant MDU. An exception is that the Y_L pin of the most significant CDP1855 MDU must be connected to the Z_R pin of the least significant MDU and to the CTL pins of all MDU's. Also the Y_R pin of the least significant MDU is tiexd to the Z_L pin of the most significant MDU.

Z_L, Z_R — Z-LEFT, Z-RIGHT:

These are tristate bi-directional pins for data transfers between the "Z" registers of cascaded MDU's. The Z_R pin is an output and Z_L is an input during a multiply and the reverse is true at all other times. The Z_L pin must be tied to the Y_R pin of the next more significant MDU. An exception is that the Z_L pin of the most significant MDU must be connected to the Y_R pin of the least significant MDU. Also, the Z_R pin of the least significant MDU is tied to the Y_L of the most significant MDU.

$\overline{SHIFT}$ — $\overline{SHIFT\ CLOCK}$:

This is a tristate bi-directional pin. It is an output on the most significant MDU. And an input on all other MDU's. It provides the MDU system timing pulses. All $\overline{SHIFT}$ pins must be connected together for cascaded operation. A maximum of the 8N +1 shifts are required for an operation where "N" equals the number of MDU devices that are cascaded.

CLK — CLOCK (Input):

This pin should be grounded on all but the most significant MDU. There is an optional reduction of clock frequency available on this pin if so desired, controlled by bit 7 of the control byte.

STB — STROBE (Input):

When RD/WE is low data is latched from bus lines on the falling edge of this signal. It may be asynchronous to the clock. Strobe also increments the selected register's sequence counter during reads and writes. TPB would be used in CDP1800 systems.

RD/$\overline{WE}$ — READ/$\overline{WRITE\ ENABLE}$ (Input):

This signal defines whether the selected register is to be read from or written to. In 1800 systems use $\overline{MRD}$ if MDU's are addressed as I/O devices, $\overline{MWR}$ is used if MDU's are addressed as memory devices.

RA2, RA1, RA0 — REGISTER ADDRESS (Input):

These input signals define which register is to be read from or written to. It can be seen in the "CONTROL TRUTH TABLE" that RA2 can be used as a chip enable. It is identifical to the CE pin, except only CE controls the tristate $\overline{C.O./O.F.}$ on the most significant MDU. In 1800 systems use N lines if MDU's are used as I/O devices, use address lines or function of address lines if MDU's are used as memory devices.

BUS 0 — BUS 7 - BUS LINES:

Tristate bi-directional bus for direct interface with CDP1800 series and other 8-bit microprocessors.

Z_R — Z-RIGHT:

See Pin 6.

Y_R — Y-RIGHT:

See Pin 5.

$\overline{CI}$ — $\overline{CARRY}$ IN (Input):

This is an input for the carry from the next less significant MDU. On the least significant MDU it must be high (V_{DD}) on all others it must be connected to the $\overline{CO}$ pin of the next less significant MDU

CN1, CN0 — CHIP NUMBER (Input):

These two input pins are wired high or low to indicate the MDU position in the cascaded chain. Both are high for the most significant MDU regardless of how many CDP1855 MDU's are used. Then CN1 = high and CN0 = low for the next MDU and so forth.

V_{SS} — GROUND:

Power supply line.

V_{DD} — V+

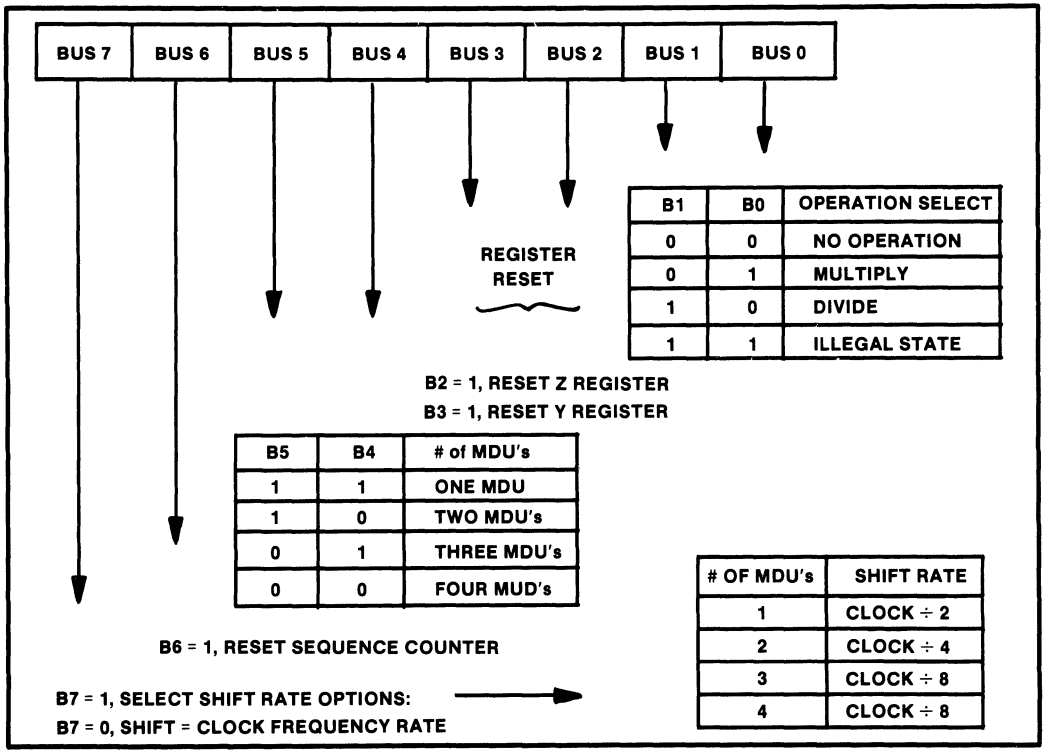
Power supply line.

CONTROL TRUTH TABLE

INPUTS*						RESPONSE
CE	RA2 (N2)	RA1 (N1)	RA0 (N0)	RD/$\overline{WE}$ (MRD)	STB (TPB)	
0	X	X	X	X	X	NO ACTION (BUS FLOATS)
X	0	X	X	X	X	NO ACTION (BUS FLOATS)
1	1	0	0	1	X	X TO BUS } INCREMENT SEQUENCE
1	1	0	1	1	X	Z TO BUS } COUNTER WHEN
1	1	1	0	1	X	Y TO BUS } STB AND RD = 1
1	1	1	1	1	X	STATUS TO BUS
1	1	0	0	0	1	LOAD X FROM BUS } INCREMENT
1	1	0	1	0	1	LOAD Z FROM BUS } SEQUENCE
1	1	1	0	0	1	LOAD Y FROM BUS } COUNTER
1	1	1	1	0	1	LOAD CONTROL REGISTER
1	1	X	X	0	0	NO ACTION (BUS FLOATS)

* ( ) = 1800 system signals. 1 = High Level, 0 = Low Level, X = High or Low Level.

CONTROL REGISTER BIT ASSIGNMENT TABLE



B1	B0	OPERATION SELECT
0	0	NO OPERATION
0	1	MULTIPLY
1	0	DIVIDE
1	1	ILLEGAL STATE

B5	B4	# of MDU's
1	1	ONE MDU
1	0	TWO MDU's
0	1	THREE MDU's
0	0	FOUR MUD's

# OF MDU's	SHIFT RATE
1	CLOCK ÷ 2
2	CLOCK ÷ 4
3	CLOCK ÷ 8
4	CLOCK ÷ 8

STATUS REGISTER

	Status Byte
Bit	7 6 5 4 3 2 1 0
Output	0 0 0 0 0 0 0 O.F.
	O.F. = 1 if overflow (only valid after a divide has been done)

NOTE: Bits 1 — 7 are read as 0 always

CDP1855, CDP1855C

DELAY NEEDED WITH AND WITHOUT PRESCALER

8N+1 Shifts/Operation at 1 Clock Cycle/Shift
N = Number of MDU's S = Shift Rate

Number of MDU's	No Prescaler		With Prescaler		
	Shifts = 8N+1 Needed	Machine Cycles Needed*	Shifts = S (8N+1) Needed	Machine Cycles Needed*	Shift Rate
1	9	2 (1 NOP)	18	3 (1 NOP)	2
2	17	2 (1 NOP)	68	9 (3 NOPs)	4
3	25	3 (1 NOP)	200	25 (9 NOPs)	8
4	33	4 (2 NOPs)	264	33 (11 NOPs)	8

*NOP instruction is shown for machine cycles needed (3/NOP). Other instructions may be used.

CDP1855 INTERFACING SCHEMES

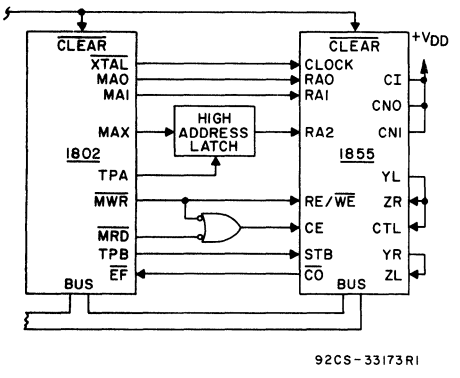


Fig. 3 - Required connection for memory mapped addressing of the MDU.

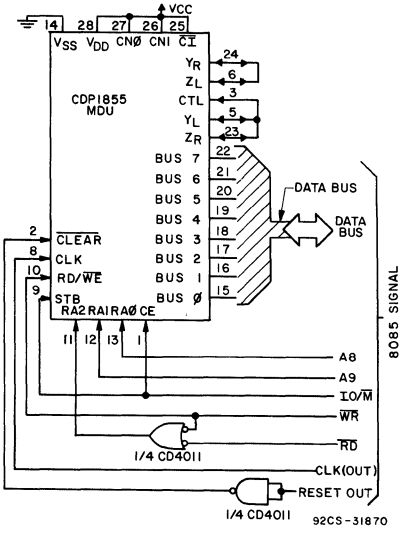


Fig. 4 - Interfacing the CDP1855 to an 8085 microprocessor as an I/O device.

PROGRAMMING EXAMPLE FOR MULTIPLICATION

For a 24-bit x 24-bit multiply using the system shown in Figure 5, the following is an assembly listing of a program to multiply $201F7C_{16}$ by $723C09_{16}$:

```
MEMORY LOCATION  OP CODE  LINE NO.  ASSEMBLY LANGUAGE
0000             F830;    0001      LDI 030H
0002             A2;      0002      PLO R2              ..LOAD 30 INTO R2.0
0003             F800;    0003      LDI 00H
0005             B2;      0004      PHI R2              ..LOAD 00 INTO R2.1 (R2=0030)
0006             6758;    0005      OUT 7; DC 058H      ..LOAD CONTROL REGISTERS
0008             ;        0006                          ..SPECIFYING THREE MDU'S,
0008             ;        0007                          ..RESET THE Y REGISTER AND
0008             ;        0008                          ..SEQUENCE COUNTER
0008             6420;    0009      OUT 4; DC 020H      ..LOAD MSB OF X REGISTER
000A             ;        0010                          ..WITH 20
000A             641F;    0011      OUT 4; DC 01FH      ..LOAD NEXT MSB OF X REG
000C             ;        0012                          ..WITH 1F
000C             647C;    0013      OUT 4; DC 07CH      ..LOAD LSB OF X REGISTER
000E             ;        0014                          ..WITH 7C
000E             6572;    0015      OUT 5; DC 072H      ..LOAD MSB OF Z REGISTER
0010             ;        0016                          ..WITH 72
0010             653C;    0017      OUT 5; DC 03CH      ..LOAD NEXT MSB OF Z REG
0012             ;        0018                          ..WITH 3C
0012             6509;    0019      OUT 5; DC 09H       ..LOAD LSB OF Z REGISTER
0014             ;        0020                          ..WITH 09
0014             6759;    0021      OUT 7; DC 059H      ..LOAD CONTROL REGISTERS
0016             ;        0022                          ..RESETTING Y REGISTERS
0016             ;        0023                          ..AND SEQUENCE COUNTERS
0016             ;        0024                          ..AND STARTING MULTIPLY
0016             ;        0025                          ..OPERATION
                          DELAY FOR MULTIPLY TO FINISH
0016             E2;      0026      SEX R2
0017             6E60;    0027      INP 6; IRX          ..MSB OF RESULTS IS STORED
0019             ;        0028                          ..AT LOCATION 0030
0019             6E60;    0029      INP 6; IRX
001B             6E60;    0030      INP 6; IRX
001D             6D60;    0031      INP 5; IRX
001F             6D60;    0032      INP 5; IRX
0021             6D;      0033      INP 5               ..COMPLETE LOADING RESULT
0022             ;        0034                          ..INTO MEMORY LOCATIONS
0022             ;        0035                          ..0030 TO 0035
0022             ;        0036                          ..RESULTS=0E558DBA2B5C
0022             3022;    0037 STOP BR STOP
0024             ;        0038      END
0000
```

The result of $201F7C_{16}$ x $723C09_{16}$ is 0E558DBA2B5C = 15760612797276_{10}. It will be stored in memory as follows:

LOC	BYTE
0030	0E
31	55
32	8D
33	BA
34	2B
35	5C

BEFORE MULTIPLY

	MDU1	MDU2	MDU3
Register X	20	1F	7C
Register Y	00	00	00
Register Z	72	3C	09

AFTER MULTIPLY

	MDU1	MDU2	MDU3
Register X	20	1F	7C
Register Y	0E	55	8D
Register Z	BA	2B	5C

CDP1855, CDP1855C

PROGRAMMING EXAMPLE FOR DIVISION

```
MEMORY LOCATION   OP CODE        LINE NO.   ASSEMBLY LANGUAGE
0000              ;              0001       Program example for a 16 bit by 8 bit divide using 1 CDP1855 MDU
0000              ;              0002       . . Gives a 16 bit answer with 8 bit remainder
0000              ;              0003
0000              68C22000;      0004       RLDI R2,2000H          . . Answer is stored at 2000 hex
0004              ;              0005                              .   Register 2 points to it
0004              68C33000;      0006       RLDI R3,3000H          .   Dividend is stored at 3000 hex
0008              ,              0007                                  Register 3 points to it
0008              68C44000,      0008       RLDI R4,4000H          .   Divisor is stored at 4000 hex
000C              ;              0009                                  Register 4 points to it
000C              ;              0010
000C              E067F0;        0011       SEX R0, OUT 7; DC OF0H     Write to the control register to use
000F              ,              0012                                  clock / 2; 1 MDU; reset sequence
000F              ;              0013                              .   counter, and no operation
000F              ;              0014
000F              E464;          0015       SEX R4, OUT 4              Load the divisor into the X register
0011              ;              0016
0011              E06600;        0017       SEX R0; OUT 6; DC 0        Load 0 into the Y register
0014              E365;          0018       SEX R3, OUT 5              Load the most significant 8 bits of
0016              ;              0019                              .   the dividend into the Z register
0016              ,              0020
0016              E067F2;        0021       SEX R0; OUT 7, DC 0F2H .   Do the first divide, also resets the
0019              ;              0022                              . . sequence counter
0019              ,              0023
0019              E26D60;        0024       SEX R2, INP 5; IRX     .   Read and store the most significant
001C              ,              0025                              .   8 bits of the answer at 2000 hex
001C              ,              0026
001C              E067F0;        0027       SEX R0; OUT 7, DC 0F0H . . Reset the sequence counter
001F              ;              0028
001F              E365,          0029       SEX R3, OUT 5          . . Load the 8 least significant 8 bits
0021              ,              0030                                  of the original dividend into the Z
0021              ;              0031                              .   register
0021              ;              0032
0021              E067F2;        0033       SEX R0, OUT 7; DC 0F2H     Do the second division
0024              ;              0034
0024              E26D60,        0035       SEX R2, INP 5, IRX         Read and store the least significant
0027              ,              0036                              .   8 bits of the answer at 2001 hex
0027              6E,            0037       INP 6                      Read and store the remainder at 2002
0028              ,              0038                                  hex
0000
```

For the divide operation (Fig. 5), the formula is:

$$\frac{Y_3Y_2Y_1Z_3Z_2Z_1}{X_3X_2X_1} = Z_3Z_2Z_1 + \frac{Y_3Y_2Y_1}{X_3X_2X_1}$$

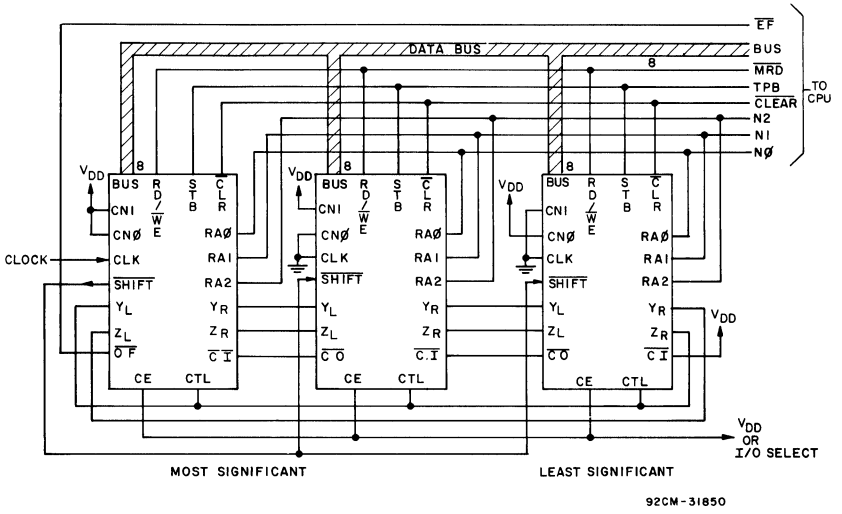


Fig. 5 - Cascading three MDU's (CDP1855) in an 1800 system with MDU's being accessed as I/O ports in programming example.

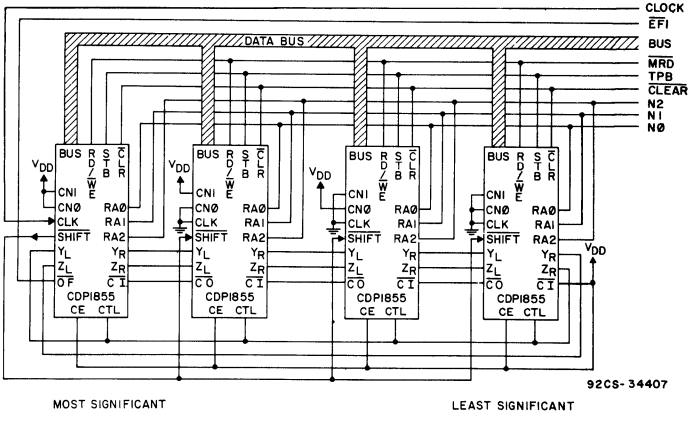


Fig. 6 - Cascading four MDU's (CDP1855).

CDP1855, CDP1855C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5% t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Fig. 7)

CHARACTERISTIC•		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Operation Timing									
Maximum Clock Frequency+		5	3.2	4	—	3.2	4	—	MHz
		10	6.4	8	—	—	—	—	
Maximum Shift Frequency (1 Device)Δ		5	1.6	2	—	1.6	2	—	
		10	3.2	4	—	—	—	—	
Minimum Clock Width	t_{CLK0}	5	—	100	150	—	100	150	ns
	t_{CLK1}	10	—	50	75	—	—	—	
Minimum Clock Period	t_{CLK}	5	—	250	312	—	250	312	
		10	—	125	156	—	—	—	
Clock to Shift Prop. Delay	t_{CSH}	5	—	200	300	—	200	300	
		10	—	100	150	—	—	—	
Minimum C.I. to Shift Setup	t_{SU}	5	—	50	67	—	50	67	
		10	—	25	33	—	—	—	
C.O. from Shift Prop. Delay	t_{PLH}	5	—	450	600	—	450	600	
	t_{PHL}	10	—	225	300	—	—	—	
Minimum C.I. from Shift Hold	t_H	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Register Input Setup	t_{SU}	5	—	-20	10	—	-20	10	
		10	—	-10	10	—	—	—	
Register after Shift Delay	t_{PLH}	5	—	400	600	—	400	600	
	t_{PHL}	10	—	200	300	—	—	—	
Minimum Register after Shift Hold	t_H	5	—	50	100	—	50	100	
		10	—	25	50	—	—	—	
C.O. from C.I. Prop. Delay	t_{PLH}	5	—	100	150	—	100	150	
	t_{PHL}	10	—	50	75	—	—	—	
Register from C.I. Prop. Delay	t_{PLH}	5	—	80	120	—	80	120	
	t_{PHL}	10	—	40	60	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25° C and nominal voltages.

+Clock frequency and pulse width are given for systems using the internal clock option of the CDP1855. Clock frequency equals shift frequency for systems not using the internal clock option.

ΔShift period for cascading of devices is increased by an amount equal to the $\overline{C.I.}$ to $\overline{C.O.}$ Prop. Delay for each device added.

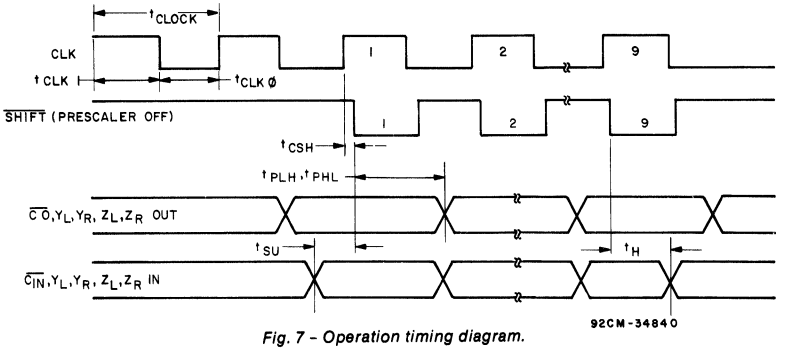


Fig. 7 - Operation timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5% t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Fig. 8)

CHARACTERISTIC•		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Write Cycle									
Minimum Clear Pulse Width	$t_{\overline{CLR}}$	5	—	50	75	—	50	75	ns
		10	—	25	40	—	—	—	
Minimum Write Pulse Width	t_{WW}	5	—	150	225	—	150	225	
		10	—	75	115	—	—	—	
Minimum Data-In Setup	t_{DSU}	5	—	-75	0	—	-75	0	
		10	—	-40	0	—	—	—	
Minimum Data-In-Hold	t_{DH}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Address to Write Setup	t_{ASU}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Minimum Address after Write Hold	t_{AH}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25° C and nominal voltages.

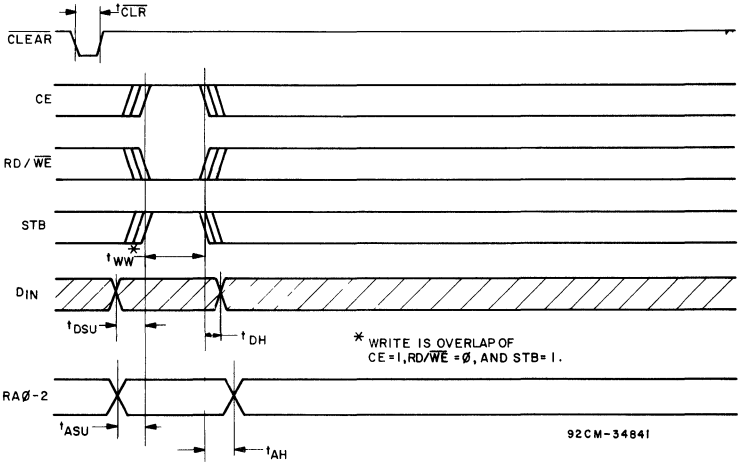


Fig. 8 - Write timing diagram.

CDP1855, CDP1855C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ±5% t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF (See Fig. 9)

CHARACTERISTIC•		V_{DD} (V)	LIMITS						UNITS
			CDP1855			CDP1855C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Read Cycle									
CE to Data Out Active	t_{CDO}	5	—	200	300	—	200	300	ns
		10	—	100	150	—	—	—	
CE to Data Access	t_{CA}	5	—	300	450	—	300	450	
		10	—	150	225	—	—	—	
Address to Data Access	t_{AA}	5	—	300	450	—	300	450	
		10	—	150	225	—	—	—	
Data Out Hold after CE	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	—	—	—	
Data Out Hold after Read	t_{DOH}	5	50	150	225	50	150	225	
		10	25	75	115	—	—	—	
Read to Data Out Active	t_{RDO}	5	—	200	300	—	200	300	
		10	—	100	150	—	—	—	
Read to Data Access	t_{RA}	5	—	200	300	—	200	300	
		10	—	100	150	—	—	—	
Strobe to Data Access	t_{SA}	5	50	200	300	50	200	300	
		10	25	100	150	—	—	—	
Minimum Strobe Width	t_{SW}	5	—	150	225	—	150	225	
		10	—	75	115	—	—	—	

•Maximum limits of minimum characteristics are the values above which all devices function.

*Typical values are for T_A = 25° C and nominal voltages.

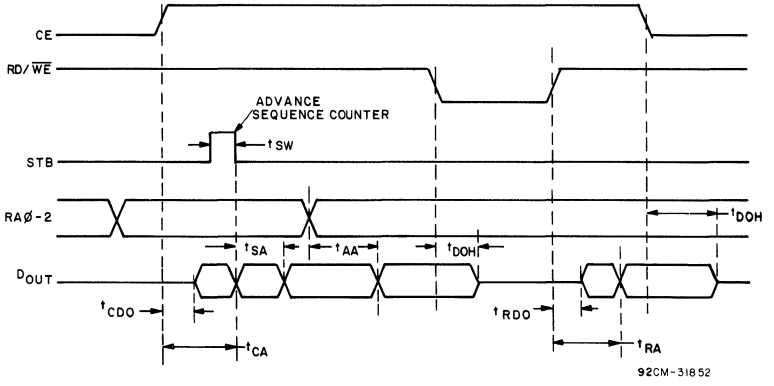


Fig. 9 - Read timing diagram.