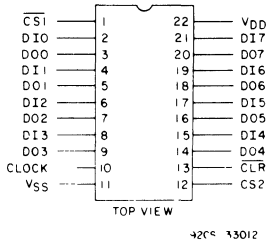
CDP1872C, CDP1874C, CDP1875C



CDP1872C Input Port TERMINAL ASSIGNMENT

High-Speed 8-Bit Input and Output Ports

Features:

- *Parallel 8-bit input/output register with buffered outputs*
- *High-speed data-in to data-out: 85 ns (max.) at V_{DD} = 5 V*
- *Flexible applications in microprocessor systems as buffers and latches*
- *High order address-latch capability in CDP1800 series microprocessor systems*
- *Output sink current = 5 mA (min.) at V_{DD} = 5 V*
- *3-state output - CDP1872C and CDP1874C*

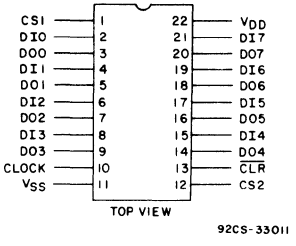
The RCA-CDP1872C, CDP1874C and CDP1875C devices are high-speed 8-bit parallel input and output ports designed for use in the CDP1800 microprocessor system and for general use in other microprocessor systems. The CDP1872C and CDP1874C are 8-bit input ports; the CDP1875C is an 8-bit output port.

These devices have flexible capabilities as buffers and data latches and are reset by $\overline{CLR}$ input when the data strobe is not active.

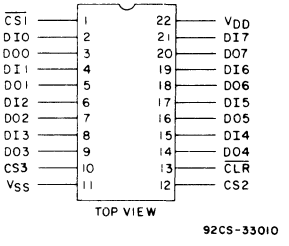
The CDP1872C and CDP1874C are functionally identical except for device selects. The CDP1872C has one active low and one active high select; the CDP1874C has two active high device selects. These devices also feature 3-state outputs when deselected. Data is strobed into the register on the leading edge of the CLOCK and latched on the trailing edge of the CLOCK.

The CDP1875C is an output port with data latched into the registers when the device selects are active. There are two active high and one active low selects. The output buffers are enabled at all times.

These devices are supplied in 22-lead hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 22-lead dual-in-line plastic package (E suffix).



CDP1874C Input Port TERMINAL ASSIGNMENT



CDP1875C Output Port TERMINAL ASSIGNMENT

File Number **1255**

CDP1872C, CDP1874C, CDP1875C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) ..... -0.5 to +7 V
(Voltage referenced to V_{SS} Terminal)
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D).
For T_A = -40°C to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60°C to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55°C to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100°C to +125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A - FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)·
PACKAGE TYPE D ..... -55°C to +125°C
PACKAGE TYPE E ..... -40°C to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = -40°C to +85°C.
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES	UNITS
DC Operating-Voltage Range	4 to 6.5	V
Input Voltage Range	V_{SS} to V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40°C to +85°C, V_{DD} ± 5%, except as noted

CHARACTERISTIC		TEST CONDITIONS			LIMITS ALL TYPES			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN.	TYP. •	MAX.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	25	50	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	5	10	—	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-4	-7	—	
Output Voltage Low-Level *	V_{OL}	—	0, 5	5	—	0	0.1	V
Output Voltage High-Level *	V_{OH}	—	0, 5	5	4.9	5	—	
Input Low Voltage	V_{IL}	0.5, 4.5	—	5	—	—	1.5	
Input High Voltage	V_{IH}	0.5,4.5	—	5	3.5	—	—	
Input Leakage Current	I_{IN}	—	0, 5	5	—	—	±1	μA
3-State Output Leakage Current #	I_{OUT}	0, 5	0, 5	5	—	—	±5	
Input Capacitance	C_{IN}	—	—	—	—	15	—	pF
Output Capacitance #	C_{OUT}	—	—	—	—	15	—	

• Typical values are for T_A = 25°C and V_{DD} ±5%.
* I_{OL} = I_{OH} = 1 μA.
# For CDP1872C and CDP1874C only.

CDP1872C, CDP1874C, CDP1875C

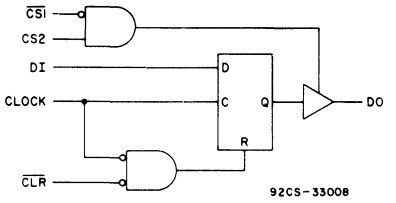


Fig. 1 - Equivalent logic diagram (1 of 8 latches shown) for CDP1872C.

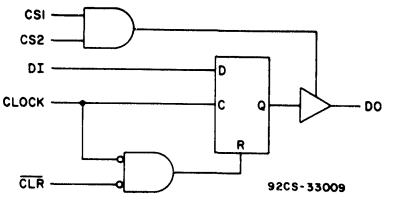


Fig. 2 - Equivalent logic diagram (1 of 8 latches shown) for CDP1874C.

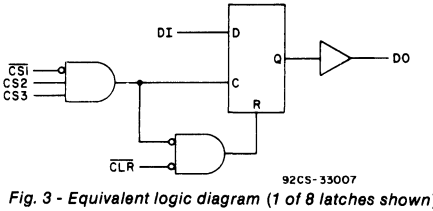


Fig. 3 - Equivalent logic diagram (1 of 8 latches shown) for CDP1875C.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V, t_r, t_f = 10 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 150 pF

CHARACTERISTIC		LIMITS		UNITS
		CDP1872C CDP1874C		
		TYP. •	MAX. †	
Input Port (Fig. 4)				
Output Enable	t_{EN}	45	90	ns
Output Disable	t_{DIS}	45	90	
Clock to Data Out	t_{CLO}	45	90	
$\overline{\text{Clear}}$ to Output	t_{CRO}	80	160	
Data In to Data Out	t_{DIO}	50	85	
Minimum Data Setup Time	t_{DSU}	10	30	
Data Hold Time	t_{DH}	10	30	
Minimum Clock Pulse Width	t_{CL}	30	60	
Minimum $\overline{\text{Clear}}$ Pulse Width	t_{CR}	30	60	

• Typical values are for T_A = 25°C and V_{DD} ±5%.

† Maximum values are for T_A = 85°C and V_{DD} ±5%.

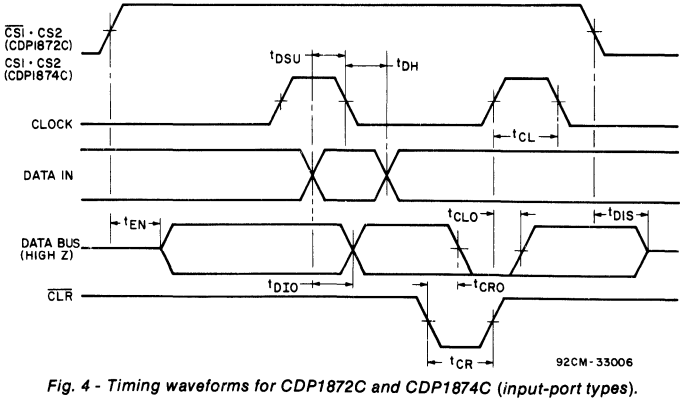


Fig. 4 - Timing waveforms for CDP1872C and CDP1874C (input-port types).

CDP1872C, CDP1874C, CDP1875C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25° C, V_{DD} = 5 V, t_r, t_f = 10 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 150 pF

CHARACTERISTIC		LIMITS		UNITS
		CDP1875C		
		TYP. •	MAX. †	
Output Port (Fig. 5)				
Clock to Data Out	t_{CLO}	50	100	ns
$\overline{\text{Clear}}$ to Output	t_{CRO}	80	160	
Data In to Data Out	t_{DIO}	50	85	
Minimum Data Setup Time	t_{DS}	10	30	
Data Hold Time	t_{DH}	10	30	
Minimum $\overline{\text{Clear}}$ Pulse Width	t_{CR}	30	60	

• Typical values are for T_A = 25° C and V_{DD} ±5%.
† Maximum values are for T_A = 85° C and V_{DD} ±5%.

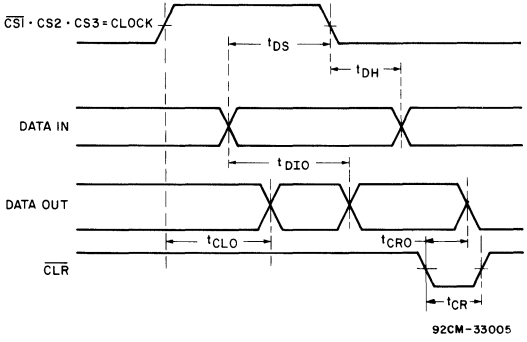


Fig. 5 - Timing waveforms for CDP1875C (output port).

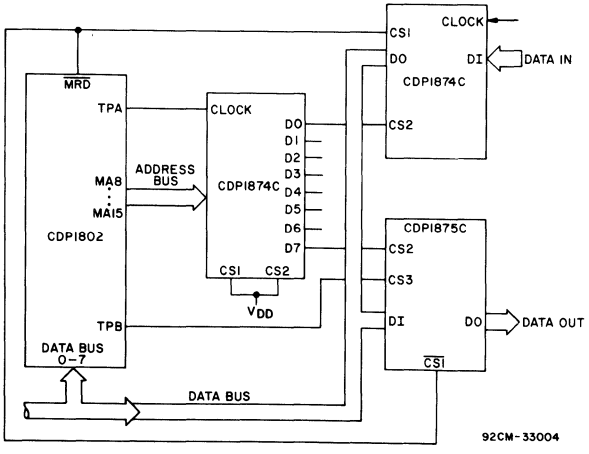


Fig. 6 - CDP1874C used as an input port and address latch with CDP1875C used as an output port.

CDP1872C, CDP1874C, CDP1875C

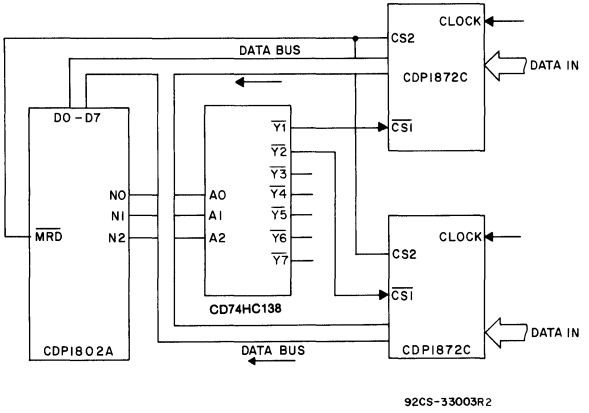


Fig. 7 - CDP1872C used as an input port and selected by CD74HC138.

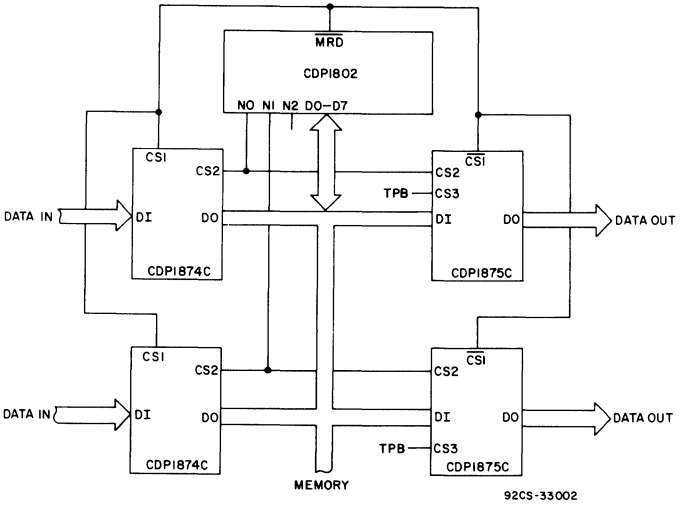


Fig. 8-CDP1874C and CDP1875C used as input/output buffers.