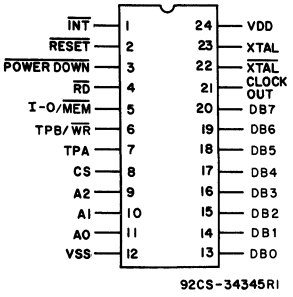
CDP1879, CDP1879C-1

CMOS Real-Time Clock



TERMINAL ASSIGNMENT

Features

- *CPU interface for use with general-purpose microprocessors*
- *Time of day/calendar*
- *Reads seconds, minutes, hours*
- *Reads day of month and month*
- *Alarm circuit with seconds, minutes or hours operation*
- *Power down mode*
- *Separate clock output selects 1 of 15 square wave signals*
- *Interrupt output activated by clock output and/or alarm circuit*
- *Data integrity sampling for clock rollover eliminated*
- *On-board oscillator 4.19 MHz, 2.09 MHz or 1.048 MHz @ 10 V (CDP1879) crystal operation*
  4.19 MHz, 2.09 MHz, 1.048 MHz or 32 kHz @ 5 V (CDP1879C-1) crystal operation
  4.19 MHz, 2.09 MHz, 1.048 MHz or 32 kHz @ 10 V or 5 V external clock operation
- *Addressable in memory space or CDP1800 series I/O mode*
- *Low standby (timekeeping) voltage with external clock*

The CDP1879 real-time clock supplies time and calendar information from seconds to months in BCD format. It consists of 5 separately addressable and programmable counters that divide down an oscillator input. The clock input can have any one of 4 possible frequencies, allowing flexibility in the choice of crystal or external clock sources. Using an external 32-kHz clock source, timekeeping can be performed down to 2.5 V (see Standby (Timekeeping) Voltage Operation).

The device can be memory-mapped for use with any general-purpose microprocessor and has the additional capability of operating in the CDP1800-series input/output mode.

The real-time clock functions as a time-of-day/calendar with an alarm capability that can be set for combinations of seconds, minutes or hours. Alarm time is configured by loading alarm latches that activate an interrupt output through a comparator when the counter and alarm latch values are equal.

Fifteen selectable square-wave signals are available as a separate clock output signal and can also activate the interrupt output. A status register is available to indicate the interrupt source. The value in an 8-bit control register determines the operational characteristics of the device, by selecting the prescaler divisor and the clock output, and controls the load and alarm functions.

A transparent "freeze" circuit precludes clock rollover during counter and latch access times to assure stable and accurate values in the counters and alarm latches.

The CDP1879 is functionally identical to the CDP1879C-1. The CDP1879 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1879C-1 has a recommended operating voltage range of 4 to 6.5 volts. The CDP1879 and the CDP1879C-1 are supplied in 24-lead hermetic dual-in-line side-brazed ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

CDP1879 MODES OF OPERATION

OPERATION	FUNCTION
Read	1. Seconds, minutes, hours, date and month counters 2. Status register to identify interrupt source
Write	1. Control register to set device operation 2. Seconds, minutes, hours, date and month counters 3. Alarm latches for alarm time
Power Down	1. Tri-state interrupt output with active alarm or clock out circuitry for wake-up control. 2. Data bus and address inputs are "DON'T CARE".
Interrupt	1. Clock out as source 2. Alarm time as source 3. Either interrupt can occur during normal or power down mode

File Number **1360**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP1879 ..... -0.5 to +11 V
CDP1879C-1 ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0 5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 40 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D, H ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in (1.59 ± 0 79 mm) from case for 10 s max ..... +265° C

4

OPERATING CONDITIONS at T_A=Full Package-Temperature Range, unless otherwise noted.
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1879		CDP1879C-1		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	
DC Standby (Timekeeping) Voltage* V_{STBY}					
T_A = -40° to +85° C†	3	—	3	—	V
T_A = 0° to +70° C	2.5	—	2.5	—	
Clock Input Rise or Fall Time t_r, t_f					
V_{DD} = 5 V	—	10	—	10	μs
V_{DD} = 10 V	—	1	—	—	

*Timekeeping function only, no READ/WRITE accesses, 32-kHz external frequency source only, no crystal operation.

†See Standby (Timekeeping) Voltage Operation, Page 11.

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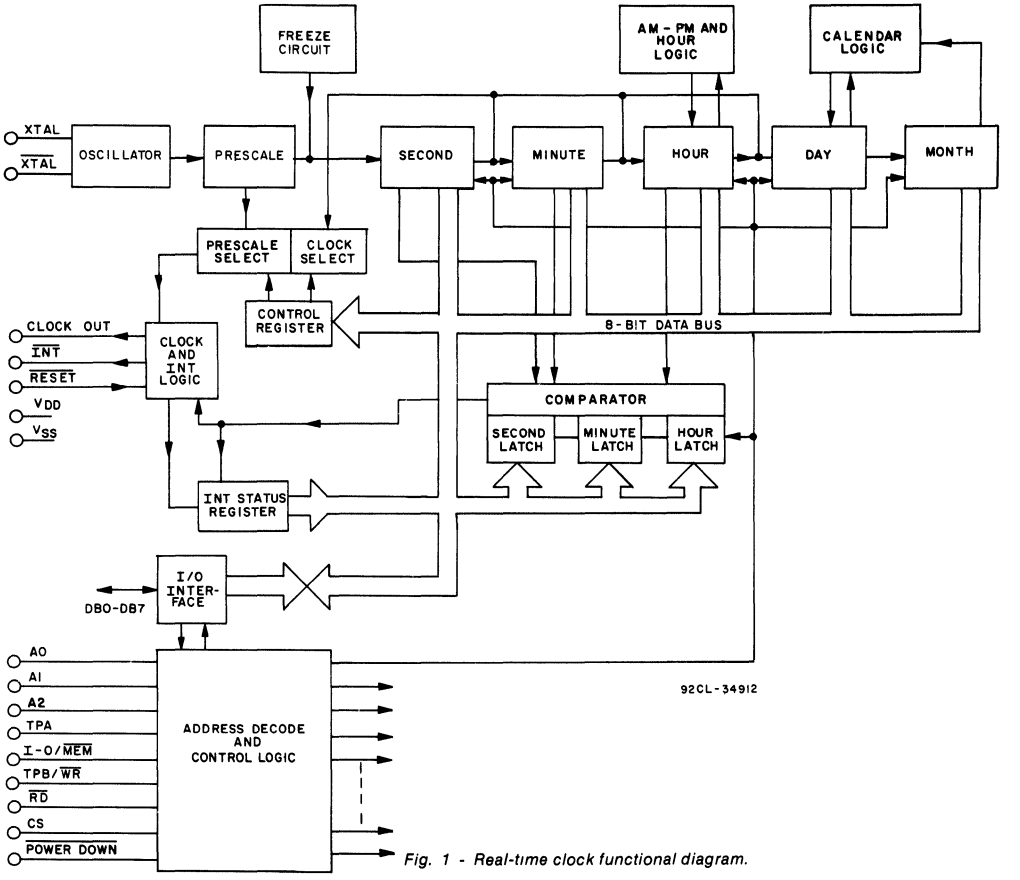

Fig. 1 - Real-time clock functional diagram.

TABLE I

Control Register Bit Assignment	
Bit 1, 0	
Frequency 00	32768 Hz
Select 01	1.048576 MHz
10	2.097152 MHz
11	4.194304 MHz
Bit 2	
Start/Stop	1 = Start
	0 = Stop
Bit 3	
Counter/Latch Control	
"0" = Write to counter and disable alarm	
"1" = Write to & enable alarm	
Clock Select	
Bits 7, 6, 5, 4	
0000 — disable μs	1000 — 62.5 ms
0001 — 488.2 μs	1001 — 125 ms
0010 — 976.5 μs	1010 — 250 ms
0011 — 1953.1 μs	1011 — 500 ms
0100 — 3906.2 μs	1100 — sec.
0101 — 7812.5 μs	1101 — min.
0110 — 15.625 ms	1110 — hour
0111 — 31.25 ms	1111 — day

TABLE II

Addresses	A2	A1	A0
Latch, Counter Seconds	0	1	0
Latch, Counter Minutes	0	1	1
Latch, Counter Hours	1	0	0
Counter, Day	1	0	1
Counter, Month	1	1	0
Control, Register	1	1	1
Status Register	1	1	1

MSB of hours counters (Bit 7) is an AM-PM bit. 0 = AM; 1 = PM.
Bit 6 of hours counter controls 12/24 hr. 1 = 12 hr: 0 = 24 hr.
Status Register: Bit 7 MSB = alarm Interrupt Source: Bit 6 = clock
MSB of Month Counter (Bit 7) is a Leap Year Bit 0 = No, 1 = Yes.

CDP1879, CDP1879C-1

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C V_{DD} ± 5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1879			CDP1879C-1			
					Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current	I_{DD}		0, 5	5	—	0.01	50	—	0.02	200	µA
			0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink)		0.4	0, 5	5	1.8	4	—	—	—	—	mA
Current, Data Bus & $\overline{INT}$	I_{OL}	0.5	0, 10	10	3.6	7	—	—	—	—	
Output High Drive (Source)		4.6	0, 5	5	-1.1	-2.3	—	-1.1	-2.3	—	
Current, Data Bus & $\overline{INT}$	I_{OH}	9.5	0, 10	10	-2.6	-4.4	—	—	—	—	
Output Low Drive (Sink)		0.4	0, 5	5	0.6	1.4	—	0.6	1.4	—	
Current, Clock Out	I_{OL}	0.5	0, 10	10	1.2	3	—	—	—	—	
Output High Drive (Source)		4.6	0, 5	5	-1.1	-2.3	—	-1.1	-2.3	—	
Current, Clock Out	I_{OH}	9.5	0, 10	10	-2.6	-4.4	—	—	—	—	
Output Low Drive (Sink)		0.4	0, 5	5	0.2	0.9	—	0.2	0.9	—	
Current, $\overline{XTAL}$ Out	I_{OL}	0.5	0, 10	10	0.4	2	—	—	—	—	
Output High Drive (Source)		4.6	0, 5	5	-0.15	-0.4		-0.15	-0.4	—	
Current, $\overline{XTAL}$ Out	I_{OH}	9.5	0, 10	10	-0.3	-0.7	—	—	—	—	
Output Voltage		—	0, 5	5	—	0	0.1	—	0	0.1	V
Low-Level	V_{OL}‡	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage		—	0, 5	5	4.9	5	—	4.9	5	—	
High Level	V_{OH}‡	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
		0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
		0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	µA
			0, 10	10	—	—	±2	—	—	—	
3-State Output		0, 5	0 ,5	5	—	—	±1	—	—	±1	
Leakage Current	I_{OUT}	0, 10	0, 10	10	—	—	±1	—	—	—	
Operating Current *											mA
External Clock	32 kHz	—	—	5	—	0.01	0.15	—	0.01	0.15	
	1 MHz	—	—	5	—	0.2	1	—	0.2	1	
	2 MHz	—	—	5	—	0.35	1.5	—	0.35	1.5	
	4 MHz	—	—	5	—	0.7	2	—	0.7	2	
	32 kHz	—	—	10	—	0.03	0.25	—	—	—	
	1 MHz	—	—	10	—	0.4	2	—	—	—	
	2 MHz	—	—	10	—	0.8	3	—	—	—	
	4 MHz	—	—	10	—	1.6	4.5	—	—	—	
XTAL Oscillator**	32 kHz	—	—	5	—	0.1	0.25	—	0.1	0.25	
	1 MHz	—	—	5	—	0.3	0.5	—	0.3	0.5	
	2 MHz	—	—	5	—	0.4	0.6	—	0.4	0.6	
	4 MHz	—	—	5	—	0.6	0.8	—	0.6	0.8	
	1 MHz	—	—	10	—	1.6	3	—	—	—	
	2 MHz	—	—	10	—	1.8	3.5	—	—	—	
	4 MHz	—	—	10	—	2	5	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	
Maximum Clock Rise	t_r,t_f	—	—	5	—	—	10	—	—	10	µs
and Fall Times		—	—	10	—	—	1	—	—	—	

•Typical values are for TA = 25° C and nominal V_{DD}.

‡I_{OL} = I_{OH} = 1 µA.

*Operating current measured with clockout = 488.2 µs and no load;

** See Table III and Fig. 6 for oscillator circuit information.

CDP1879, CDP1879C-1

PROGRAMMING MODEL

WRITE AND READ REGISTERS

BCD FORMAT

DB7 DB0

TENS 0-5	UNITS 0-9

SECONDS COUNTER (00-59)

DB7 DB0

TENS 0-5	UNITS 0-9

MINUTES COUNTER (00-59)

DB7 DB6 DB0

X	X	TENS 0-2	UNITS 0-9

HOURS COUNTER (01-12 or 00-23)
DB7 0=AM, 1=PM
DB6 0=24 HR, 1=12 HR

DB7 DB0

TENS 0-3	UNITS 0-9

DAY OF MONTH COUNTER
(01-28, 29, 30, 31)

DB7 DB0

X	TENS 0 or 1	UNITS 0-9

MONTH COUNTER

(JAN=1 DEC=12)
DB7 0=NO LEAP YEAR
1=LEAP YEAR

WRITE ONLY REGISTERS

DB7 DB0

7	6	5	4	3	2	1	0

CONTROL REGISTER

DB0-DB1 - FREQUENCY SELECT
DB2 - START/STOP
DB3 - COUNTER/ALARM LATCH CONTROL
DB4-DB7 - CLOCK OUTPUT SELECT

DB7 DB0

TENS 0-5	UNITS 0-9

SECONDS ALARM LATCH (00-59)

DB7 DB0

TENS 0-5	UNITS 0-9

MINUTES ALARM LATCH (00-59)

DB7 DB6 DB0

X	X	TENS 0-2	UNITS 0-9

HOURS ALARM LATCH (01-12 or 00-23)
12 HR, DB7=0 AM, 1=PM
24 HR, DB7=X

READ ONLY REGISTER

DB7 DB6 DB0

X	X	0	0	0	0	0	0

INTERRUPT STATUS REGISTER
DB7=1 ALARM CIRCUIT ACTIVATED $\overline{INT}$.
DB6=1 CLOCK OUTPUT ACTIVATED $\overline{INT}$.

REGISTER TRUTH TABLE

ADDRESS			ACTIVE SIGNAL		BIT 3 CONTROL REGISTER	REGISTER OPERATION
A2	A1	A0	TPB/$\overline{WR}$	$\overline{RD}$		
0	1	0	X	—	0	Write Seconds Counter
0	1	0	—	X	0	Read Seconds Counter
0	1	1	X	—	0	Write Minutes Counter
0	1	1	—	X	0	Read Minutes Counter
1	0	0	X	—	0	Write Hours Counter
1	0	0	—	X	0	Read Hours Counter
1	0	1	X	—	0	Write Date Counter
1	0	1	—	X	0	Read Date Counter
1	1	0	X	—	0	Write Month Counter
1	1	0	—	X	0	Read Month Counter
0	1	0	X	—	1	Write Seconds Alarm Latch
0	1	1	X	—	1	Write Minutes Alarm Latch
1	0	0	X	—	1	Write Hours Alarm Latch
1	1	1	X	—	—	Write Control Register
1	1	1	—	X	—	Read Int. Status Register

GENERAL OPERATION

The real-time clock contains seconds, minutes, and hours, date and month counters that hold time of day/calendar information (see Fig. 2). The frequency of an intrinsic oscillator is divided down to supply a once-a-second signal to the counter series string. The counters are separately addressable and can be written to or read from

The real-time clock contains seconds, minutes and hour write-only alarm latches that store the alarm time (see Fig. 3). When the value of the alarm latches and counters are equal, the interrupt output is activated. The interrupt output can also be activated by a clock output transition The clock output is derived from the prescaler and counters and can be one of 15 square-wave signals. The value in the read-only interrupt status register identifies the interrupt source

Operational control of the real-time clock is determined by the byte in a write-only control register. The 8-bit value in this register determines the correct divisor for the prescaler, a data direction and alarm enable bit, clock output select, and start/stop control (see Fig. 4).

Data transfer and addressing are accomplished in two modes of operation, memory mapping and I/O mapping using the CDP1800-series microprocessors. The mode is selected by the level on an input pin. (I-O/$\overline{\text{MEM}}$). Memory mapping implies use of the address lines as chip selects and address inputs using linear selection or partial or full decoding methods. I/O mapping with the CDP1800-series microprocessors involves use of the N line outputs in conjunction with input and output instructions to transfer data to and from memory.

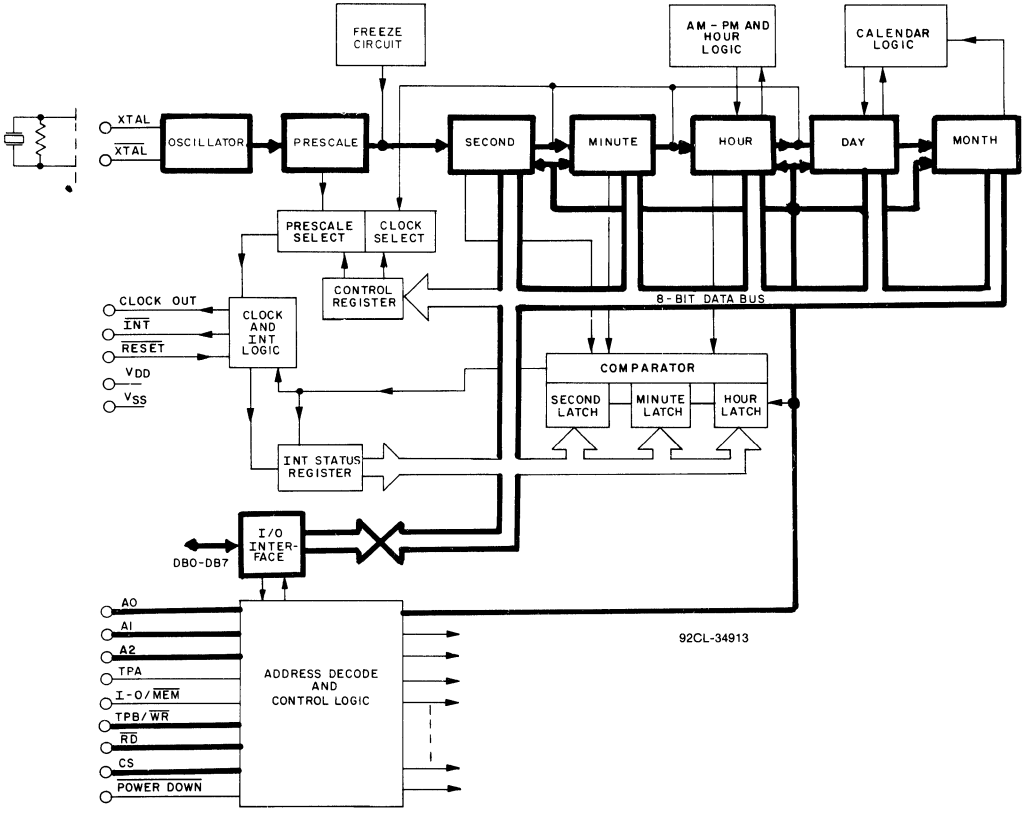

Fig. 2 - Functional diagram - time counters highlighted.

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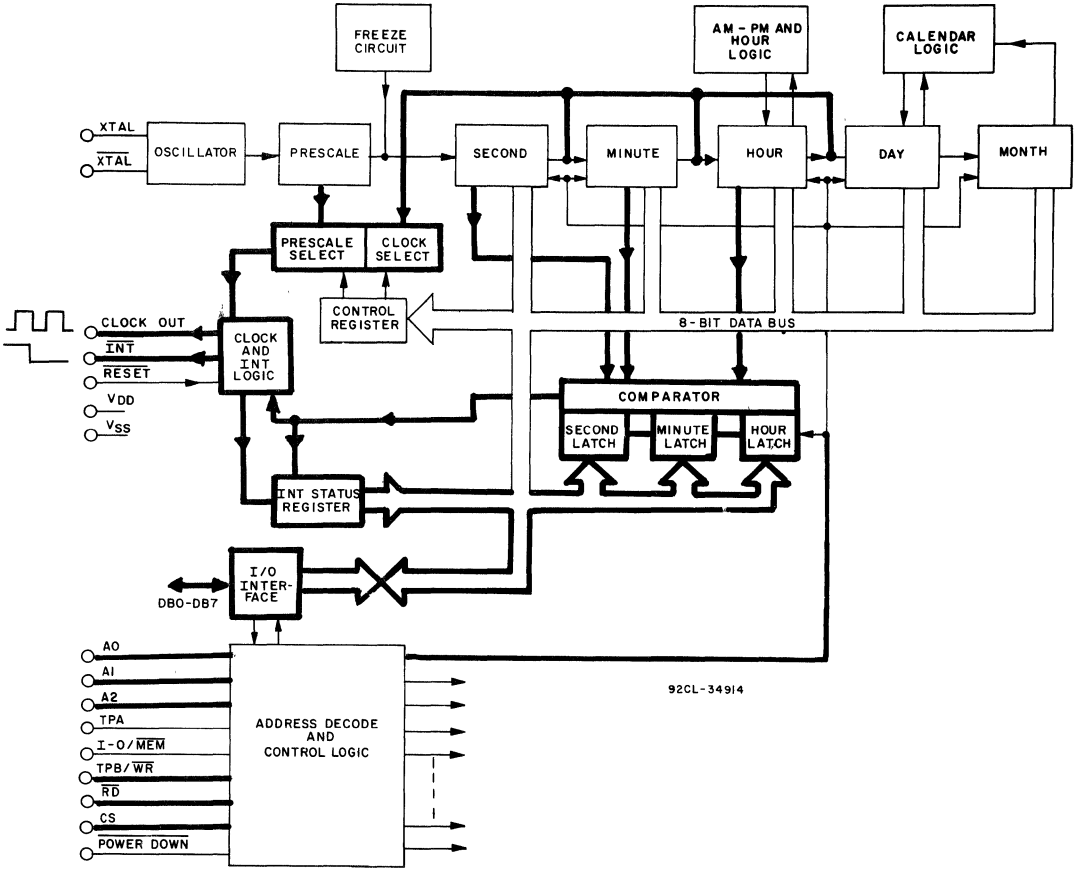

Fig. 3 - Functional diagram - alarm circuit, clock output, interrupt, and status registers highlighted

OPERATIONAL SEQUENCE

Power is applied and the real-time clock is reset. This sets the interrupt output pin high. After the CS pin is set high and with address 7 on the address input lines, the control register is loaded via the data bus to configure the clock.

With selective addressing, the seconds through month counters are then written to and loaded to set the current time. The real-time clock will now hold the current "wall clock" time, with an accuracy determined by the crystal or external clock used. If the alarm function is desired, the control register is accessed and loaded again. This new byte will allow subsequent time data to be entered into the seconds, minutes and hours alarm latches. This sequence is also used when selecting one of the 15 available clock-out signals.

If the alarm function was selected, the interrupt output pin will be set low when the values in the seconds, minutes and hour alarm latches match those in the seconds, minutes and hour counters.

If one of the 15 sub second-to-day clock outputs is selected by the byte in the control register, the clock output pin toggles at that frequency (50% duty cycle). The interrupt output will also be set low on the first clock out negative transition. The interrupt source (alarm or clock out) can be determined by reading the interrupt status register. The clock output can be deselected by placing zero in the upper nibble of the control register if the alarm function is selected as the only interrupt source.

COUNTERS (See Fig. 2)

The counter section consists of an on-board oscillator, a prescaler and 5 counters that hold the time of day/calendar information.

1 of 4 possible external crystals determine the frequency of the on-board oscillator (32,768 Hz, 1.048576 MHz, 2.097152 MHz, 4.194304 MHz). The oscillator output is divided down by a prescaler that supplies a once-a-second pulse to the counters. The seconds counter divides the pulse by 60 and its output clocks the minute counter every 60 seconds. Further division by the minutes, hours, day of month and month counters result in 5 counters holding data that reflects the time/calendar from seconds to months. The counters are addressed separately and BCD data is transferred to and from via the data bus. The most significant

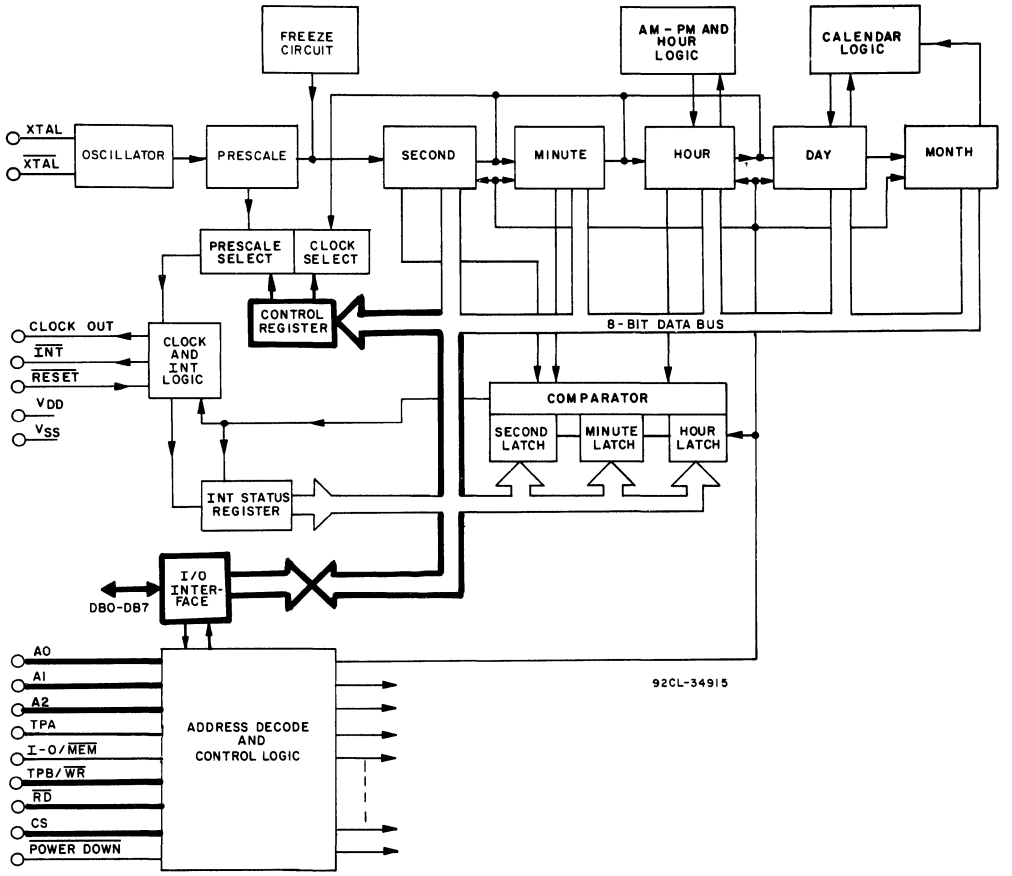

Fig. 4 - Functional diagram - control register highlighted.

bit of the hours counter (Bit 7) is user programmed to indicate AM or PM and will be inverted every 12th hour. (0 = AM, 1 = PM). Bit 6 of the hours counter is user programmed to enable the hours counter for 12 or 24 hour operation. (0 = 24, 1 = 12). If 24-hour operation is selected, the AM-PM bit is "don't care", but still toggles every 12th hour. Writing to the seconds counter resets the last 7 stages of the prescaler, allowing time accuracy to approximately 1/100 of a second.

The most significant bit of the month counter is a Leap Year bit. If it is set to "1", the counter will count to February 29, then roll to March 1. If set to "0" it will go to March 1st after February 28th.

ALARM AND INTERRUPT STATUS REGISTER (See Fig. 3)

The alarm circuit consists of 1) seconds, minutes and hour alarm latches that hold the alarm time, 2) the outputs of the seconds, minutes and hour counters, and 3) a comparator that drives an interrupt output. The comparator senses the counter and alarm latch values and activates the interrupt output (active low) when they are equal.

The write-only alarm latches have the same addresses as their comparable counters. Bit 3 in the control register determines data direction to the latches or counters and alarm enabling. For example, during a write cycle, if bit 3 in the control register is a "1", addressing the seconds counter or alarm latch will load the seconds alarm latch from the data bus and will enable the alarm function. Conversely, if bit 3 in the control register is a "0", addressing the seconds counter or alarm latch during a write cycle will place the value on the data bus into the seconds counter and will disable the alarm function. The interrupt output can be activated by the alarm circuit or the clock output. When an interrupt occurs, the upper two bits of the interrupt status register identify the interrupt source. The interrupt status register has the same address as the control register. Addressing the interrupt status register with the $\overline{RD}$ line active will place these register bits on the data bus. Bits 0-5 are held low. A "1" in bit 6 represents a clock output transition as the interrupt source. A "1" in bit 7 will identify the alarm circuit as the interrupt source.

Activating the reset pin (active low) resets the hour latch to "30" which prevents a match between alarm and time registers during an initialization procedure. Activating the reset pin or writing to the control register resets the interrupt output (high) and clears the interrupt status register.

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CLOCK OUTPUT (See Table I and Fig. 3)

One of 15 counter and prescaler overflows can be selected as a 50% duty cycle output signal that is available at the "clock out" pin. The frequency is selected by the upper nibble in the control register. For example, selecting a one-second clock output will result in a repetitive signal that will be high for 500 ms and low for the same period. The high-to-low transition of the output signal will set the clock bit in the status register and activate the interrupt output. The level of the "clock out" signal is derived from the value in the counter. Example: if hours clock is selected and the minutes counter holds 4 minutes, the clock out will be low for 26 minutes and high for 30 minutes. Thereafter, the clock out will toggle at a 50% duty cycle rate.

CONTROL REGISTER (See Table I and Fig. 4)

BIT 7	6	5	4	3	2	1	BIT 0

CONTROL REGISTER BYTE

The 8-bit value in the control register determines the following:

1. **Bit 0 and 1 — Frequency Select** — Since there are one of 4 possible crystals the oscillator in the real-time clock can operate with, these bit levels determine the prescaler divisor so that an accurate one second pulse is supplied to the counter series string.

BIT 1	BIT 0	FREQUENCY
0	0	32,768 Hz
0	1	1.048576 MHz
1	0	2.097152 MHz
1	1	4.194304 MHz

2. **Bit 2 — Start-Stop Control** — Counter enabling is controlled by the value at this location. A "1" will allow the counters to function and a "0" in this location will disable the counters.
3. **Bit 3 — Counter/Latch Control** — The level at this location controls two functions. It is required since the counters and alarm latches have the same addresses.
   1) A "0" in bit 3 will direct subsequent data to or from the counter selected and the alarm function will be disabled.
   2) A "1" in bit 3 will direct subsequent data to or from the alarm latch and will enable the alarm.
4. **Bits 4 to 7 — Clock Select** — These bits select one of 15 square-wave signals that will be present at the "clock-out" pin. If bits 4 to 7 are zero's, the clock output pin will be high. If a clock is selected, the first high-to-low clock out transition will activate the interrupt pin (active low) and place a "1" in bit 6 of the status register. Writing to the control register or activating the reset pin will set the interrupt pin high and reset the interrupt status register.

Normal operation requires the control register to be written to and loaded first with a control word. However, subsequent writing to a counter if a "clock out" is selected may cause an interrupt out signal. Therefore, "clock-out" should be deselected by writing zero's into bits 4 through 7 if the interrupt is used. When the counters are loaded, the control register is again written to with the value in the upper nibble selecting the "clock out" signal. See Table I.

READ AND WRITE SIGNALS

When the I-O/$\overline{MEM}$ pin is low, the real-time clock is enabled for memory mapped operation. Data on the bus is placed in, or read from a counter, alarm latch or register by 1) placing the CS pin high, 2) selective addressing, 3) placing the TPB/$\overline{WR}$ pin low during a write cycle with the $\overline{RD}$ pin high or 4) setting the $\overline{RD}$ pin low during a read cycle with the TPB/$\overline{WR}$ pin high.

The I/O mapping mode used with the CDP1800 series microprocessor is selected by setting the I-O/$\overline{MEM}$ pin high. The TPB/$\overline{WR}$ pin on the real-time clock is connected to the TPB output pin of the microprocessor. Data on the bus is written to or read from the counters, latches and registers by 1) placing the CS pin high, 2) selective addressing utilizing the microprocessor N lines and I/O instructions, 3) placing the TPB/$\overline{WR}$ pin high with the $\overline{RD}$ pin low during an output or write operation (data is latched on TPB's trailing edge), 4) setting the $\overline{RD}$ line high during an input or read operation. Data is placed on the bus by the real-time clock between the trailing edges of TPA and TPB.

FREEZE CIRCUIT

Since writing to or reading from the counters or alarm latches is performed asynchronously, the once-a-second signal from the prescaler may pulse the counter series string during these operations. This can result in erroneous data. To avoid this occurring, a transparent "freeze" circuit is incorporated into the real-time clock. This circuit is designed to trap and hold the one-second input clock transition if it occurs during access times. When the operations are completed, it is inserted into the counter series string. To utilize the "freeze" circuit, address "1" (A0 = 1, A1 = 0, A2 = 0) is selected first while performing a write operation. Read or write accesses may now be performed with assurance the data is stable. All operations must be concluded within 250 ms of the address "1" access. If memory mapping any dummy write operation after selecting address "1" will set the "freeze" circuit. If using the I/O mode, a 61 output instruction will perform the same function. There is no time restriction on subsequent accesses as long as the read or write operations are preceded by selecting address "1".

POWER DOWN

Power down operation is initiated with a low signal on the "POWER DOWN" input pin. In conjunction with the interrupt output, it is used to supply external control circuits with a 3 level control signal. The operating current is not appreciably reduced during "POWER DOWN" operation. When power down is initiated, any inputs on the address or data bus are ignored. The clock output is set low. The interrupt output is tri-stated. If enabled previously, the alarm circuitry is active and will set the interrupt output pin low when alarm time occurs. The interrupt output will also go low if a clock was selected and an internal high-to-low transition occurs during power down. The clock output pin will remain low. If power down is initiated in the middle of a read or write sequence, it will not become activated until the read or write cycle is completed.

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PIN FUNCTIONS

VDD, VSS — Power and ground for device.

DB0 — DB7 — DATA BUS — 8-bit bidirectional bus that transfers BCD data to and from the counters, latches and registers.

A0, A1, A2 — Address inputs that select a counter, latch or register to read from or write to.

TPA — Strobe input used to latch the value on the chip select pin. CS is latched on the trailing edge of TPA. During memory mapping, it is used to latch the high order address bit used for the chip select. When the real-time clock is used with other microprocessors, or when the high order address of the CDP1800 series microprocessor is externally latched, it is connected to VDD. In the input/output mode, it is used to gate the N lines.

I-O/$\overline{\text{MEM}}$ — Tied low during memory mapping and high when the input/output mode of the CDP1800 series microprocessor is used.

$\overline{\text{RD}}$, TPB/$\overline{\text{WR}}$ — DIRECTION SIGNALS — Active signals that determine data direction flow. In the memory mapped mode, data is placed on the bus from the counters or status register when $\overline{\text{RD}}$ pin is active.

Data is transferred to a counter, latch or the control register when $\overline{\text{RD}}$ is high and TPB/$\overline{\text{WR}}$ is active and latched on the trailing edge (low to high) of the TPB/$\overline{\text{WR}}$ signal.

In the input/output mode, data is placed on the bus from a counter or status register when $\overline{\text{RD}}$ is not active between the trailing edges of TPA and TPB. Data on the bus is written to a counter, latch, or the control register during TPB when $\overline{\text{RD}}$ is active and latched on TPB's trailing edge. The following connections are required between the microprocessor and real-time clock in the CDP1800 series I/O mode.

MICROPROCESSOR REAL-TIME CLOCK

$\overline{\text{MRD}}$	$\overline{\text{RD}}$
TPB	TPB/$\overline{\text{WR}}$
TPA	TPA
N LINES	ADDRESS LINES
I-O/$\overline{\text{MEM}}$	VDD

CS — CHIP SELECT — Used to enable or disable the inputs and outputs. TPA is used to strobe and latch a positive level on this pin to enable the device.

XTAL AND $\overline{\text{XTAL}}$ — The frequency of the internal oscillator is determined by the value of the crystal connected to these pins. "XTAL" may be driven directly by an external frequency source.

CLOCK OUT — 1 of 15 square wave frequencies will appear at this pin when selected. During power down, this pin will be placed low, and will be high during normal operation when the clock is deselected.

$\overline{\text{POWER DOWN}}$ — POWER DOWN CONTROL — A low on this pin will place the device in the power down mode.

$\overline{\text{INT}}$ — Interrupt Output — A low on this pin indicates an active alarm time or high-to-low transition of the "clock out" signal.

$\overline{\text{RESET}}$ — A low on this pin clears the status register and places the interrupt output pin high.

4

FREQUENCY INPUT REQUIREMENTS

The Real-Time Clock operates with the following frequency input sources:

1. An external crystal that is used with the on-board oscillator. The oscillator is biased by a large feedback resistor and oscillates at the crystal frequency (see Fig. 6, Table III).
2. An external frequency input that is supplied at the XTAL input. $\overline{\text{XTAL}}$ is left open (see Fig. 5). A typical external oscillator circuit is shown in Fig. 7 in section, "Standby (Timekeeping) VOLTAGE OPERATION".

TABLE III - Typical Oscillator Circuit Parameters for Suggested Oscillator Circuit, see Fig. 6

PARAMETERS	4.197 MHz	2.097 MHz	1.049 MHz	32768 Hz*	UNITS
R_f	22	22	22	22	MΩ
C_O	39	39	39	39	pF
C_I	5	5	5	5	pF
R_S	—	—	—	200	KΩ
C_L	—	—	—	91	pF
Crystal Impedance	73	200	200	50K (max.)	Ω

*CDP1879C-1 only

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FREQUENCY INPUT REQUIREMENTS (Cont'd)

Design Considerations for Stable Crystal Oscillation

1. Stray capacitances should be minimized for best oscillator performance. Circuit board traces should be kept to a maximum of 1 inch, and there should be no parallel traces.
2. A signal line or power source line must not cross or go near the oscillator circuit line.
3. It is advisable to put a 0.1-microfarad capacitor between VDD and VSS of the CDP1879.

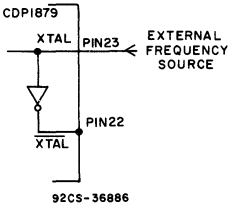

Fig. 5 - Connections for an external-frequency source applied to real-time clock.

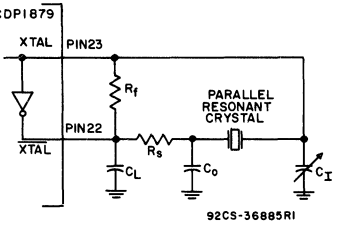

Fig. 6 - Suggested oscillator circuit applied to real-time clock (see Table III).

STANDBY (TIMEKEEPING) VOLTAGE OPERATION

When any one of the four specified crystals is used with the on-board oscillator, the Real-Time Clock can operate at a minimum of 4 volts VDD. However, at 32 kHz the clock will run (timekeeping only, no device READ/WRITE accesses) down to 3 volts at -40° to +85° C and 2.5 volts at 0° to +70° C. To achieve this low voltage operation, an external 32-kHz clock source must be supplied at the XTAL input (see Fig. 7). The standby requirements for CHIP SELECT/DESELECT are listed in Table IV, and Fig. 8 indicates the timing waveforms. Fig. 9 illustrates the typical timekeeping curve over the full temperature range.

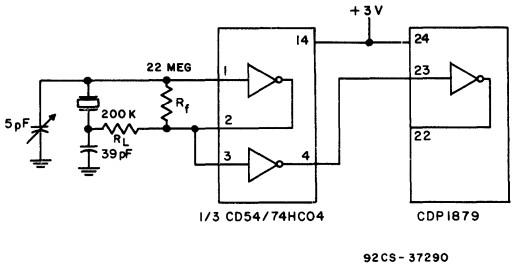

Fig. 7 - Typical external clock-source circuit.

Table IV - Standby (Timekeeping) Characteristics at Full-Temperature Range

CHARACTERISTIC		VDD (V)	VSTBY (V)	LIMITS CDP1879 Min.	LIMITS CDP1879 Max.	LIMITS CDP1879C-1 Min.	LIMITS CDP1879C-1 Max.	UNITS
Chip Deselect to Standby (Timekeeping) Voltage Time	t_{CSTBY}	5	2.5, 3	2	—	2	—	μs
		10	2.5, 3	1	—	—	—	
Recovery to Normal Operation Time	t_{RC}	5	2.5, 3	2	—	2	—	
		10	2.5, 3	1	—	—	—	

STANDBY (TIMEKEEPING) VOLTAGE OPERATION (Cont'd)

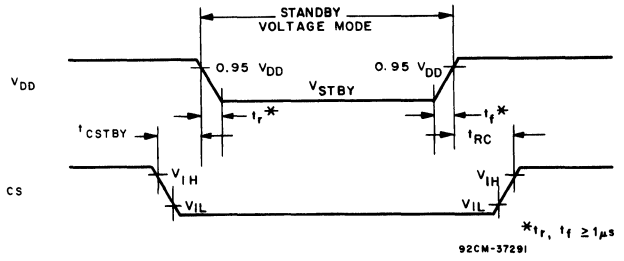

Fig. 8 - Standby (timekeeping) voltage- and timing-waveforms.

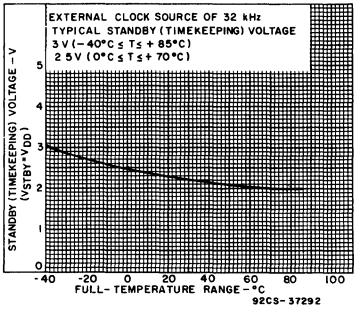

Fig. 9 - Typical standby (timekeeping) voltage vs. full-temperature range.

APPLICATIONS

A typical application for this real-time clock is as a wake-up control to a CPU to reduce total system power in intermittent-use systems. A hookup diagram illustrating this feature is shown in Fig. 10. In this configuration, the alarm and power-down features of the CDP1879 are utilized in the control of the sleep and wake-up states of the CPU. A typical shut-down/start-up sequence for this system could proceed as follows:

1. The CPU has finished a current task and will be inactive for the next six hours.
2. The CPU loads the CDP1879 alarm registers with the desired wake-up time.
3. The CDP1800 Q output is set high, which stops the CPU oscillator (as an alternative, in an NMOS system, power to all components except the clock chip could be shut off).
4. This Q output signal is received by the CDP1879 as a power-down signal.
5. The CDP1879 tri-states the interrupt output pin.
6. The CDP1879 eventually times out, and sets an alarm by driving the $\overline{INT}$ output low.
7. The alarm signal resets the CPU (to avoid oscillator start-up problems) and flags the processor for a warm-start routine.
8. The CPU, once into its normal software sequence, writes to the CDP1879 control register to reset the interrupt request.

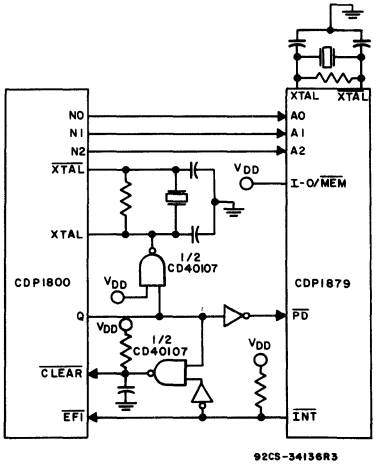

Fig. 10 - CPU wake-up circuit using the CDP1879 real-time clock.

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APPLICATIONS (Cont'd)

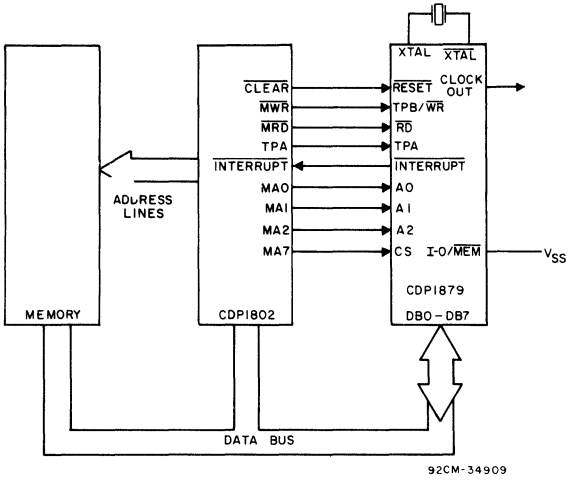

Fig. 11 - Typical CDP1802 memory-mapped system.

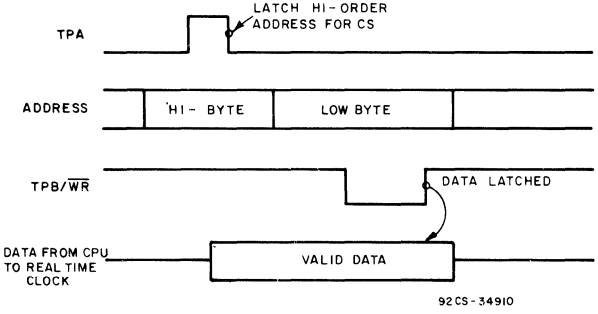

Fig. 12 - CDP1800-series memory-mapped write-cycle timing waveforms.

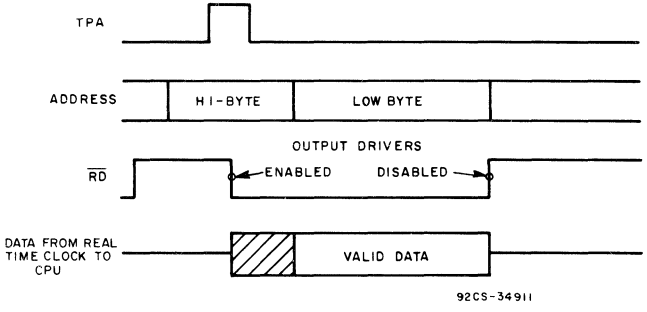

Fig. 13 - CDP1800-series memory-mapped read-cycle timing waveforms.

APPLICATIONS (Cont'd)

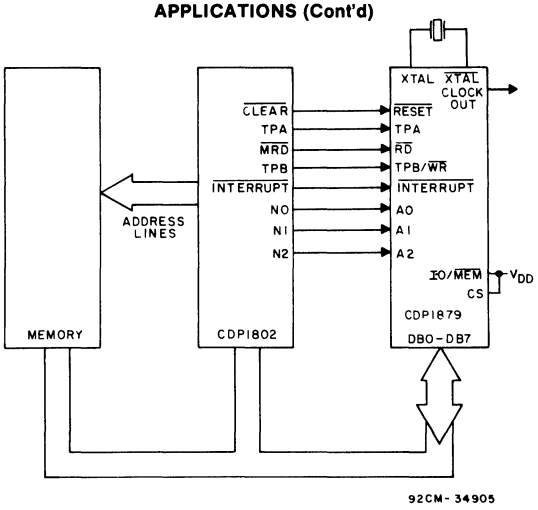

Fig. 14 - Typical CDP1802 input/output-mapped system.

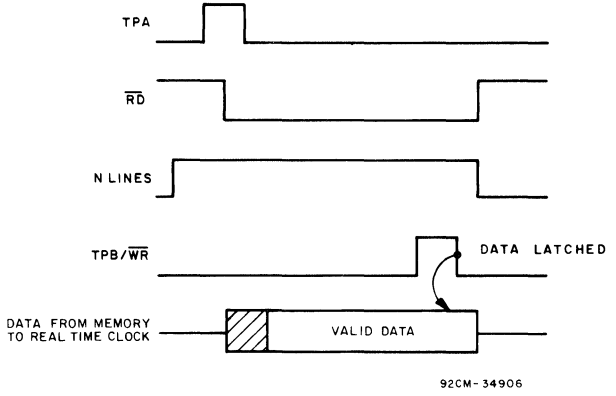

Fig. 15 - CDP1800-series input/output-mapping timing waveforms with output instruction

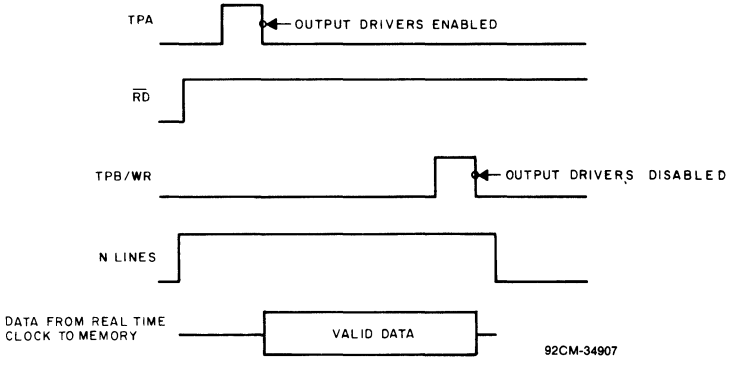

Fig. 16 - CDP1800-series input/output-mapping timing waveforms with input instruction

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DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, Input t_r,t_f = 10 ns, C_L = 50 pF

CHARACTERISTIC		V_{DD}	LIMITS				UNITS
			CDP1879		CDP1879C-1		
Read Cycle Times (see Fig. 17)		(V)	Min.†	Max.	Min.†	Max.	
Data Access from Address	tDA	5	—	400	—	400	ns
		10	—	190	—	—	
$\overline{\text{Read}}$ Pulse Width	tRD	5	270	—	270	—	
		10	160	—	—	—	
Data Access from $\overline{\text{Read}}$	tDR	5	—	375	—	375	
		10	—	170	—	—	
Address Hold after $\overline{\text{Read}}$	tRH	5	0	—	0	—	
		10	0	—	—	—	
Output Hold after $\overline{\text{Read}}$	tDH	5	50	230	50	230	
		10	40	130	—	—	
Chip Select Setup to TPA	tCS	5	50	—	50	—	
		10	30	—	—	—	

†Time required by a limit device to allow for the indicated function

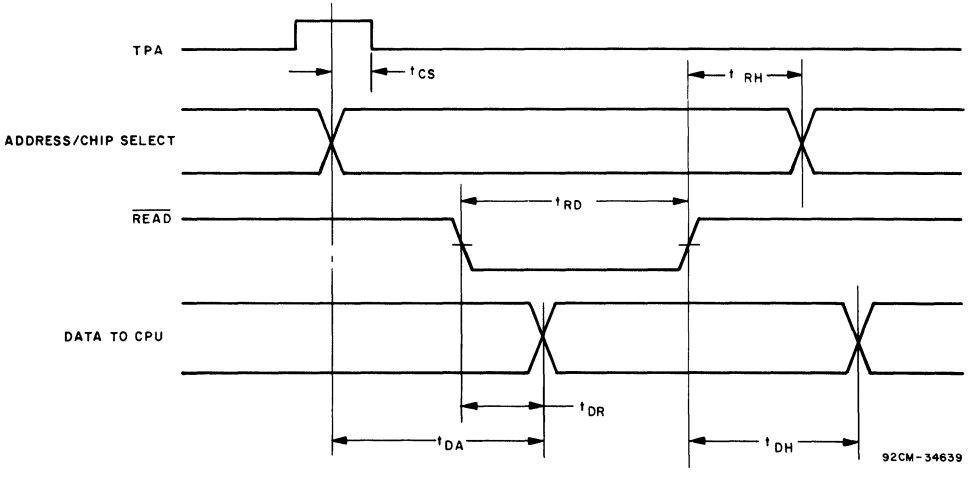

Fig. 17 - Read-cycle timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, Input t_r,t_f = 10 ns, C_L = 50 pF

CHARACTERISTIC Write Cycle Times (see Fig. 18)		V_{DD} (V)	LIMITS				UNITS
			CDP1879		CDP1879C-1		
			Min.†	Max.	Min.†	Max.	
Address Setup to $\overline{\text{Write}}$	tAS	5	225	—	225	—	ns
		10	110	—	—	—	
$\overline{\text{Write}}$ Pulse Width	tWR	5	150	—	150	—	
		10	70	—	—	—	
Data Setup to $\overline{\text{Write}}$	tDS	5	65	—	65	—	
		10	30	—	—	—	
Address Hold after $\overline{\text{Write}}$	tAH	5	0	—	0	—	
		10	0	—	—	—	
Data Hold after $\overline{\text{Write}}$	tWH	5	150	—	150	—	
		10	80	—	—	—	
Chip Select Setup to TPA	tCS	5	50	—	50	—	
		10	30	—	—	—	

†Time required by a limit device to allow for the indicated function.

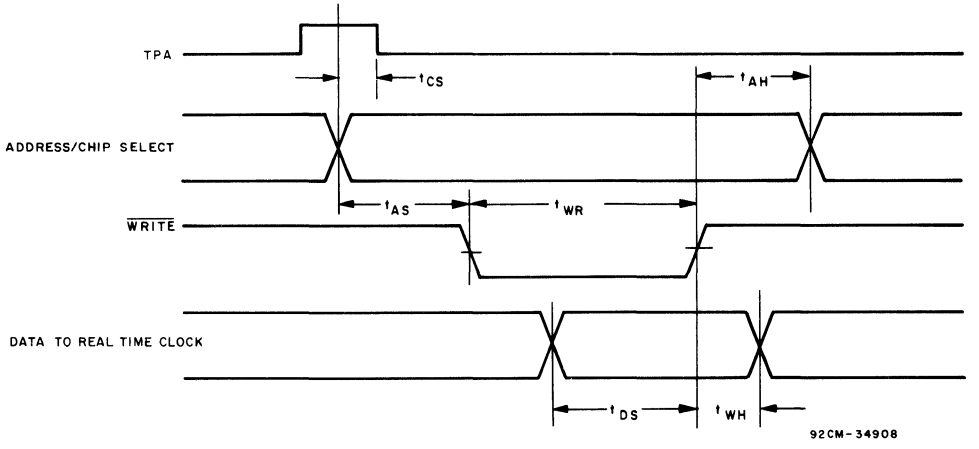

Fig. 18 - Write-cycle timing waveforms.