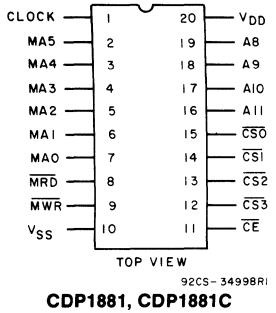
CDP1881, CDP1881C, CDP1882, CDP1882C

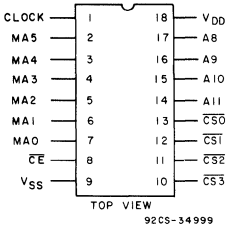
CMOS 6-Bit Latch and Decoder Memory Interfaces



CDP1881, CDP1881C TERMINAL ASSIGNMENT

Features

- *Performs memory address latch and decoder functions multiplexed or non-multiplexed*
- *Decodes up to 16 K-bytes of memory*
- *Interfaces directly with CDP1800-series microprocessors at maximum clock frequency*
- *Can replace existing CDP1866 and CDP1867 (upward speed and function capability)*



CDP1882, CDP1882C TERMINAL ASSIGNMENT

The RCA-CDP1881 and CDP1882 are CMOS 6-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to four 4K x 8-bit memories to provide a 16K-byte memory system. With four 2K x 8-bit memories an 8K-byte system can be decoded.

The devices are also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

The CDP1881 and CDP1882 are intended for use with 2K or 4K-byte RAMs and are identical except that in the CDP1882 $\overline{MWR}$ and $\overline{MRD}$ are excluded.

The CDP1881 and CDP1882 are functionally identical to the CDP1881C and the CDP1882C. They differ in that the CDP1881 and CDP1882 have a recommended operating voltage range of 4 to 10 5 volts and their C versions have a recommended operating voltage range of 4 to 6.5 volts.

The CDP1881 and CDP1882 are supplied in 20-lead and 18-lead packages, respectively. The CDP1881 is supplied only in a dual-in-line plastic package (E suffix). The CDP1882 is supplied in dual-in-line, hermetic side-brazed ceramic (D suffix) and in plastic (E suffix) packages.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal)
- CDP1881 and CDP1882 ..... -0.5 to +11 V
- CDP1881C and CDP1882C ..... -0.5 to +7 V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0 5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
- For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
- For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
- For T_A -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
- For T_A = +100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW

OPERATING-TEMPERATURE RANGE (T_A):
- PACKAGE TYPE D ..... -55 to +125°C
- PACKAGE TYPE E ..... -40 to +85°C

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C

File Number **1367**

CDP1881, CDP1881C, CDP1882, CDP1882C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range.
For maximum relibility, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1881, CDP1882		CDP1881C, CDP1882C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as noted

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
				CDP1881 CDP1882			CDP1881C CDP1882C			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current I_{DD}	—	0, 5	5	—	1	10	—	5	50	μA
	—	0, 10	10	—	10	100	—	—	—	
Output Low Drive (Sink) Current I_{OL}	0 4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0, 10	10	3.2	6 4	—	—	—	—	
Output High Drive (Source) Current I_{OH}	4.6	0, 5	5	-1.15	-2 3	—	-1.15	-2.3	—	
	9.5	0, 10	10	-2.3	-4.6	—	—	—	—	
Output Voltage Low-Level V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
	—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High-Level V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
	—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage V_{IL}	0.5, 4.5	—	5	—	—	1 5	—	—	1.5	
	1, 9	—	10	—	—	3	—	—	—	
Input High Voltage V_{IH}	0 5, 4.5	—	5	3.5	—	—	3.5	—	—	
	1, 9	—	10	7	—	—	—	—	—	
Input Leakage Current I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
		0, 10	10	—	—	±2	—	—	—	
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current I_{DD1} Δ	0, 5	0, 5	5	—	—	2	—	—	2	mA
	0, 10	0, 10	10	—	—	4	—	—	—	
Minimum Data Retention Voltage V_{DR}	V_{DD} = V_{DR}			—	2	2 4	—	2	2.4	V
Data Retention Current I_{DR}	V_{DD} = 2.4 V			—	0.01	1	—	0.5	5	μA

*Typical values are for T_A = 25° C
‡I_{OL} = I_{OH} = 1 μA
ΔOperating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with outputs open circuit. (Equivalent to typical CDP1800 system at 3.2 MHz, 5-V; and 6.4 MHz, 10-V).

CDP1881, CDP1881C, CDP1882, CDP1882C

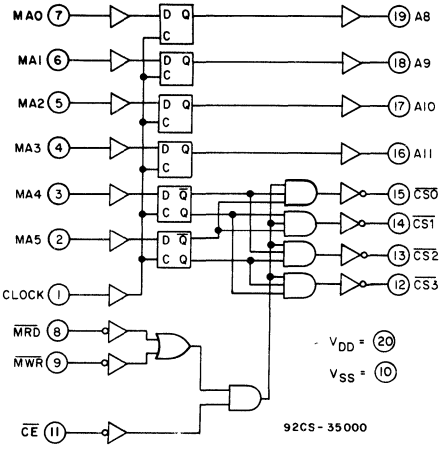


Fig. 1 - Functional diagram for the CDP1881, CDP1881C.

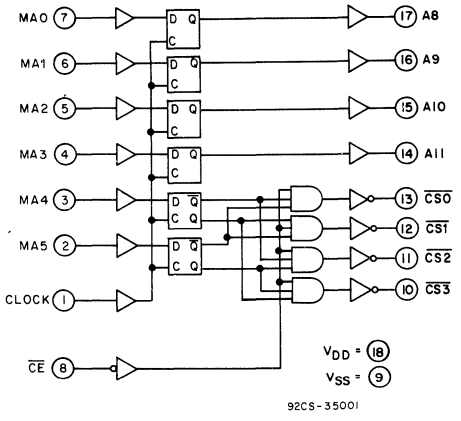


Fig. 2 - Functional diagram for the CDP1882, CDP1882C.

TRUTH TABLES for the CDP1881, CDP1881C and CDP1882, CDP1882C.

INPUTS						OUTPUTS			
$\overline{MWR}\Delta$	$\overline{MRD}\Delta$	$\overline{CE}$	CLK	MA4	MA5	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
1	1	X	X	X	X	1	1	1	1
X	X	1	X	X	X	1	1	1	1
0	X	0	1	0	0	0	1	1	1
0	X	0	1	1	0	1	0	1	1
0	X	0	1	0	1	1	1	0	1
0	X	0	1	1	1	1	1	1	0
0	X	0	0	X	X	PREVIOUS STATE			
X	0	0	1	0	0	0	1	1	1
X	0	0	1	1	0	1	0	1	1
X	0	0	1	0	1	1	1	0	1
X	0	0	1	1	1	1	1	1	0
X	0	0	0	X	X	PREVIOUS STATE			

ΔCDP1881, CDP1881C Only

INPUTS			OUTPUTS
$\overline{CE}$	CLK	MA0, MA1, MA2, MA3	A8, A9, A10, A11
X	1	1	1
X	1	0	0
X	0	X	PREVIOUS STATE

Logic 1 = High, Logic 0 = Low, X = Don't Care

CDP1881, CDP1881C, CDP1882, CDP1882C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, tr, tf = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF, See Fig. 3.

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1881, CDP1882			CDP1881C, CDP1882C			
			Min.	Typ.•	Max.Δ	Min.	Typ.•	Max.Δ	
Minimum Setup Time, Memory Address to CLOCK,	t_{MACL}	5	—	10	35	—	10	35	ns
		10	—	8	25	—	—	—	
Minimum Hold Time, Memory Address After CLOCK,	t_{CLMA}	5	—	8	25	—	8	25	
		10	—	8	25	—	—	—	
Minimum CLOCK Pulse Width	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times: $\overline{\text{Chip Enable}}$ to $\overline{\text{Chip Select}}$	t_{CECS}	5	—	75	150	—	75	150	
		10	—	45	100	—	—	—	
$\overline{\text{MRD}}$ or $\overline{\text{MWR}}$ to $\overline{\text{Chip Select}}$*	t_{MCS}	5	—	75	150	—	75	150	
		10	—	40	100	—	—	—	
CLOCK to $\overline{\text{Chip Select}}$	t_{CLCS}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
CLOCK to Address	t_{CLA}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
Memory Address to $\overline{\text{Chip Select}}$	t_{MACS}	5	—	100	175	—	100	175	
		10	—	75	125	—	—	—	
Memory Address to Address	t_{MAA}	5	—	80	125	—	80	125	
		10	—	40	60	—	—	—	

•Typical values are for T_A = 25°C.

ΔMaximum limits of minimum characteristics are the values above which all devices function.

*For the CDP1881 and CDP1881C types only.

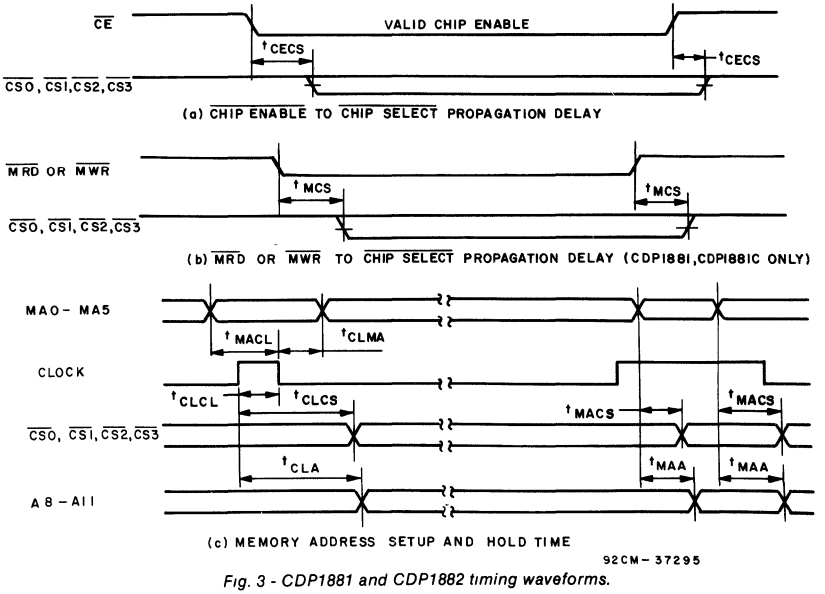


Fig. 3 - CDP1881 and CDP1882 timing waveforms.

CDP1881, CDP1881C, CDP1882, CDP1882C

SIGNAL DESCRIPTIONS/PIN FUNCTIONS

CLOCK: Latch-Input Control - a high at the clock input will allow data to pass through the latch to the output pin. Data is latched on the high to low transition of the clock input. This input is connected to TPA in CDP1800-series systems.

MA0-MA3: Address inputs to the high-byte address latches.

MA4, MA5: High-byte address inputs decoded to produce chip selects $\overline{CS0}$ - $\overline{CS3}$.

$\overline{MRD}$, $\overline{MWR}$: MEMORY READ ($\overline{MRD}$) and MEMORY WRITE ($\overline{MWR}$) signal inputs on the CDP1881, CDP1881C A low at either input, when the $\overline{CE}$ pin is low, will enable the decoder chip select outputs ($\overline{CS0}$ - $\overline{CS3}$).

$\overline{CE}$: CHIP ENABLE input - a low at the $\overline{CE}$ input of CDP1882, CDP1882C will enable the chip select decoder A low at the $\overline{CE}$ input of CDP1881, CDP1881C, coincident with a low at either the $\overline{MRD}$ or $\overline{MWR}$ pin, will enable the chip select decoder A high on this pin forces $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ to a high (false) state.

A8-A11: Latched high-byte address outputs.

$\overline{CS0}$-$\overline{CS3}$: One of four latched and decoded Chip Select outputs.

V_{DD}, V_{SS}: Power and ground pins, respectively.

APPLICATION INFORMATION

The CDP1881 and CDP1882 can interface directly with the multiplexed address bus of the CDP1800-series microprocessor family at maximum clock frequency. A single CDP1881 or CDP1882 is capable of decoding up to 16K-bytes of memory.

The CDP1881 is provided with $\overline{MRD}$ and $\overline{MWR}$ inputs for controlling bus contention, and is especially useful for interfacing with RAMs that do not have an output enable function ($\overline{OE}$). Fig. 4 shows the CDP1881 in a minimum system configuration which includes the CDP1833 ROM (1K x 8) and two 2K x 8 RAMS. The CDP1881, in this example performs the following functions:

(1) Latch and decode high-order address bits for use as chip selects.
(2) Gate chip selects with $\overline{MRD}$ and $\overline{MWR}$ to prevent bus contention with the CPU
(3) Latch high-order address bits A8 to A11.

A system using the CDP1882 is shown in Fig. 5. The CDP1882 performs the memory address latch and decoder functions. Note that the RAM has an output enable ($\overline{OE}$) pin which eliminates the need for $\overline{MRD}$ and $\overline{MWR}$ inputs on the latch/decoder. Instead, the $\overline{MRD}$ line is connected directly to the RAM output enable ($\overline{OE}$) pin

In Fig. 6 the CDP1882 is used to decode a 16K-byte ROM system consisting of four CDM5332s.

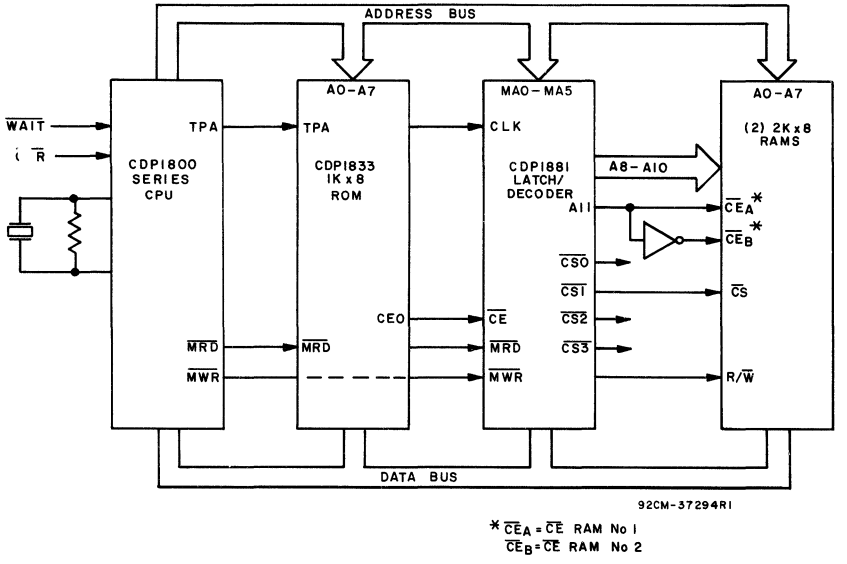


Fig. 4 - Minimum 1800-system using the CDP1881

CDP1881, CDP1881C, CDP1882, CDP1882C

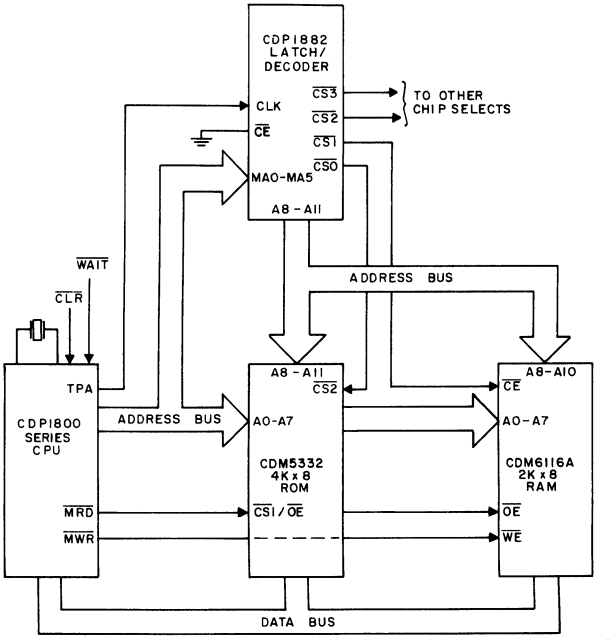


Fig. 5 - CDP1800-series system using the CDP1882.

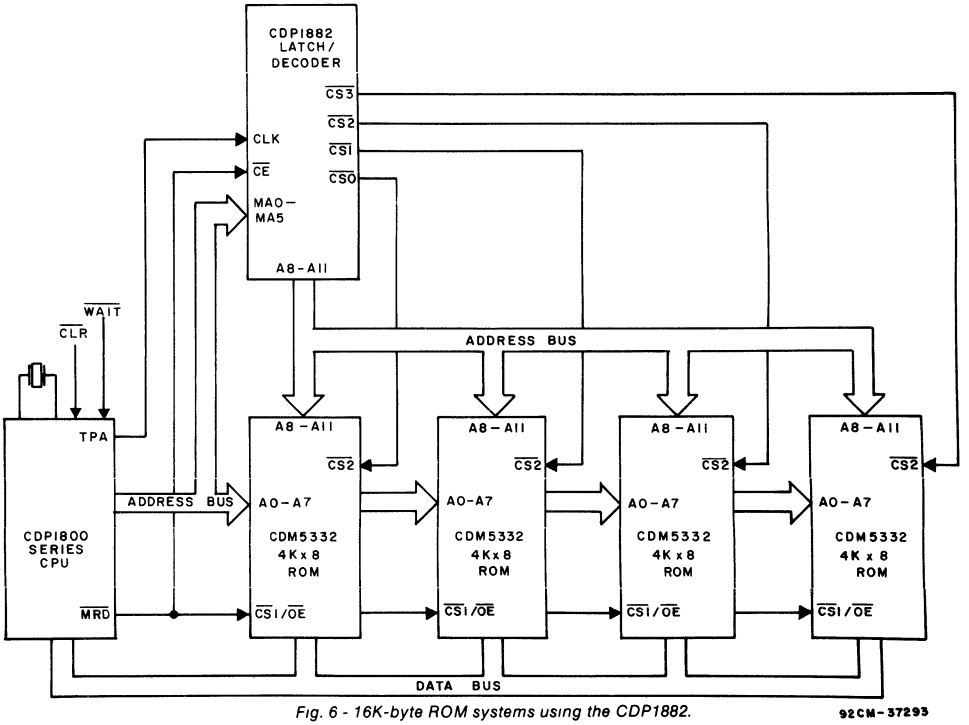


Fig. 6 - 16K-byte ROM systems using the CDP1882.