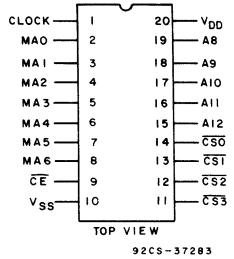
CDP1883, CDP1883C



CDP1883, CDP1883C TERMINAL ASSIGNMENT

CMOS 7-Bit Latch and Decoder Memory Interfaces

Features:

- *Performs memory address latch and decoder functions multiplexed or non-multiplexed*
- *Interfaces directly with the CDP1800-series microprocessors*
- *Allows decoding for systems up to 32K bytes*

The RCA-CDP1883 is a CMOS 7-bit memory latch and decoder circuit intended for use in CDP1800-series microprocessor systems It can serve as a direct interface between the multiplexed address bus of this system and up to four 8K x 8-bit memories to implement a 32K-byte memory system With four 4K x 8-bit memories, a 16K-byte system can be decoded

The device is also compatible with non-multiplexed address bus microprocessors By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications

The CDP1833 is compatible with CDP1800-series microprocessors operating at maximum clock frequency.

The CDP1883 and CDP1883C are functionally identical. They differ in that the CDP1883 has a recommended operating voltage range of 4 to 10.5 volts and the C version has a recommended operating voltage range of 4 to 6.5 volts

The CDP1883 and CDP1883C are supplied in 20-lead, dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY—VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal)
CDP1883 ..... -0 5 to +11 V
CDP1883C ..... -0 5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0 5 to V_{DD} +0 5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A=-40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A=FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPE E ..... -40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in (1 59 ± 0 79 mm) from case for 10 s max ..... +265°C

File Number **1507**

CDP1883, CDP1883C

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1883		CDP1883C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} ± 5%, Except as Noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1883			CDP1883C			
					Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Quiescent Device Current	I_{DD}	— —	0, 5 0, 10	5 10	— —	1 10	10 100	— —	5 —	50 —	μA
Output Low Drive (Sink) Current	I_{OL}	0.4 0.5	0, 5 0, 10	5 10	1.6 3.2	3.2 6.4	— —	1.6 —	3.2 —	— —	mA
Output High Drive (Source) Current	I_{OH}	4.6 9.5	0, 5 0, 10	5 10	-1.15 -2.3	-2.3 -4.6	— —	-1.15 —	-2.3 —	— —	
Output Voltage Low-Level	V_{OL}‡	— —	0, 5 0, 10	5 10	— —	0 0	0.1 0.1	— —	0 —	0.1 —	V
Output Voltage High-Level	V_{OH}‡	— —	0, 5 0, 10	5 10	4.9 9.9	5 10	— —	4.9 —	5 —	— —	
Input Low Voltage	V_{IL}	0.5, 4.5 0.5, 9.5	— —	5 10	— —	— —	1.5 3	— —	— —	1.5 —	
Input High Voltage	V_{IH}	0.5, 4.5 0.5, 9.5	— —	5 10	3.5 7	— —	— —	3.5 —	— —	— —	
Input Leakage Current	I_{IN}	Any Input	0, 5 0, 10	5 10	— —	— —	±1 ±2	— —	— —	±1 —	μA
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current	I_{DD1}Δ	0, 5 0, 10	0, 5 0, 10	5 10	— —	— —	2 4	— —	— —	2 —	mA
Minimum Data Retention Voltage	V_{DR}	$V_{DD} = V_{DR}$			—	2	2.4	—	2	2.4	V
Data Retention Current	I_{DR}	V_{DD} = 2 4 V			—	0.01	1	—	0.5	5	μA

*Typical values are for T_A = 25° C

‡I_{OL} = I_{OH} = 1 μA

ΔOperating current is measured at 200 kHz for V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with outputs open circuit.

CDP1883, CDP1883C

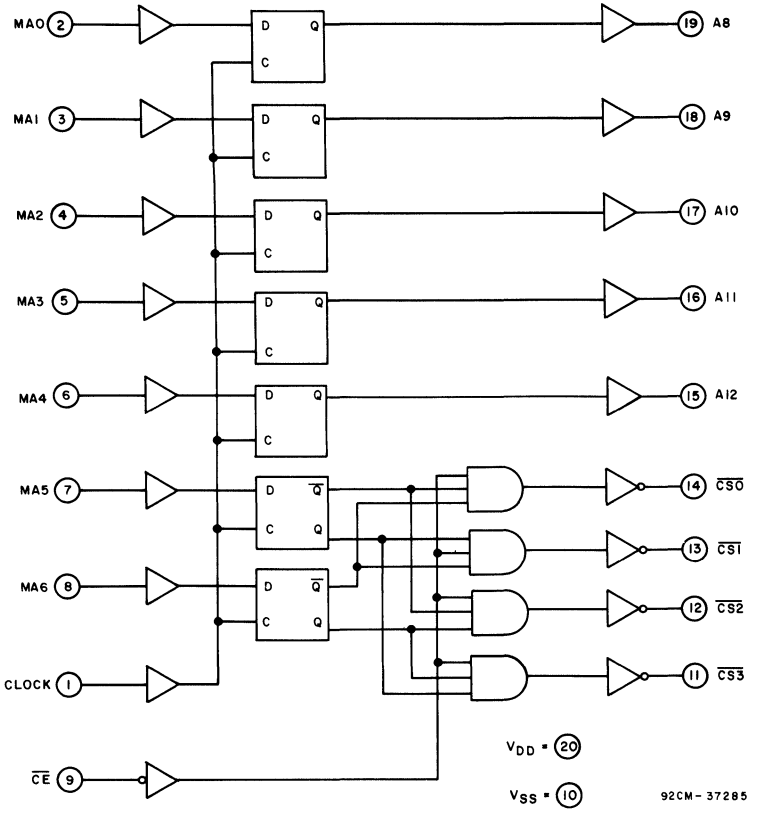


Fig. 1 - Functional diagram for the CDP1883, CDP1883C.

SIGNAL DESCRIPTIONS/PIN FUNCTIONS

CLOCK: Latch Input Control—a high on the clock input will allow data to pass through the latch to the output pin Data is latched on the high-to-low transition of the clock input. This pin is connected to TPA in the CDP1800 system and tied to V_{DD} for other applications.

MA0-MA4: address inputs to the high byte address latches

MA5-MA6: high byte address inputs decoded to produce chip selects $\overline{CS0}$-$\overline{CS3}$

$\overline{CE}$: CHIP ENABLE input A low on this pin will enable the chip select decoder. A high on this pin forces the $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and $\overline{CS3}$ outputs to a high (false) state.

A8-A12: latched high-byte address outputs.

$\overline{CS0}$-$\overline{CS3}$: one of four latched and decoded Chip Select outputs.

V_{DD}, V_{SS}: power and ground pins, respectively.

TRUTH TABLES FOR CDP1883, CDP1833C

INPUTS				OUTPUTS			
$\overline{CE}$	CLK	MA5	MA6	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
0	1	0	0	0	1	1	1
0	1	1	0	1	0	1	1
0	1	0	1	1	1	0	1
0	1	1	1	1	1	1	0
0	0	X	X	PREVIOUS STATE			
1	X	X	X	1	1	1	1

INPUTS			OUTPUTS
$\overline{CE}$	CLK	MA0-4	A8-A12
X	1	1	1
X	1	0	0
X	0	X	PREVIOUS STATE

X = DON'T CARE

CDP1883, CDP1883C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ± 5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF. See Fig. 2.

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1883			CDP1883C			
			Min.	Typ.•	Max.Δ	Min.	Typ.•	Max.Δ	
Minimum Setup Time, Memory Address to CLOCK	t_{MACL}	5	—	10	35	—	10	35	ns
		10	—	8	25	—	—	—	
Minimum Hold Time, Memory Address After CLOCK	t_{CLMA}	5	—	8	25	—	8	25	
		10	—	8	25	—	—	—	
Minimum CLOCK Pulse Width	t_{CLCL}	5	—	50	75	—	50	75	
		10	—	25	40	—	—	—	
Propagation Delay Times: $\overline{\text{Chip Enable}}$ to $\overline{\text{Chip Select}}$	t_{CECS}	5	—	75	150	—	75	150	
		10	—	45	100	—	—	—	
CLOCK to $\overline{\text{Chip Select}}$	t_{CLCS}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
CLOCK to Address,	t_{CLA}	5	—	100	175	—	100	175	
		10	—	65	125	—	—	—	
Memory Address to $\overline{\text{Chip Select}}$	t_{MACS}	5	—	100	175	—	100	175	
		10	—	75	125	—	—	—	
Memory Address to Address	t_{MAA}	5	—	80	125	—	80	125	
		10	—	40	60	—	—	—	

•Typical values are for T_A = 25° C
ΔMaximum limits of minimum characteristics are the values above which all devices function

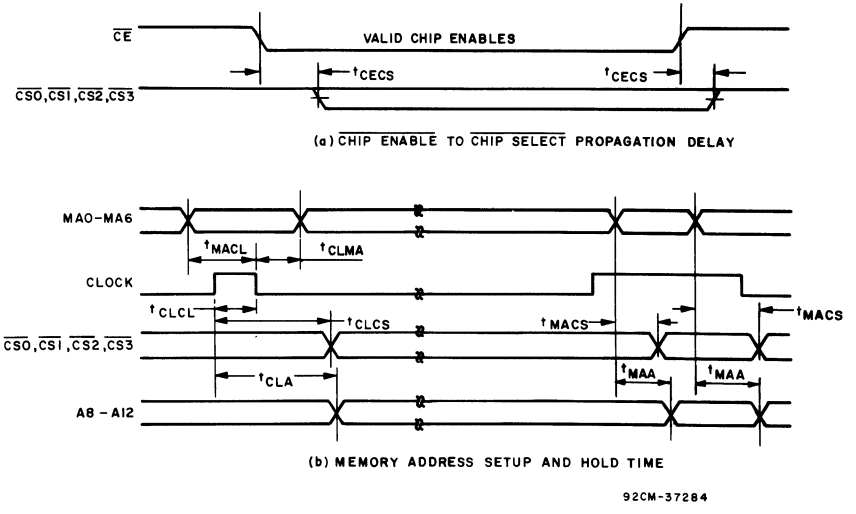


Fig. 2 - CDP1883 timing waveforms.

CDP1883, CDP1883C

APPLICATION INFORMATION

The CDP1883 and CDP1883C can be interfaced, without external components, with CDP1800-series microprocessor systems. These microprocessors feature a multiplexed address bus and provide an address latch signal (TPA) that is used as the Clock input of the CDP1883

This signal is used to latch 7 bits of the high-order address. The lower five high-order address inputs are latched and held to be used with the eight lower-order address inputs to access an 8K x 8-bit memory. The two upper high-order address inputs are latched and decoded for use as chip selects.

The latched address and decoding functions of the CDP1883 and CDP1883C allow them to operate with 32K-byte memory systems. In addition, smaller memory systems can be configured with 4K x 8-bit or smaller memories, or a mix of memory sizes up to 8K x 8-bit.

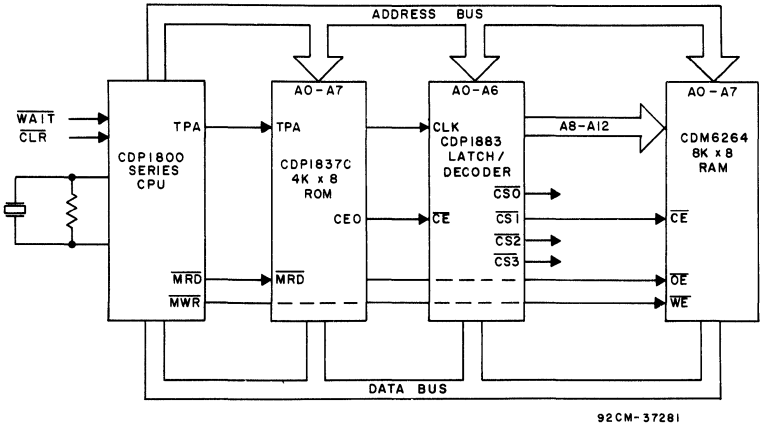


Fig. 3 - Minimum 1800-system using the CDP1883 to interface with an 8K x 8-bit memory.

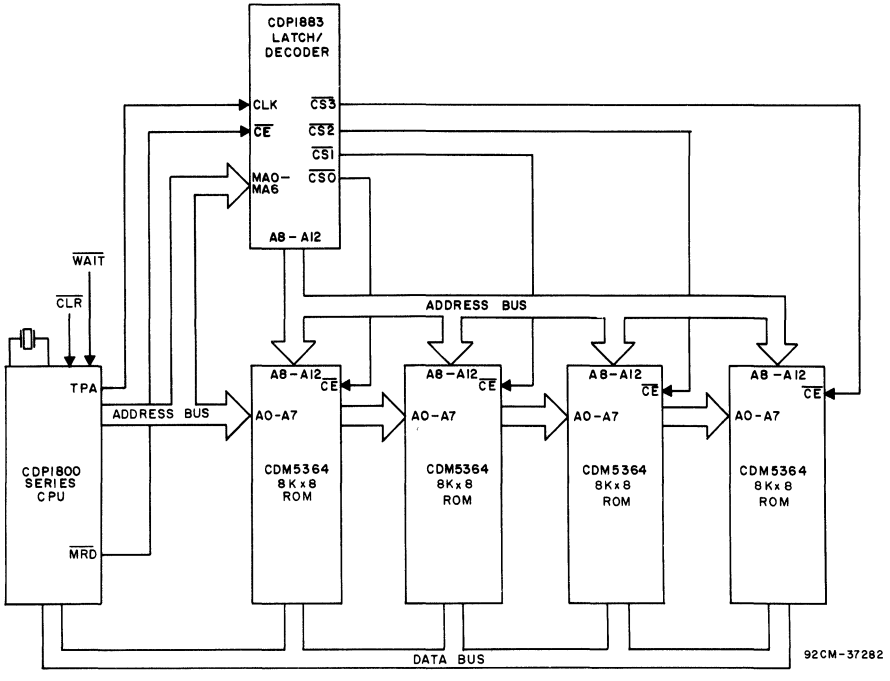


Fig 4 - 32K-byte ROM system using the CDP1883.