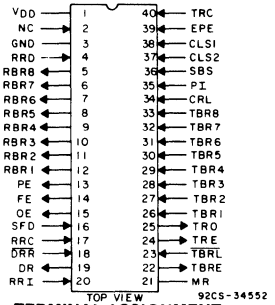
CDP6402, CDP6402C



TERMINAL ASSIGNMENT

CMOS Universal Asynchronous Receiver/Transmitter (UART)

Features:

- Low-power CMOS circuitry — 7.5 mW typ. at 3.2 MHz (max. freq.) at V_{DD} = 5 V
- *Baud rate - DC to 200K bits/sec (max.) at V_{DD} = 5 V, 85°C*
  DC to 400K bits/sec (max.) at V_{DD} = 10 V, 85°C
- *4 V to 10.5 operation*
- *Automatic data formatting and status generation*
- *Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1.5,or 2 stop bits*
- *Operating-temperature range: (CDP6402D, CD) -55 to +125° (CDP6402E, CE) -40 to +85° C*
- *Replaces industry types IM6402 and HD6402*

The RCA CDP6402 and CDP6402C are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits for interfacing computers or microprocessors to asynchronous serial data channels. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data channels. The receiver converts serial start, data, parity, and stop bits to parallel data verifying proper code transmission, parity and stop bits. The transmitter converts parallel data into serial form and automatically adds start parity and stop bits.

The data word can be 5, 6, 7 or 8 bits in length. Parity may be odd, even or inhibited. Stop bits can be 1, 1.5, or 2 (when transmitting 5-bit code).

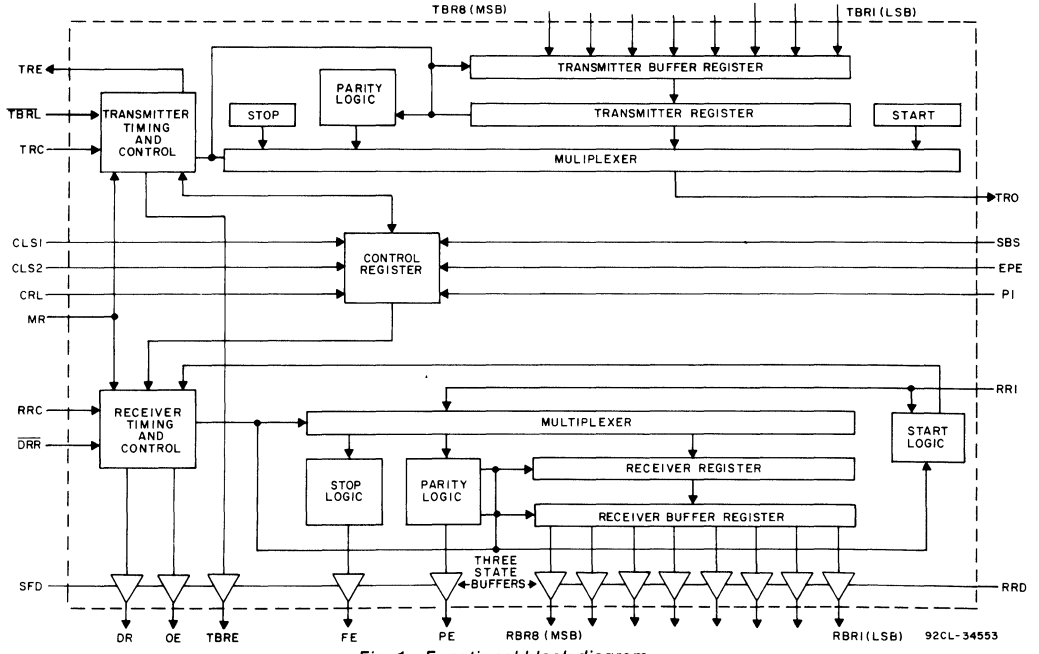


Fig. 1 - Functional block diagram.

4

File Number **1328**

CDP6402, CDP6402C

The CDP6402 and CDP6402C can be used in a wide range of applications including modems, printers, peripherals, video terminals, remote data acquisition systems, and serial data links for distributed processing systems.

The CDP6402 and CDP6402C are functionally identical. They differ in that the CDP6402 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP6402C has a recommended operating voltage range of 4 to 6.5 volts. Both types are supplied in 40-lead dual-in-line ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal)
CDP6402 ..... -0.5 to +11 V
CDP6402C ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 100 μA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Lineary at 12 mW/° C to 200 mW
For T_A = -55 to 100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = + 100 to +125° C (PACKAGE TYPE D) ..... Derate Lineary at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A).
PACKAGE TYPE D ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0 79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP6402		CDP6402C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85° C, V_{DD} ±10%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP6402			CDP6402C			
					Min.	Typ.•	Max.	Min.	Typ.•	Max.	
Quiescent Device Current	I_{DD}	— —	0, 5 0, 10	5 10	— —	0.01 1	50 200	— —	0.02 —	200 —	μA
Output Low Drive (Sink) Current	I_{OL}	0.4 0.5	0, 5 0, 10	5 10	2 5	4 7	— —	1.2 —	2.4 —	— —	mA
Output High Drive (Source) Current	I_{OH}	4.6 9.5	0, 5 0, 10	5 10	-0.55 -1.3	-1.1 -2.6	— —	-0.55 —	-1.1 —	— —	
Output Voltage Low-Level	V_{OL}‡	— —	0, 5 0, 10	5 10	— —	0 0	0.1 0.1	— —	0 —	0.1 —	V
Output Voltage High Level	V_{OH}‡	— —	0, 5 0, 10	5 10	4.9 9.9	5 10	— —	4.9 —	5 —	— —	
Input Low Voltage	V_{IL}	0.5, 4.5 0.5, 9.5	— —	5 10	— —	— —	0.8 0.2 V_{DD}	— —	— —	0.8 —	
Input High Voltage	V_{IH}	0.5, 4.5 0.5, 9.5	— —	5 10	V_{DD}-2 7	— —	— —	V_{DD}-2 —	— —	— —	
Input Leakage Current	I_{IN}	Any Input	0, 5 0, 10	5 10	— —	±10^{-4} ±10^{-4}	±1 ±2	— —	— —	±1 —	μA
3-State Output Leakage Current	I_{OUT}	0, 5 0, 10	0, 5 0, 10	5 10	— —	±10^{-4} ±10^{-4}	±1 ±10	— —	±10^{-4} —	±1 —	
Operating Current,	I_{DD1}‡	— —	0, 5 0, 10	5 10	— —	1.5 10	— —	— —	1.5 —	— —	mA
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	

•Typical values are for T_A=25° C and nominal V_{DD}. ‡I_{OL}=I_{OH}=1 μA.

#Operating current is measured at 200 kHz or V_{DD} = 5 V and 400 kHz for V_{DD} = 10 V, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2 MHz).

DESCRIPTION OF OPERATION

Initialization and Controls

A positive pulse on the MASTER RESET (MR) input resets the control, status, and receiver buffer registers, and sets the serial output (TRO) High. Timing is generated from the clock inputs RRC and TRC at a frequency equal to 16 times the serial data bit rate. The RRC and TRC inputs may be driven by a common clock, or may be driven independently by two different clocks. The CONTROL REGISTER LOAD (CRL) input is strobed to load control bits for PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECTS (SBS), and CHARACTER LENGTH SELECTS (CLS1 and CLS2). These inputs may be hand wired to V_{SS} or V_{DD} with CRL to V_{DD}. When the initialization is completed, the UART is ready for receiver and/or transmitter operations.

Transmitter Operation

The transmitter section accepts parallel data, formats it, and transmits it in serial form (Fig. 2) on the TRO terminal.

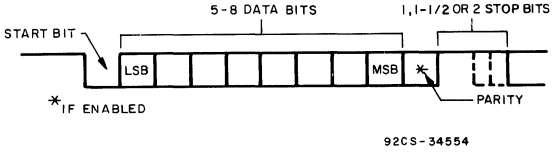


Fig. 2 - Serial data format.

Transmitter timing is shown in Fig. 3. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{TBRL}$ input. Valid data must be present at least t_{DT} prior to, and t_{TD} following, the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of $\overline{TBRL}$ clears TBRE. ½ to 1½ cycles later, depending on when the $\overline{TBRL}$ pulse occurs with respect to TRC, data is transferred to the transmitter register and TRE is cleared. TBRE is set to a logic High one cycle after that.

Output data is clocked by TRC. The clock rate is 16 times the data rate. (C) A second pulse on $\overline{TBRL}$ loads data into the transmitter buffer register Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins.

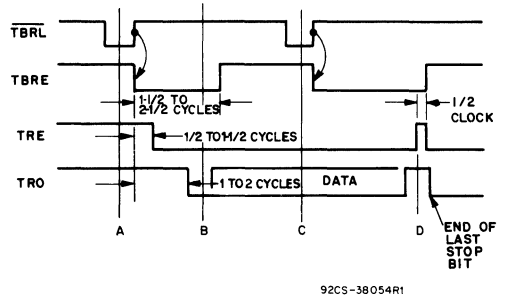


Fig. 3 - Transmitter timing waveforms.

Receiver Operation

Data is received in serial form at the RRI input. When no data is being received, RRI input must remain high. The data is clocked through the RRC. The clock rate is 16 times the data rate. Receiver timing is shown in Fig. 4.

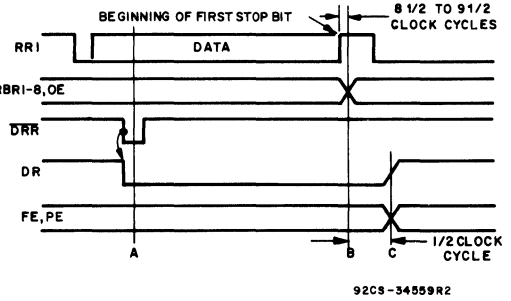


Fig. 4 - Receiver timing waveforms.

(A) A low level on $\overline{DRR}$ clears the DR line. (B) During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OE indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. (C) 1/2 clock cycle later DR is set to a logic high and FE is evaluated. A logic high on FE indicates an invalid stop bit was received A logic high on PE indicates a parity error.

Start Bit Detection

The receiver uses a 16X clock for timing (Fig. 5) The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7 1/2. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at 9 clocks into the first stop bit.

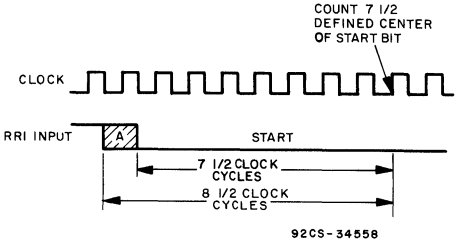


Fig. 5 - Start bit timing waveforms.

CDP6402, CDP6402C

Table I - Control Word Function

CONTROL WORD							
CLS2	CLS1	PI	EPE	SBS	DATA BITS	PARITY BIT	STOP BIT(S)
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

Table II - Function Pin Definition

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	N/C	No Connection
3	GND	Ground (V_{SS})
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register ouputs RBR1-RBR8 to a high impedance state
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs Word formats less than 8 characters are right justified to RBR1
6	RBR7	See Pin 5 - RBR8
7	RBR6	
8	RBR5	
9	RBR4	
10	RBR3	
11	RBR2	
12	RBR1	
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits The output is active until parity matches on a succeeding character When parity is inhibited, this output is low
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (i.e., DRR; active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE and DR, and sets TRE, TBRE, and TRO. TRE is actually set on the first rising edge of TRC after MR goes high. MR should be strobed after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.

Table II - Function Pin Definition (Cont'd)

PIN	SYMBOL	DESCRIPTION
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8 For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length
27	TBR2	See Pin 26 - TBR1
28	TBR3	
29	TBR4	
30	TBR5	
31	TBR6	
32	TBR7	
33	TBR8	

PIN	SYMBOL	DESCRIPTION
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits).
38	CLS1*	See Pin 37 - CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity A low level selects odd parity
40	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table I (Control Word Function)

4

CDP6402, CDP6402C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC †		V_{DD} (V)	LIMITS				UNITS
			CDP6402		CDP6402C		
			Typ.•	Max.Δ	Typ.•	Max.Δ	
System Timing (See Fig. 6)							
Minimum Pulse Width: CRL	t_{CRL}	5 10	50 40	150 100	50 —	150 —	ns
Minimum Setup Time Control Word to CRL	t_{CWC}	5 10	20 0	50 40	20 —	50 —	
Minimum Hold Time Control Word after CRL	t_{CCW}	5 10	40 20	60 30	40 —	60 —	
Propagation Delay Time SFD High to SOD	t_{SFDH}	5 10	130 100	200 150	130 —	200 —	
SFD Low to SOD	t_{SFDL}	5 10	130 40	200 60	130 —	200 —	
RRD High to Receiver Register High Impedance	t_{RRDH}	5 10	80 40	150 70	80 —	150 —	
RRD Low to Receiver Register Active	t_{RRDL}	5 10	80 40	150 70	80 —	150 —	
Minimum Pulse Width: MR		5 10	200 100	400 200	200 —	400 —	

•Typical values for T_A = 25°C and nominal V_{DD}.

ΔMaximum limits of minimum characteristics are the values above which all devices function.

†All measurements are made at the 50% point of the transition except tri-state measurements

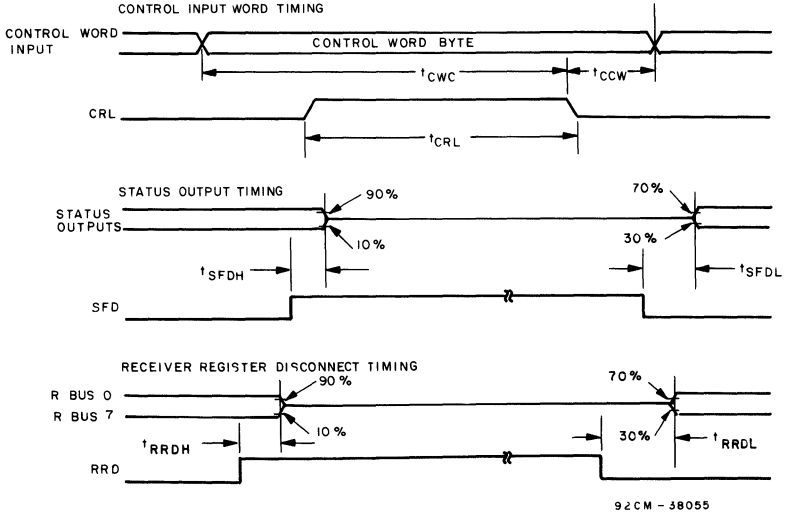


Fig. 6 - System timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC †		V_{DD} (V)	LIMITS CDP6402 Typ.•	CDP6402 Max.Δ	CDP6402C Typ.•	CDP6402C Max.Δ	UNITS
Transmitter Timing (See Fig. 7)							
Minimum Clock Period (TRC)	t_{CC}	5 10	250 125	310 155	250 —	310 —	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 —	125 —	
Clock High Level	t_{CH}	5 10	100 75	125 100	100 —	125 —	
$\overline{TBRL}$	t_{THTH}	5 10	80 40	200 100	80 —	200 —	
Minimum Setup Time: $\overline{TBRL}$ to Clock	t_{THC}	5 10	175 90	275 150	175 —	275 —	
Data to $\overline{TBRL}$ ↗	t_{DT}	5 10	20 0	50 40	20 —	50 —	
Minimum Hold Time: Data after $\overline{TBRL}$ ↗	t_{TD}	5 10	40 20	60 30	40 —	60 —	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5 10	300 150	450 225	300 —	450 —	
Clock to TBRE	t_{CT}	5 10	330 100	400 150	330 —	400 —	
$\overline{TBRL}$ to TBRE	t_{TTHR}	5 10	200 100	300 150	200 —	300 —	
Clock to TRE	t_{TTS}	5 10	330 100	400 150	330 —	400 —	

•Typical values for T_A = 25°C and nominal V_{DD}.

ΔMaximum limits of minimum characteristics are the values above which all devices function.

†All measurements are made at the 50% point of the transition except tri-state measurements.

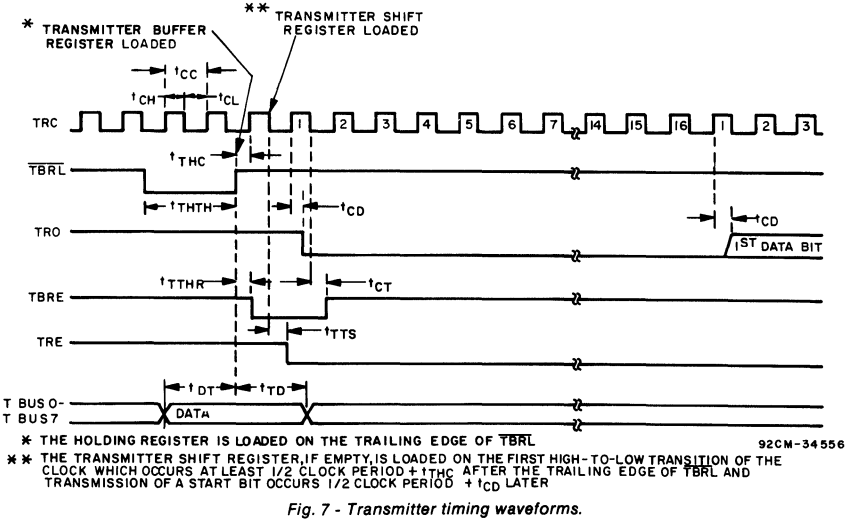


Fig. 7 - Transmitter timing waveforms.

CDP6402, CDP6402C

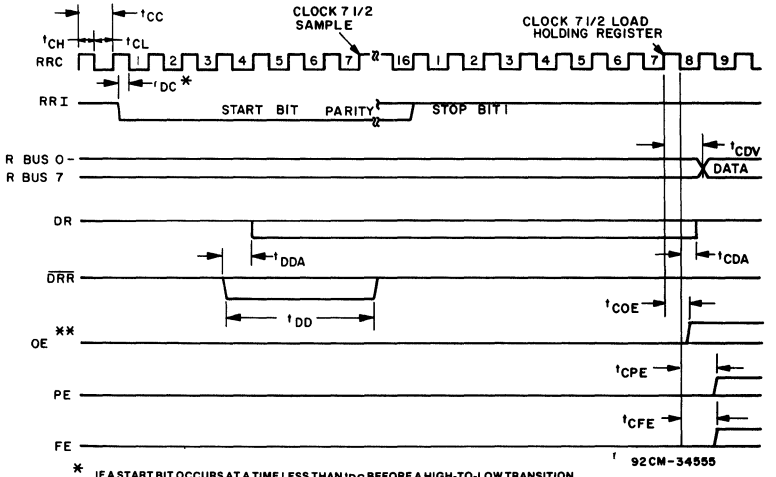
DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC †		V_{DD} (V)	LIMITS CDP6402 Typ.•	CDP6402 Max.Δ	CDP6402C Typ.•	CDP6402C Max.Δ	UNITS
Receiver Timing (See Fig. 8)							
Minimum Clock Period (RRC)	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width:							
Clock Low Level	t_{CL}	5	100	125	100	125	
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	
		10	75	100	—	—	
$\overline{\text{DATA RECEIVED RESET}}$	t_{DD}	5	50	75	50	75	
		10	25	40	—	—	
Minimum Setup Time:							
Data Start Bit to Clock	t_{DC}	5	100	150	100	150	
		10	50	75	—	—	
Propagation Delay Time:							
$\overline{\text{DATA RECEIVED RESET}}$ to Data Received	t_{DDA}	5	150	250	150	250	
		10	75	125	—	—	
Clock to Data Valid	t_{CDV}	5	275	400	275	400	
		10	110	175	—	—	
Clock to DR	t_{CDA}	5	275	400	275	400	
		10	110	175	—	—	
Clock to Overrun Error	t_{COE}	5	275	400	275	400	
		10	100	150	—	—	
Clock to Parity Error	t_{CPE}	5	240	375	240	375	
		10	120	175	—	—	
Clock to Framing Error	t_{CFE}	5	200	300	200	300	
		10	100	150	—	—	

•Typical values for T_A = 25°C and nominal V_{DD}.

ΔMaximum limits of minimum characteristics are the values above which all devices function.

†All measurements are made at the 50% point of the transition except tri-state measurements.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE

Fig. 8 - Receiver timing waveforms.