CDP6805E2, CDP6805E2C, CDP6805E3, CDP6805E3C

March 1998

CMOS 8-Bit Microprocessor

Hardware Features

- **Full Speed Operating Power @ 5V . . . . . 35mW(Typ)**
- **Wait Mode Power . . . . . 5mW(Typ)**
- **Stop Mode Power . . . . . 25μW(Typ)**
- **112 Bytes of On-Chip RAM**
- **16 Bidirectional I/O Lines on CDP6805E2**
- **13 Bidirectional I/O Lines on CDP6805E3**
- **Internal 8-Bit Timer with Software Programmable 7-Bit Prescaler**
- **External Timer Input**
- **Full External and Timer Interrupts**
- **Multiplexed Address/Data Bus**
- **Master Reset and Power-On Reset**
- **CDP6805E2 is Capable of Addressing up to 8K Bytes of External Memory**
- **CDP6805E3 is Capable of Addressing up to 64K Bytes of External Memory**
- **Single 3V to 6V Supply**
- **On-Chip Oscillator**
- **40 Pin Dual-in-Line Package (E Suffix)**
- **44 Lead Plastic Chip Carrier Package (Q Suffix)**
- **-40^{o}C to +85^{o}C Operation with CDP6805E2C and CDP6805E3C**

Software Features

- **Efficient Use of Program Space**
- **Versatile Interrupt Handling**
- **True Bit Manipulation**
- **Addressing Modes with Indexed Addressing for Tables**
- **Efficient Instruction Set**
- **Memory Mapped I/O**
- **Two Power Saving Standby Modes**

Description

The CDP6805E2 and CDP6805E3 Microprocessors Unit (MPUs) belong to the CDP6805 Family of CMOS Microcomputers. These 8-bit fully static and expandable microprocessors contain a CPU, on-chip RAM, I/O and Timer. They are low power, low cost processors designed for mid-range applications in the consumer, automotive, industrial and communications markets where very low power consumption constitutes an important factor. The major features of the CDP6805E2 and CDP6805E3 MPUs are listed under “Hardware Features” and “Software Features”.

Ordering Information

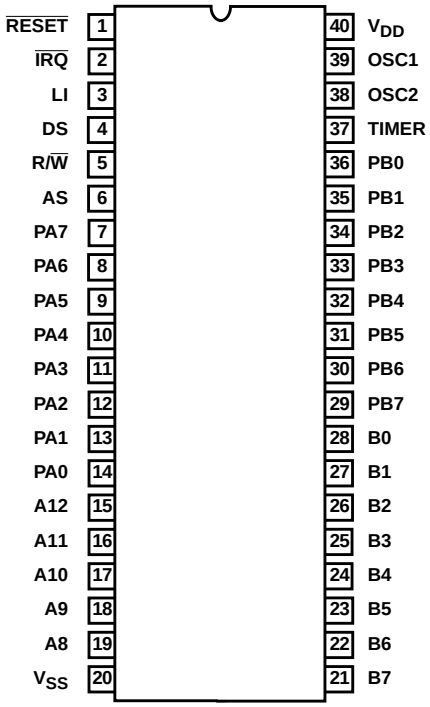
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CDP6805E2E	0 to 70	40 Ld PDIP	E40.6
CDP6805E3E	0 to 70	40 Ld PDIP	E40.6
CDP6805E2CE	-40 to 85	40 Ld PDIP	E40.6
CDP6805E3CE	-40 to 85	40 Ld PDIP	E40.6
CDP6805E2	0 to 70	44 Ld PLCC	N44.65
CDP6805E3	0 to 70	44 Ld PLCC	N44.65
CDP6805E2C	-40 to 85	44 Ld PLCC	N44.65
CDP6805E3C	-40 to 85	44 Ld PLCC	N44.65

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

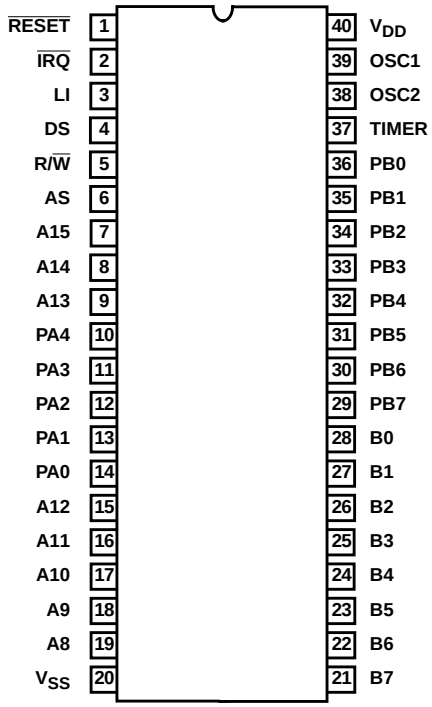
File Number **2746.3**

Pinouts

CDP6805E2 (PDIP)
TOP VIEW

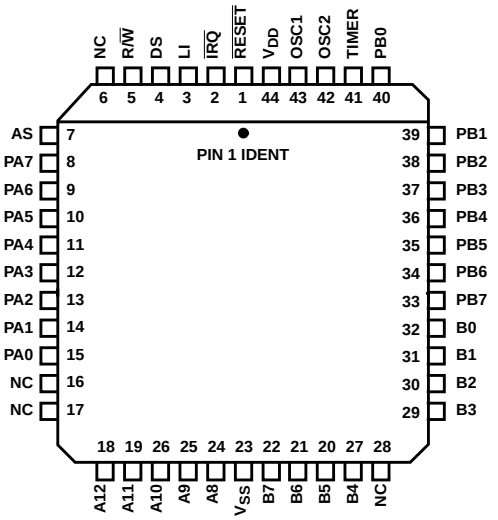


CDP6805E3 (PDIP)
TOP VIEW

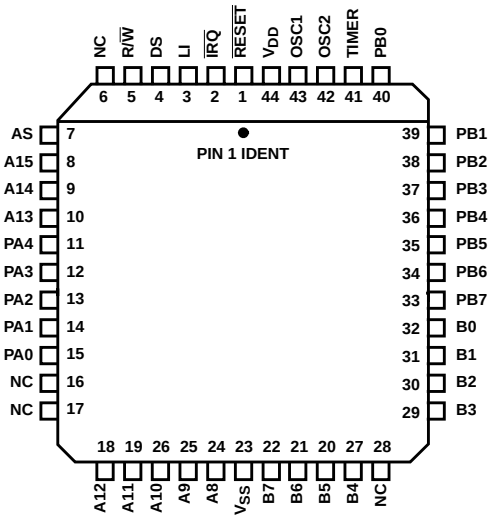


Pinouts (Continued)

CDP6805E2 (PLCC)
TOP VIEW



CDP6805E3 (PLCC)
TOP VIEW



Block Diagrams

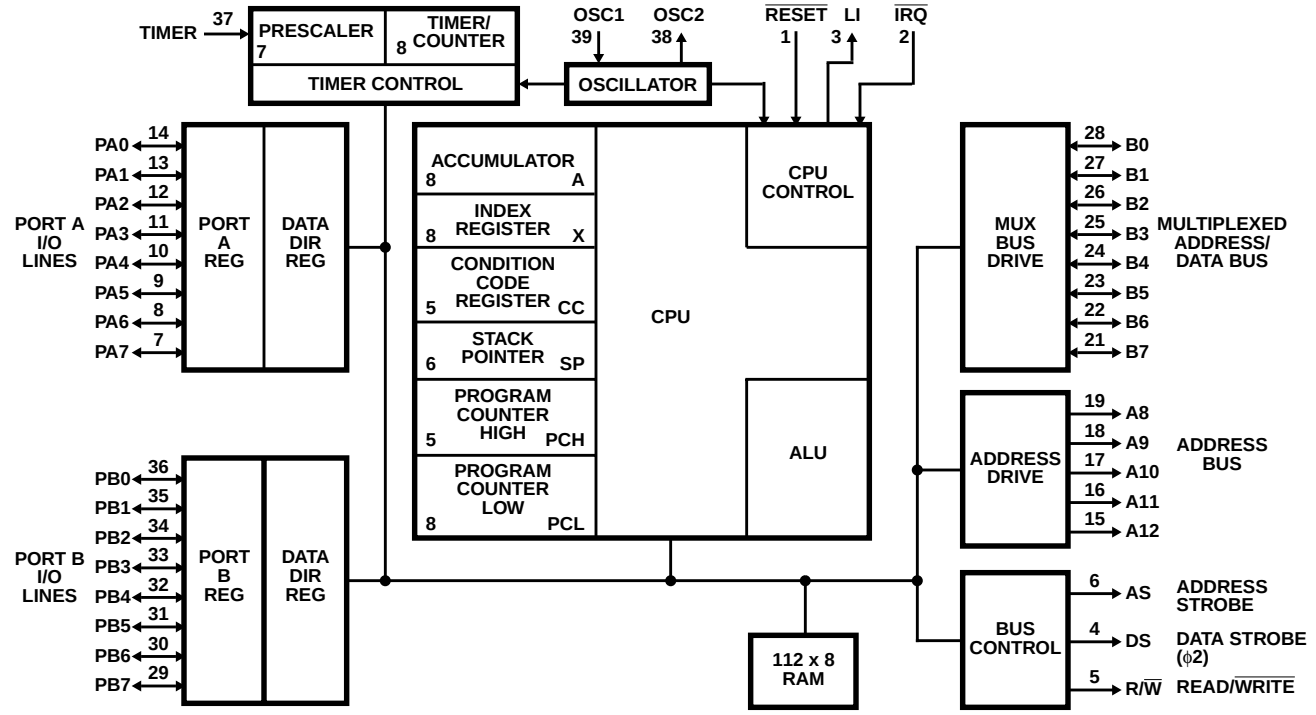


FIGURE 1A. CDP6805E2 BLOCK DIAGRAM

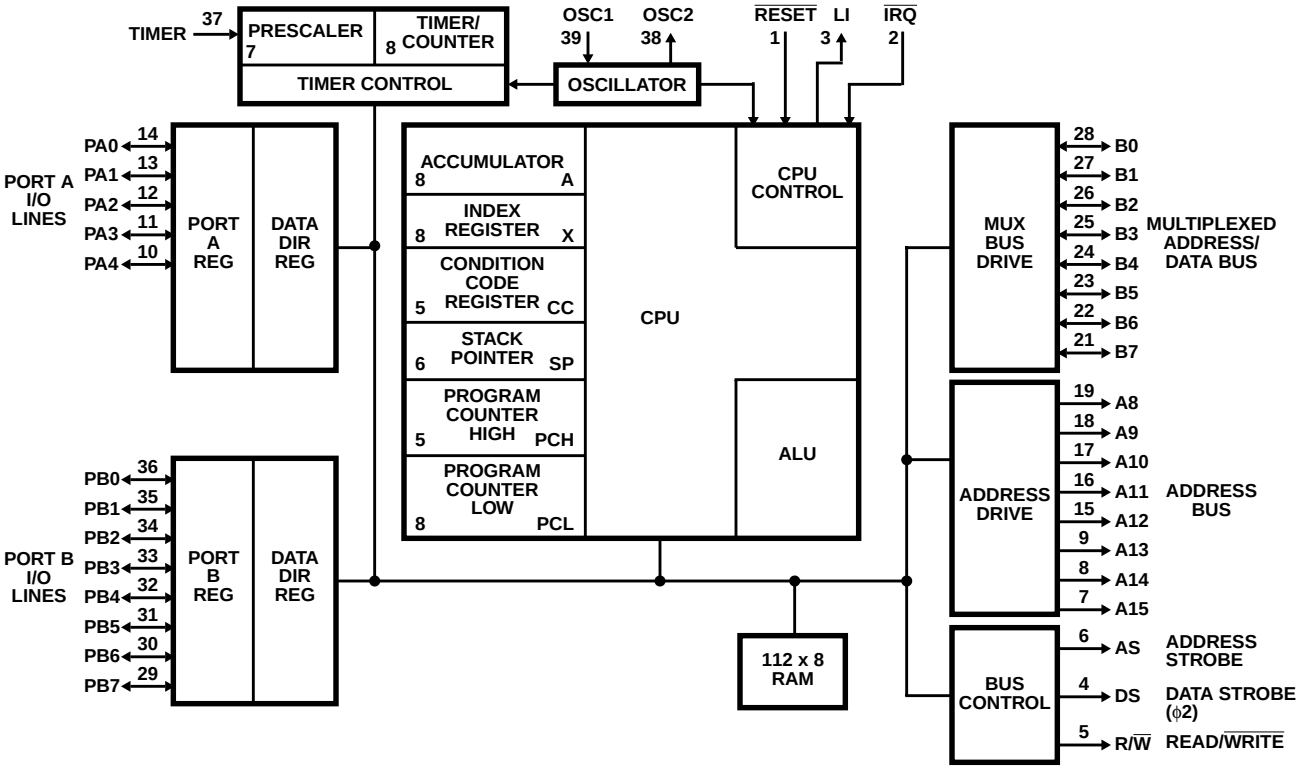


FIGURE 1B. CDP6805E3 BLOCK DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) . . . . . -0.3V to +8V
Voltage Referenced to V_{SS} Terminal)
All Voltage Input Voltages Except OSC1 (V_{IN}). Vss-0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . .±10mA

Operating Conditions

Temperature Range (T_A) . . . . . -40°C to 85°C

CDP6805E2,CDP6805E2E,
CDP6805E3, CDP6805E3E . . . . . .0°C to 70°C
CDP6805E2C, CDP6805E2CE,
CDP6805E3C, CDP6805E3CE . . . . . -40°C to 85°C
T_A = Full Package Temperature Range (All Package Types)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PDIP Package 50
PLCC Package 50
Device Dissipation Per Output Transistor 100mW
Maximum Storage Temperature Range (T_{STG}) . . . .-55°C to 150°C
Maximum Lead Temperature (During Soldering) . . . . . 265°C
At Distance 1/16 ±1/32 in. (1.59 ± 0.79mm)
From Case for 10s Max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications 3.0V (V_{DD} = 3VDC, V_{SS} = 0, T_A = T_L to T_H), Unless Otherwise Specified

PARAMETER	SYMBOL	MIN	MAX	UNIT
Output Voltage $I_{LOAD} \leq 10\mu A$	V_{OL}	-	0.1	V
	V_{OH}	V_{DD} - 0.1	-	V
Total Supply Current (C_L = 50pF - no DC loads) t_{CYC} = 5µs				
Run (V_{IL} = 0.2V, V_{IH} = V_{DD} -0.2V)	I_{DD}	-	1.3	mA
Wait (Note 2)	I_{DD}	-	200	µA
Stop (Note 2)	I_{DD}	-	100	µA
Output High Voltage				
(I_{LOAD} = 0.25mA) A8-A15, B0-B7	V_{OH}	2.7	-	V
(I_{LOAD} = 0.1mA) PA0-PA7, PB0-PB7	V_{OH}	2.7	-	V
(I_{LOAD} = 0.25mA) DS, AS, R/$\overline{W}$	V_{OH}	2.7	-	V
Output Low Voltage				
(I_{LOAD} = 0.25mA) A8-A15, B0-B7	V_{OL}	-	0.3	V
(I_{LOAD} = 0.25mA) PA0-PA7, PB0-PB7	V_{OL}	-	0.3	V
(I_{LOAD} = 0.25mA) DS, AS, R/$\overline{W}$	V_{OL}	-	0.3	V
Input High Voltage				
PA0-PA7, PB0-PB7, B0-B7	V_{IH}	2.1	-	V
Timer, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	2.5	-	V
OSC1	V_{IH}	2.1	-	V
Input Low Voltage (All inputs)	V_{IL}	-	0.5	V
Frequency of Operation				
Crystal	f_{OSC}	0.032	1.0	MHz
External Clock	f_{OSC}	DC	1.0	MHz
Input Current				
$\overline{RESET}$, $\overline{IRQ}$, Timer, OSC1	I_{IN}	-	±1	µA

DC Electrical Specifications 3.0V (V_{DD} = 3VDC, V_{SS} = 0, $T_A = T_L$ to T_H), Unless Otherwise Specified

PARAMETER	SYMBOL	MIN	MAX	UNIT
Three-State Output Leakage PA0-PA7, PB0-PB7, B0-B7	I_{TSL}	-	±10	µA
Capacitance $\overline{RESET}$, $\overline{IRQ}$, Timer	C_{IN}	-	8.0	pF
DS, AS, R/$\overline{W}$, A8-A15, PA0-PA7, PB0-PB7, B0-B7	C_{OUT}	-	12.0	pF

NOTES:

2. Test conditions are Quiescent Current Values are:
   Port A and B programmed as inputs.
   V_{IL} = 0.2V for PA0-PA7, PB0-PB7, and B0-B7.
   $V_{IH} = V_{DD}$ - 0.2V for $\overline{RESET}$, $\overline{IRQ}$, and Timer.
   OSC1 input is a square wave from V_{SS} +0.2V to V_{DD} - 0.2V.
   OSC2 output load (including tester) is 35pF maximum.
   Wait Mode I_{DD} is affected linearly by this capacitance.
3. References to PA5-7 pertain to CDP6805E2 and references to A13-15 pertain to CDP6805E3.

DC Electrical Specifications 5.0 (V_{DD} = 5VDC ±10%, V_{SS} = 0, $T_A = T_L$ to T_H), Unless Otherwise Specified

PARAMETER	SYMBOL	MIN	MAX	UNIT
Output Voltage $I_{LOAD} \leq 10\mu A$	V_{OL}	-	0.1	V
	V_{OH}	V_{DD} - 0.1	-	V
Total Supply Current (C_L = 130pF - On Bus, C_L = 50pF - On Ports, No DC Loads, t_{CYC} = 1µs Run (V_{IL} = 0.2V, $V_{IH} = V_{DD}$ - 0.2V)	I_{DD}	-	10	mA
Wait (Note 4)	I_{DD}	-	1.5	mA
Stop (Note 4)	I_{DD}	-	200	µA
Output High Voltage (I_{LOAD} = 1.6mA) A8-A15, B0-B7	V_{OH}	4.1	-	V
(I_{LOAD} = 0.36mA) PA0-PA7, PB0-PB7	V_{OH}	4.1	-	V
(I_{LOAD} = 1.6mA) DS, AS, R/$\overline{W}$	V_{OH}	4.1	-	V
Output Low Voltage (I_{LOAD} = 1.6mA) A8-A15, B0-B7	V_{OL}	-	0.4	V
(I_{LOAD} = 1.6mA) PA0-PA7, PB0-PB7	V_{OL}	-	0.4	V
(I_{LOAD} =1.6mA) DS, AS, R/$\overline{W}$	V_{OL}	-	0.4	V
Input High Voltage PA0-PA7, PB0-PB7, B0-B7	V_{IH}	V_{DD} - 2.0	-	V
Timer, $\overline{IRQ}$, $\overline{RESET}$	V_{IH}	V_{DD} - 0.8	-	V
OSC1	V_{IH}	V_{DD} - 1.5	-	V
Input Low Voltage (All Inputs)	V_{IL}	-	0.8	V
Frequency of Operation Crystal	f_{OSC}	0.032	5.0	MHz
External Clock	f_{OSC}	DC	5.0	MHz
Input Current $\overline{RESET}$, $\overline{IRQ}$, Timer, OSC1	I_{IN}	-	±1	µA

DC Electrical Specifications 5.0 (V_{DD} = 5VDC ±10%, V_{SS} = 0, T_A = T_L to T_H), Unless Otherwise Specified

PARAMETER	SYMBOL	MIN	MAX	UNIT
Three-State Output Leakage PA0-PA7, PB0-PB7, B0-B7	I_{TSI}	-	±10	µA
Capacitance $\overline{RESET}$, $\overline{IRQ}$, Timer	C_{IN}	-	8.0	pF
Capacitance DS, AS, R/$\overline{W}$, A8-15, PA0-PA7, PB0-PB7, B0-B7	C_{OUT}	-	12.0	pF

NOTES:

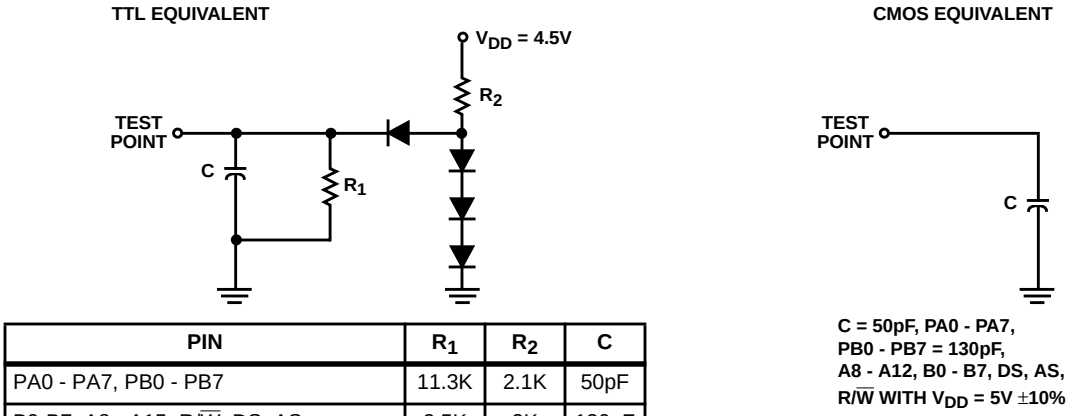
4. Test conditions are Quiescent Current Values are:
   Port A and B programmed as inputs.
   V_{IL} = 0.2V to PA0 - PA7, PB0-PB7, and B0-B7.
   V_{IH} = V_{DD} - 0.2V for $\overline{RESET}$, $\overline{IRQ}$, and Timer.
   OSC1 input is a squarewave from V_{SS} + 0.2V to V_{DD} - 0.2V.
   OSC2 output load (including tester) is 35pF maximum.
   Wait mode (I_{DD}) is affected linearly by this capacitance.
5. References to PA5-7 pertain to CDP6805E2 and references to A13-15 pertain to CDP6805E3.

TABLE 1. CONTROL TIMING (V_{SS} = 0, T_A = T_L to T_H)

PARAMETER	SYMBOL	V_{DD} = 3V f_{OSC} = 1MHz			V_{DD} = 5V ± 10% f_{OSC} = 5MHz			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
I/O Port Timing - Input Setup Time (Figure 3)	t_{PVASL}	500	-	-	250	-	-	ns
Input Hold Time (Figure 3)	t_{ASLPX}	100	-	-	100	-	-	ns
Output Delay Time (Figure 3)	t_{ASLPV}	-	-	0	-	-	0	ns
Interrupt Setup Time (Figure 6)	t_{ILASL}	2	-	-	0.4	-	-	µS
Crystal Oscillator Start-up Time (Figure 5)	t_{OXOV}	-	30	300	-	15	100	mS
Wait Recovery Start-up Time (Figure 7)	t_{IVASH}	-	-	10	-	-	2	µS
Stop Recovery Start-up Time (Crystal Oscillator) (Figure 8)	t_{ILASH}	-	30	300	-	15	100	mS
Required Interrupt Release (Figure 7)	t_{DSLIH}	-	-	5	-	-	1.0	µs
Timer Pulse Width (Figure 7)	t_{TH}, t_{TL}	0.5	-	-	0.5	-	-	t_{CYC}
Reset Pulse Width (Figure 5)	t_{RL}	5.2	-	-	1.05	-	-	µS
Timer Period (Figure 7)	t_{TLTL}	1.0	-	-	1.0	-	-	t_{CYC}
Interrupt Pulse Width Low (Figure 16)	t_{ILIH}	1.0	-	-	1.0	-	-	t_{CYC}
Interrupt Pulse Period (Figure 16)	t_{ILIL}	(Note 2)	-	-	(Note 2)	-	-	t_{CYC}
Oscillator Cycle Period (1/5 of t_{CYC})	t_{OLOL}	1000	-	-	200	-	-	ms
OSC1 Pulse Width High	t_{OH}	350	-	-	75	-	-	ns
OSC1 Pulse Width Low	t_{OL}	350	-	-	75	-	-	ns

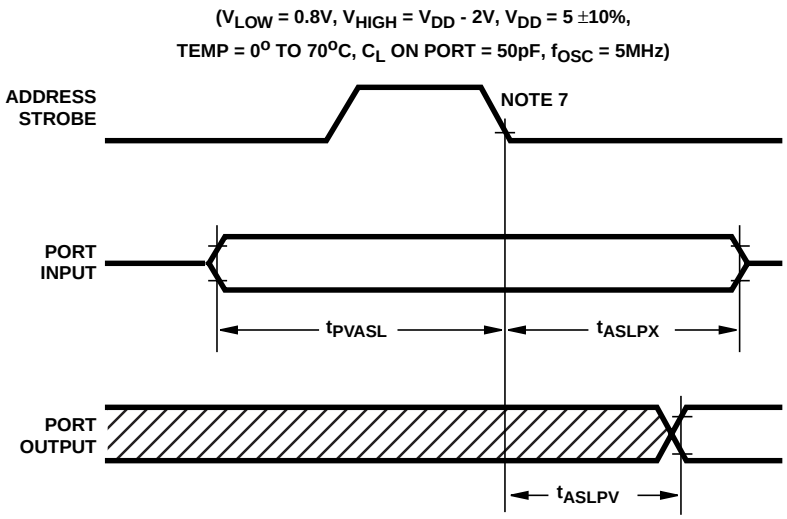
NOTE:

6. The minimum period of t_{ILIL} should not be less than the number of t_{CYC} cycles it takes to execute the interrupt service routine plus 20 t_{CYC} cycles.



PIN	R_1	R_2	C
PA0 - PA7, PB0 - PB7	11.3K	2.1K	50pF
B0-B7, A8 - A15, R/$\overline{W}$, DS, AS	2.5K	2K	130pF

FIGURE 2. EQUIVALENT TEST-LOAD CIRCUITS



NOTE:

7. The address strobe of the first cycle of the next instruction as shown in Table 1.

FIGURE 3. I/O PORT TIMING WAVEFORMS

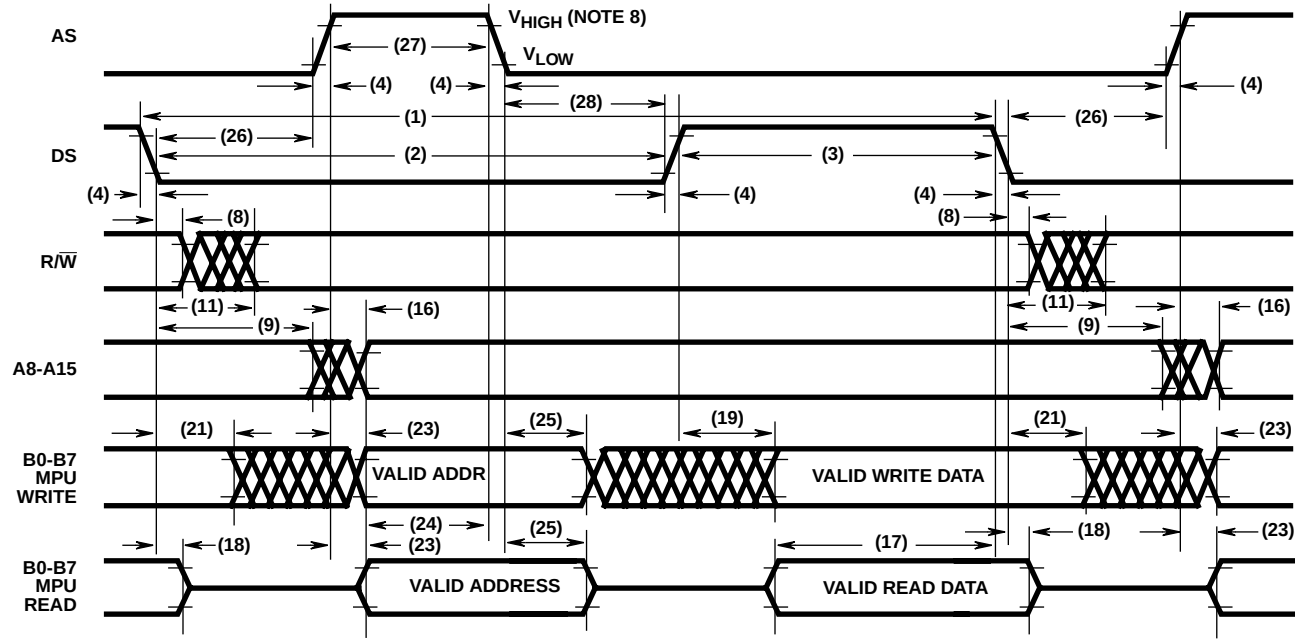
TABLE 2. BUS TIMING (T_A = T_L TO T_H, V_{SS} = 0 V) See Figure 4

NUM	PARAMETERS	SYMBOL	f_{OSC} = 1MHz, V_{DD} = 3V 50pF Load		f_{OSC} = 5MHz V_{DD} = 5V ±10%, 1 TTL AND 130PF LOAD		UNITS
			MIN	MAX	MIN	MAX	
1	Cycle Time	t_{CYC}	5000	DC	1000	DC	ns
2	Pulse Width, DS Low	PW_{EL}	2800	-	560	-	ns
3	Pulse Width, DS High or $\overline{RD}$, $\overline{WR}$, Low	PW_{EH}	1800	-	375	-	ns
4	Clock Transition	t_r, t_f	-	100	-	30	ns
8	R/$\overline{W}$ Hold	t_{RWH}	10	-	10	-	ns

TABLE 2. BUS TIMING ($T_A = T_L$ TO T_H, V_{SS} = 0 V) See Figure 4 **(Continued)**

NUM	PARAMETERS	SYMBOL	f_{OSC} = 1MHz, V_{DD} = 3V 50pF Load		f_{OSC} = 5MHz V_{DD} = 5V ±10%, 1 TTL AND 130PF LOAD		UNITS
			MIN	MAX	MIN	MAX	
9	Non-Muxed Address Hold	t_{AH}	800	-	100	-	ns
11	R/$\overline{W}$ Delay from DS Fall	t_{AD}	-	500	-	300	ns
16	Non-Muxed Address Delay from AS Rise	t_{ADH}	0	200	0	100	ns
17	MPU Read Data Setup	t_{DSR}	200	-	115	-	ns
18	Read Data Hold	t_{DHR}	0	1000	0	160	ns
19	MPU Data Delay, Write	t_{DDW}	-	0	-	120	ns
21	Write Data Hold	t_{DHW}	800	-	55	-	ns
23	Muxed Address Delay from AS Rise	t_{BHD}	0	250	0	120	ns
24	Muxed Address Valid to AS Fall	t_{ASL}	600	-	55	-	ns
25	Muxed Address Hold	t_{AHL}	250	750	60	180	ns
26	Delay DS Fall to AS Rise	t_{ASD}	800	-	160	-	ns
27	Pulse Width, AS High	PW_{ASH}	850	-	175	-	ns
28	Delay, AS Fall to DS Rise	t_{ASED}	800	-	160	-	ns

Waveforms

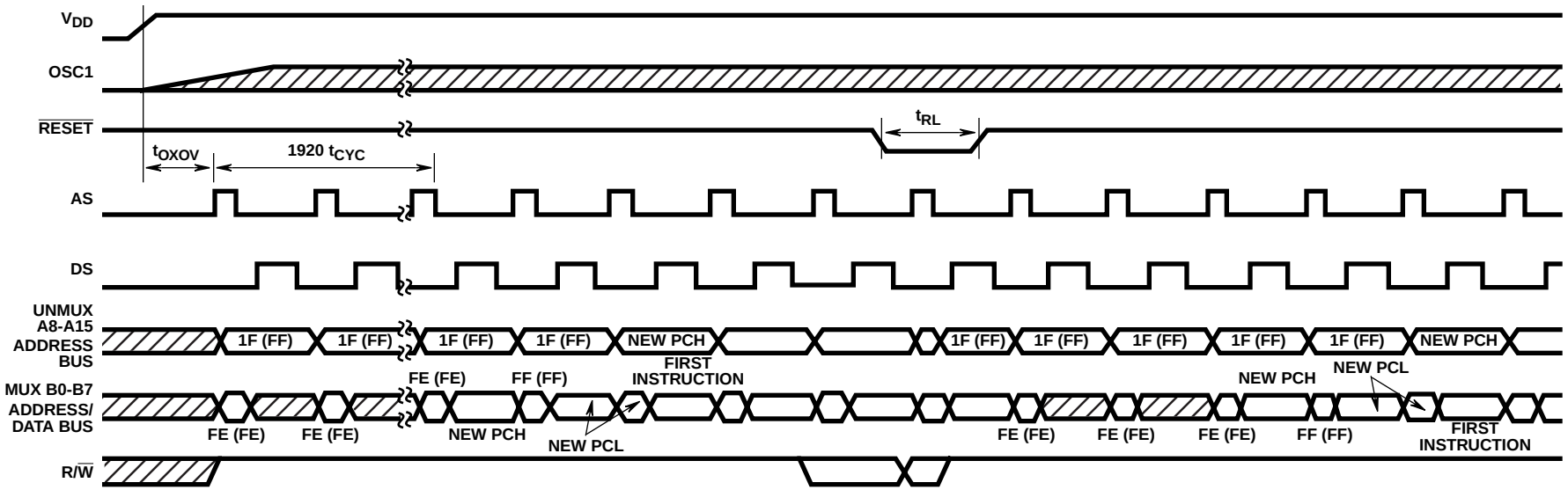


NOTE:

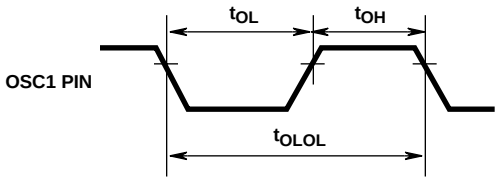
8. $V_{HIGH} = V_{DD}$ -0.2V, V_{LOW} = 0.5V for V_{DD} = 3V
   $V_{HIGH} = V_{DD}$ -2V, V_{LOW} = 0.8V for V_{DD} = 5V ±10%

FIGURE 4. BUS TIMING WAVEFORMS

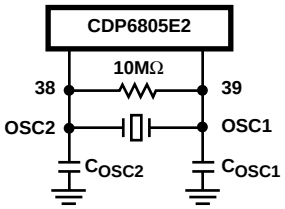
Waveforms (Continued)



OSCILLATOR WAVEFORM



CRYSTAL OSCILLATOR CONNECTIONS



CRYSTAL PARAMETERS REPRESENTATIVE FREQUENCY

	5MHz	4MHz	1MHz
RS Max	50Ω	75Ω	400Ω
C0	8pF	7pF	5pF
C1	0.02pF	0.012pF	0.008pF
Q	50k	40k	30k
C_{OSC1}	15-30pF	15-30pF	15-40pF
C_{OSC2}	15-25pF	15-25pF	15-30pF

CRYSTAL CIRCUIT

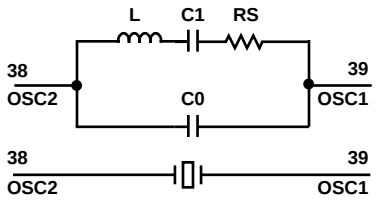
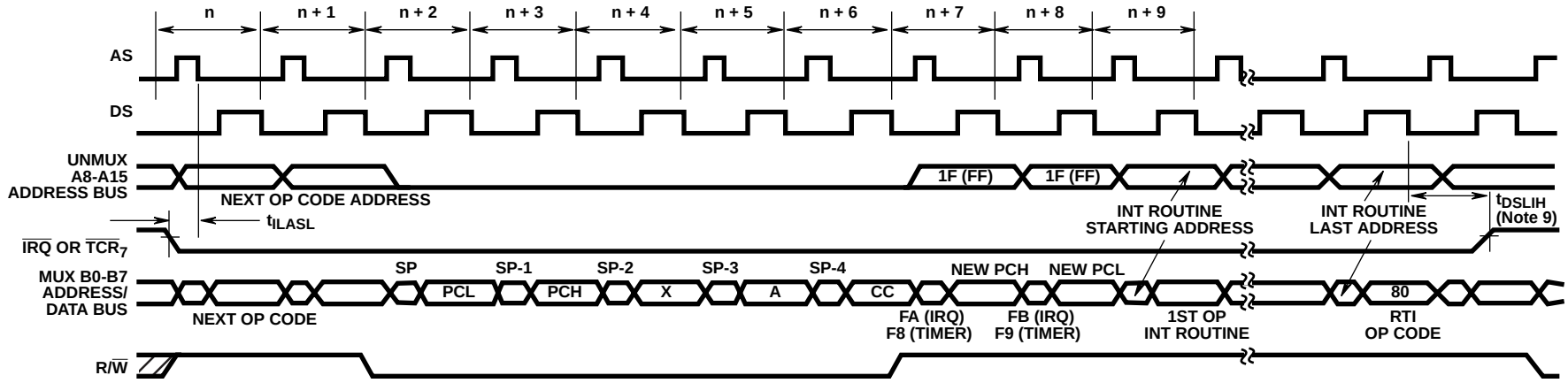


FIGURE 5. POWER-ON RESET AND RESET TIMING WAVEFORMS

Waveforms (Continued)



NOTE:

9. t_{DSLIH} - The interrupting device must release the $\overline{IRQ}$ line within this time to prevent subsequent recognition of the same interrupt.

FIGURE 6. $\overline{IRQ}$ AND $\overline{TCR}_7$ INTERRUPT TIMING WAVEFORMS

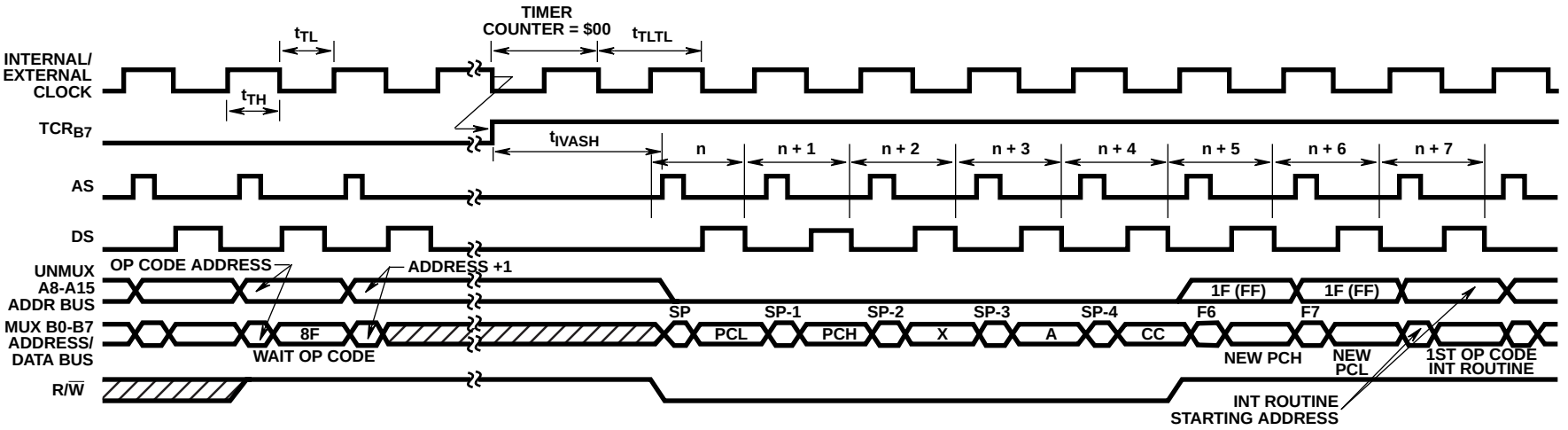
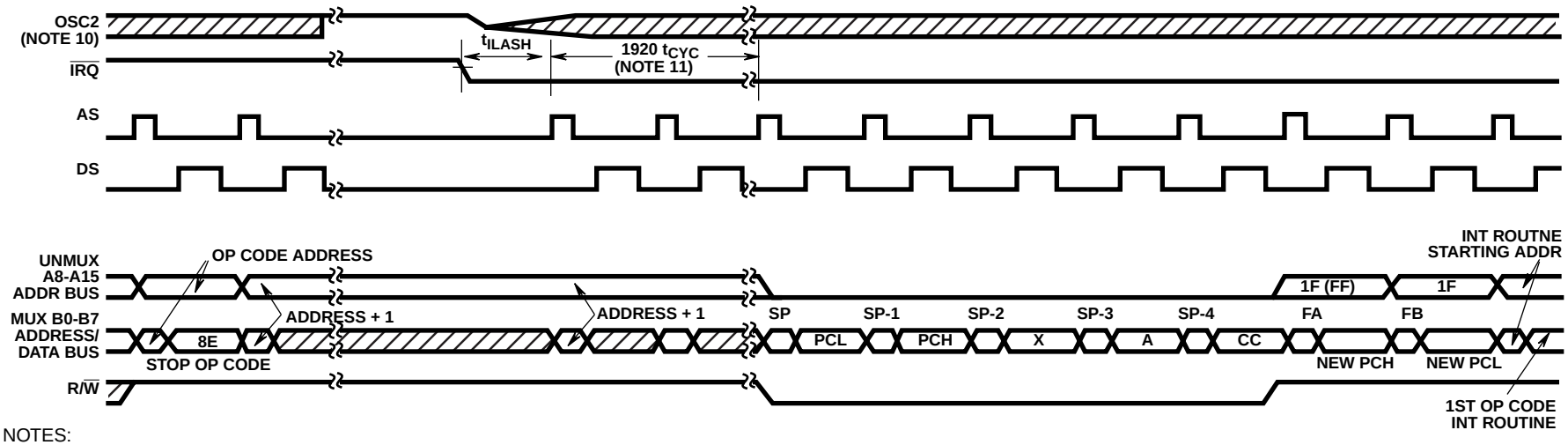


FIGURE 7. TIMER INTERRUPT AFTER WAIT INSTRUCTION TIMING WAVEFORMS

Waveforms (Continued)



NOTES:

10. Represents the internal gating of the OSC1 input pin.

11. t_{CYC} is on instruction cycle (for f_{OSC} = 5MHz, t_{CYC} = 1µs)

FIGURE 8. INTERRUPT RECOVERY FROM STOP INSTRUCTION TIMING WAVEFORMS

Functional Pin Description

V_{DD} and V_{SS} - V_{DD} and V_{SS} provide power to the chip. V_{DD} provides power and V_{SS} is ground.

$\overline{IRQ}$ (Maskable Interrupt Request) - $\overline{IRQ}$ is a level sensitive and edge sensitive input which can be used to request an interrupt sequence. The MPU completes the current instruction before it responds to the request. If $\overline{IRQ}$ is low and the interrupt mask bit (I-bit) in the Condition Code Register is clear, the MPU begins an interrupt sequence at the end of the current instruction. The interrupt circuit recognizes both a “Wire ORed” level as well as pulses on the $\overline{IRQ}$ line (see Interrupt Section for more details). $\overline{IRQ}$ requires an external resistor to V_{DD} for “Wire OR” operation.

$\overline{RESET}$ - The $\overline{RESET}$ input is not required for start up but can be used to reset the MPU’s internal state and provide an orderly software start up procedure. Refer to the RESET section for a detailed description.

TIMER - The TIMER input is used for clocking the on chip timer. Refer to TIMER section for a detailed description.

AS (Address Strobe) - Address Strobe (AS) is an output strobe used to indicate the presence of an address on the 8-bit multiplexed bus. The AS line is used o demultiplex the eight least significant address bits from the data bus. A latch controlled by Address Strobe should capture address on the negative edge. This output is capable of driving one standard TTL load and 130pF and is available at $f_{OSC} \div 5$ when the MPU is not in the WAIT or STOP states.

DS (Data Strobe) - This output is used to transfer data to or from a peripheral or memory. DS occurs anytime the MPU does a data read or write. DS also occurs when the MPU does a data transfer to or from the MPU’s internal memory. Refer to Table 2 and Figure 4 for timing characteristics. This output is capable of driving one standard TTL load and 130pF. DS is a continuous signal at $f_{OSC} \div 5$ when the MPU is not in WAIT or STOP state. Some bus cycles are redundant reads of op code bytes.

R/$\overline{W}$ (Read/Write) - The R/$\overline{W}$ output is used to indicate the direction of data transfer for both internal memory and I/O registers, and external peripheral devices and memories. This output is used to indicate to a selected peripheral whether the MPU is going to read or write data on the next Data Strobe (R/$\overline{W}$ low = processor write; R/$\overline{W}$ high = processor read). The R/$\overline{W}$ output is capable of driving one standard TTL load and 130pF. The normal standby state is Read (high).

A8-A15 (High Order Address Lines) - The A8-A15 output lines constitute the higher order non-multiplexed addresses. Each output line is capable of driving one standard TTL load and 130pF.

B0-B7 (Address/Data Bus) - The B0-B7 bidirectional lines constitute the lower order addresses and data. These lines are multiplexed, with address present at Address Strobe time and data present at Data Strobe time. When in the data mode, these lines are bidirectional, transferring data to and from memory and peripheral devices as indicated by the R/$\overline{W}$ pin. As outputs in either the data or address modes, these lines are capable of driving one standard TTL load and 130pF.

OSC1, OSC2 - The CDP6805E2/3 provides for two types of oscillator inputs - crystal circuit or external clock. The two oscillator pins are used to interface to a crystal circuit, as shown in Figure 5. If an external clock is used, it must be connected to OSC1. The input at these pins is divided by five to form the cycle rate seen on the AS and DS pins. The frequency range is specified by f_{OSC}. The OSC1 to bus transitions relationships are provided in Figure 9 for system designs using oscillators slower than 5MHz.

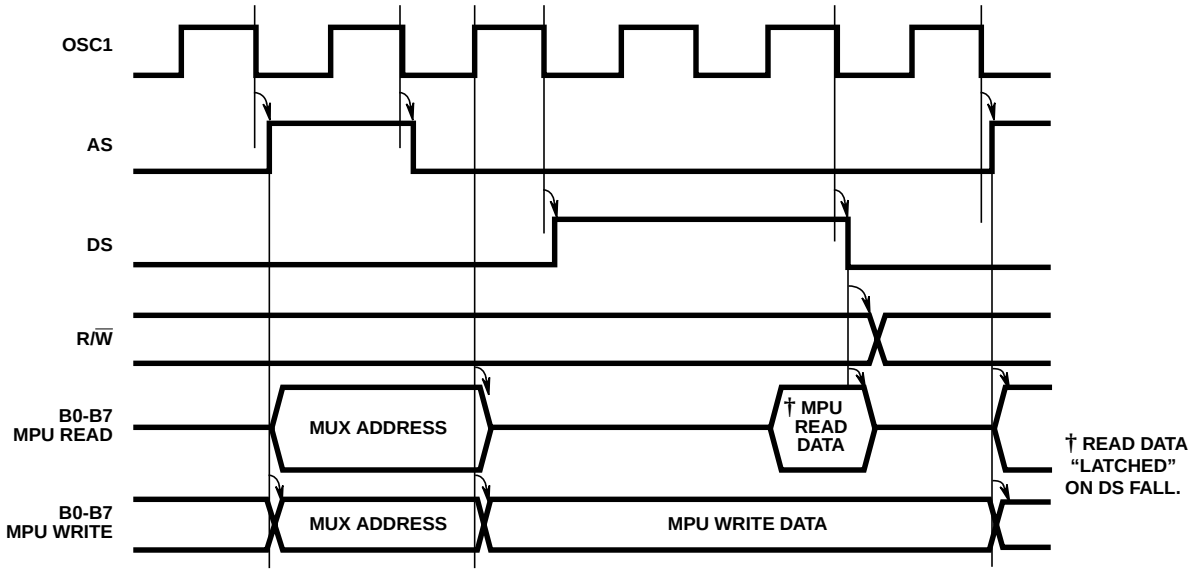


FIGURE 9. OSC1 TO BUS TRANSISTIONS TIMING WAVEFORMS

Crystal - The circuit shown in Figure 5 is recommended when using a crystal. The internal oscillator is designed to interface with an AT-cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in the electrical characteristics table. An external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time.

External Clock - An external clock should be applied to the OSC1 input with the OSC2 input not connected, as shown in Figure 10.

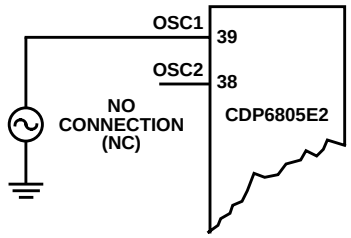


FIGURE 10. EXTERNAL CLOCK CONNECTION

LI (Load Instruction) - This output is used to indicate that a fetch of the next opcode is in progress. LI remains low during an External or Timer interrupt. The LI output is only used for certain debugging and test systems. For normal operations this pin is not connected. The LI output is capable of driving one standard TTL load and 50pF. This signal overlaps Data Strobe.

PA0-PA7 - These eight pins constitute Input/Output Port A. Each line is individually programmed to be either an input or output under software control via its Data Direction Register as shown below. An I/O pin is programmed as an output when the corresponding DDR bit is set to a “1”, and as an input when it is set to a “0”. In the output mode the bits are latched and appear on the corresponding output pins. An MPU read of the port bits programmed as outputs reflect the last value written to that location. When programmed as an input, the input data bit(s) are not latched. An MPU read of the port bits programmed as inputs reflects the current status of the corresponding input pins. The Read/Write port timing is shown in Figure 3. See typical I/O Port Circuitry in Figure 11. During a Power-On Reset or external $\overline{\text{RESET}}$ all lines are configured as inputs (zero in Data Direction Register). The output port register is not initialized by reset. The TTL compatible three-state output buffers are capable of driving one standard TTL load and 50pF. The DDR is a read/write register.

PB0-PB7 - These eight pins interface to Input/Output Port B. Refer to PA0-PA7 description for details of operation.

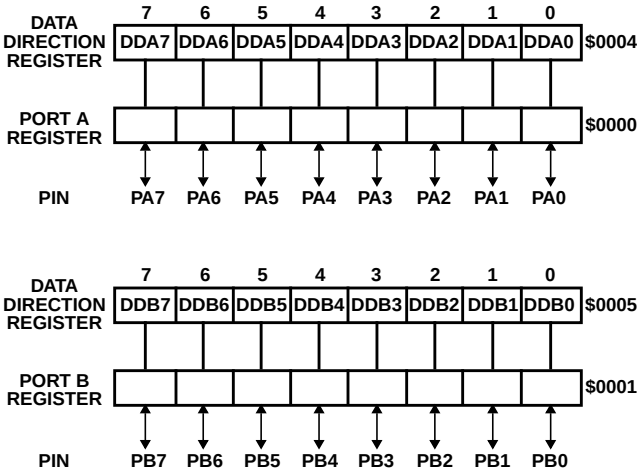


TABLE 3. I/O PIN FUNCTIONS

R/$\overline{W}$	DDR	I/O PIN FUNCTIONS
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

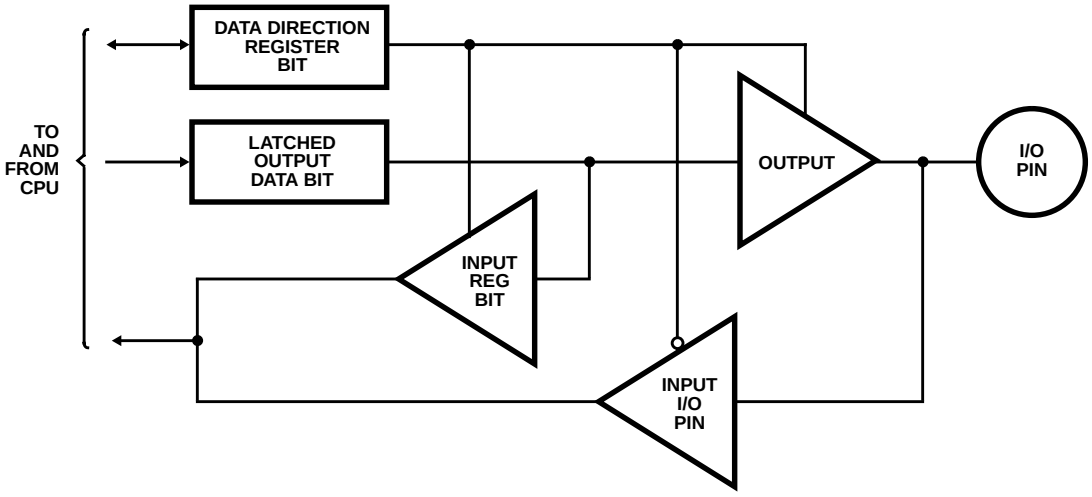


FIGURE 11. TYPICAL I/O PORT CIRCUITRY

Functional Description

Throughout the following sections references to CDP6805E2 imply both the CDP6805E2 and the CDP6805E3. Values in parenthesis refer to the CDP6805E3.

Memory Addressing

The CDP6805E2 is capable of addressing 8192 (65,536) bytes of memory and I/O registers. The address space is divided into internal memory space and external memory space, as shown in Figure 12.

The internal memory space is located within the first 128 bytes of memory (first half of page zero) and is comprised of the I/O port locations, timer locations, and 112 bytes of RAM. The MPU can read from or write to any of these locations. A program write to on chip locations is repeated on the external bus to permit off chip memory to duplicate the content of on chip memory. Program reads to on chip locations also appear on the external bus, but the MPU accepts data only from the addressed on chip location. Any read data appearing on the input bus is ignored.

The stack pointer is used to address data stored on the stack. Data is stored on the stack during interrupts and subroutine calls. At power up, the stack pointer is set to $7F and it is decremented as data is pushed onto the stack. When data is removed from the stack, the stack pointer is incriminated. A maximum of 64 bytes of RAM is available for stack usage. Since most programs use only a small part of the allotted stack locations for interrupts and/or subroutine stacking purposes, the unused bytes are usable for program data storage.

All memory locations above location $007F are part of the external memory map. In addition, ten locations in the I/O portion of the lower 128 bytes of memory space, as shown in Figure 12, are part of the external memory map. All of the external memory space is user definable except the highest 10 locations. Locations $1FF6 to $1FFF ($FFF6 to $FFFF) of the external address space are reserved for interrupt and reset vectors (see Figure 12).

Registers

The CDP6805E2 contains five registers as shown in the programming model in Figure 13. The interrupt stacking order is shown in Figure 14.

Accumulator (A) - This Accumulator is an 8-bit general purpose register used for arithmetic calculations and data manipulations.

Index Register (X) - The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit operand which is used to create an effective address. The index register is also used for data manipulations with the Read/Modify/Write type of instructions and as a temporary storage register when not performing addressing operations.

Program Counter (PC) - The program counter is a 13-bit (16-bit) register that contains the address of the next instruction to be executed by the processor.

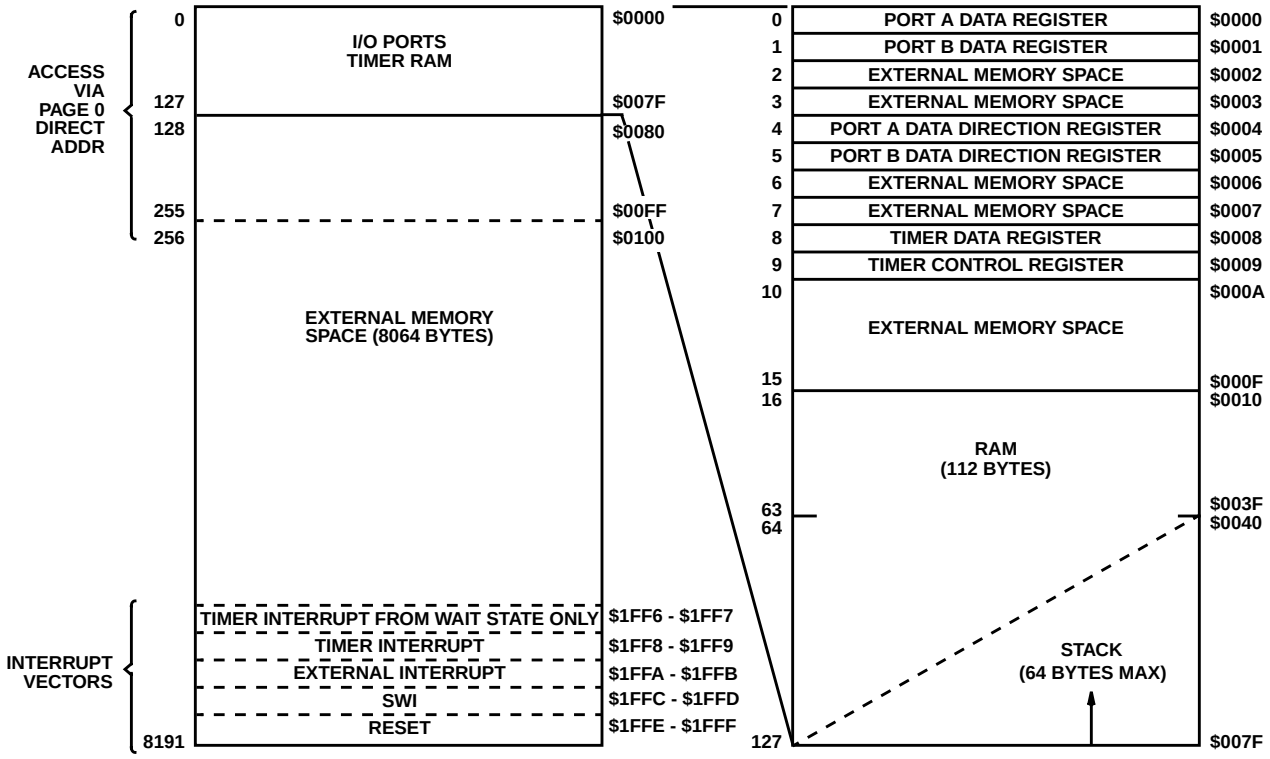


FIGURE 12A. CDP6805E2 ADDRESS MAP

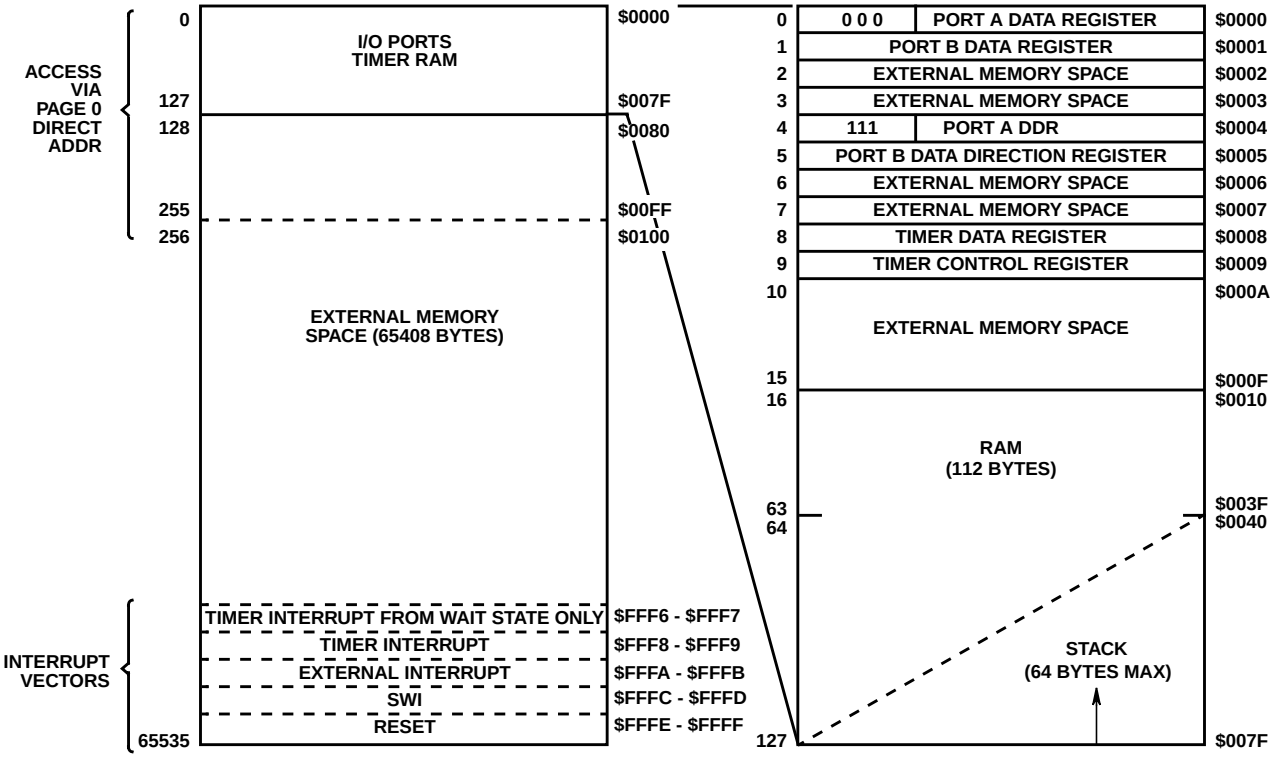


FIGURE 12B. CDP6805E3 ADDRESS MAP

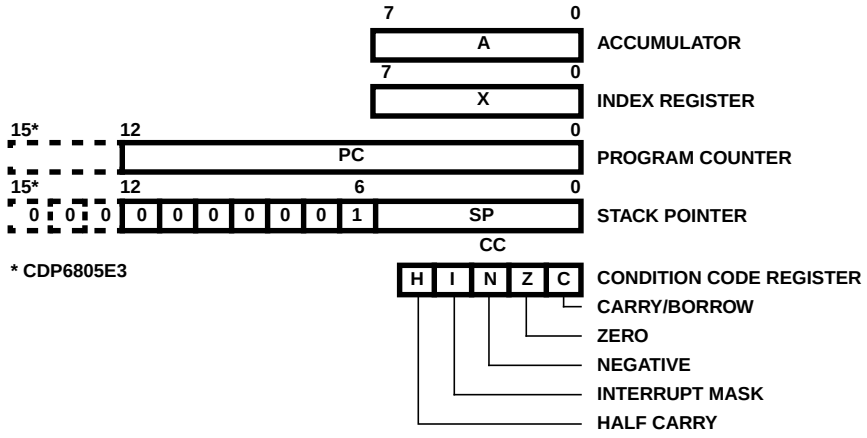
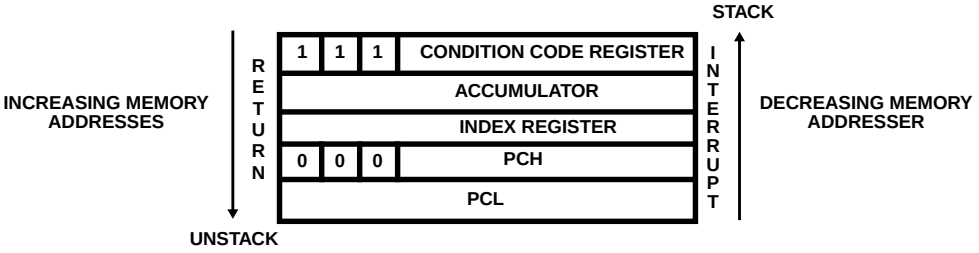


FIGURE 13. PROGRAMMING MODEL



NOTE: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

FIGURE 14. STACKING ORDER

Stack Pointer (SP) - The stack pointer is 13-bit (16-bit) register containing the address of the next free location on the stack. When accessing memory, the seven most significant bits are permanently set to 0000001 (0000000001). They are appended to the six least-significant register bits to produce an address within the range of $007F to $0040. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a “reset stack pointer” instruction, the stack pointer is set to its upper limit ($007F). Nested interrupts and/or subroutines may use up to 64 (decimal) locations, beyond which the stack pointer “wraps around” and points to its upper limit thereby losing the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five bytes.

Condition Code Register (CC) - The condition code register is a 5-bit register in which each bit is used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each of the five bits is explained below.

- **Half Carry Bit (H) -** The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H-bit is useful in Binary Coded Decimal addition subroutines.
- **Interrupt Mask Bit (I) -** When the I-bit is set, both the external interrupt and the timer interrupt are disabled. Clearing this bit enables the above interrupts. If an interrupt occurs while the I-bit is set, the interrupt is latched and will be processed when the I-bit is next cleared.
- **Negative Bit (N) -** When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logical one).
- **Zero Bit (Z) -** When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.
- **Carry Bit (C) -** The C-bit is set when a carry or a borrow out of the ALU occurs during an arithmetic instruction. The C-bit is also modified during bit test, shift, rotate, and branch types of instruction.

Resets

The CDP6805E2 has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a Power On Reset function; refer to Figure 5.

$\overline{\text{RESET}}$ (Pin #1) - The $\overline{\text{RESET}}$ input pin is used to reset the MPU and provide an orderly software start up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one t_{CYC}. The $\overline{\text{RESET}}$ pin is provided with a Schmitt Trigger to improve its noise immunity capability.

Power On Reset - The Power On Reset occurs when a positive transition is detected on V_{DD}. The Power On Reset is used strictly for power turn on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power down reset. The power on circuitry provides for a 1920 t_{CYC} delay from the time of the first oscillator operation. If the external reset pin is low at the end of the 1920 t_{CYC} time out, the processor remains in the reset condition.

Either of the two types of reset conditions causes the following to occur:

- Timer control register interrupt request bit (bit 7) is cleared to a “0”.
- Timer control register interrupt mask bit (bit 6) is set to a “1”.
- All data direction register bits are cleared to a “0” (inputs).
- Stack pointer is set to $007F
- The address bus is forced to the reset vector ($1FFE, $1FFF ($FFFE, $FFFF)
- Condition code register interrupt mask bit(1) is set to a “1”
- STOP and WAIT latches are reset.
- External interrupt latch is reset.

All other functions, such as other registers (including output ports) the timer, etc., are not cleared by the reset conditions.

Interrupts

The CDP6805E2 is capable of operation with three different interrupts, two hardware (timer interrupt and external interrupt) and one software (SWI). When any of these interrupts occur, normal processing is suspended at the end of the current instruction, execution. All of the program registers (the machine state) are pushed onto the stack; refer to Figure 14 for stacking order. The appropriate vector pointing to the starting address of the interrupt service routine is then fetched; refer to Figure 15 for the interrupt sequence.

The priority of the various interrupts from highest to lowest is as follows:

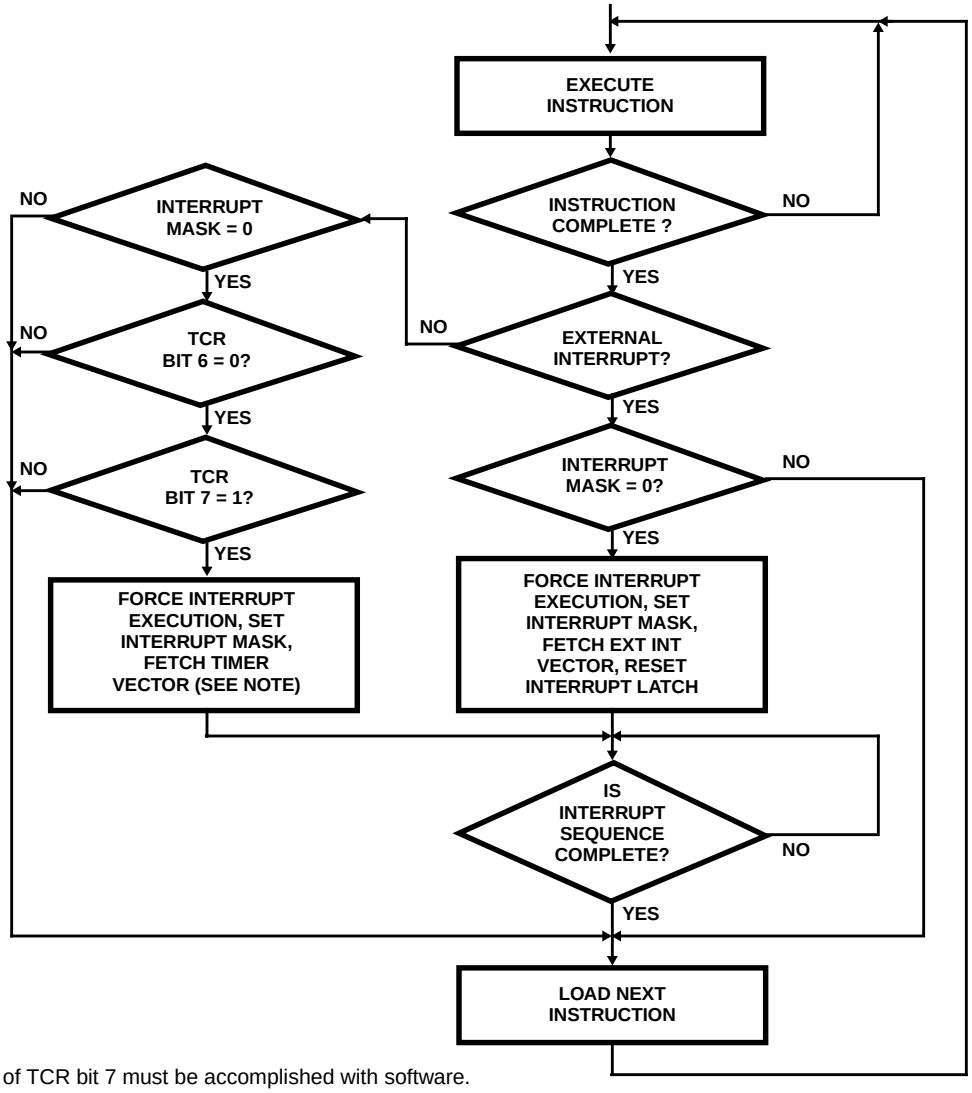
Timer Interrupt - If the timer mask bit (TCR6) is cleared, then each time the timer decrements to zero (transitions from $01 to $00) an interrupt request is generated. The actual processor interrupt is generated only if the interrupt mask bit of the condition code register is also cleared. When the interrupt is recognized, the current state of the machine is pushed onto the stack and the I-bit in the condition code register is set. This masks further interrupts until the present one is serviced. The processor now vectors to the timer interrupts service routine. The address for this service routine is specified by the contents of $1FF8 and $1FF9 ($FFF8 and $FFF9). The contents of $1FF6 and $1FF7 ($FFF6 and $FFF7) specify the service routine. Also, software must be used to clear the timer interrupt request bit (TCR7). At the end of the time interrupt service routine, the software normally executes an RTI instruction which restores the machine state and starts executing the interrupted program.

External Interrupt - If the interrupt mask bit of the condition code register is cleared and external interrupt pin $\overline{IRQ}$ is "low", then the external interrupt occurs. The action of the external interrupt is identical to the timer interrupt with the exception that the service routine address is specified by the contents of $1FFA and $1FFB ($FFFA and $FFFB). The interrupt logic recognizes both a "wire ORed" level and pulses on the external interrupt line. Figure 16 shows both a functional diagram and timing for the interrupt line. The timing diagram and timing for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{IRQ}$) to the processor. The first configuration shows many interrupt lines "wire ORed" to form the interrupts at the processor. Thus, if after servicing an interrupt the $\overline{IRQ}$ remains low, then the next interrupt is recognized. The second method is single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the length of the interrupt service routine. Once a pulse occurs, the next pulse should not occur until the MPU software has exited the routine (an RTI occurs). This time (t_{ILIL}) is obtained by adding 20 instruction cycles (one cycle $t_{CYC} = 5/f_{OSC}$) to the total number of cycles it takes to complete the service routine including the RTI instruction; refer to Figure 6.

Software Interrupt (SWI) - The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask in the condition code register. The service routine address is specified by the contents of memory locations $1FFC and $1FFD ($FFFC and $FFFD). See Figure 15 for interrupt and instruction Processing Flowchart.

The following three functions are not strictly interrupts; however, they are tied very closely to the interrupts. These functions are $\overline{RESET}$, STOP, WAIT.

$\overline{RESET}$ - The $\overline{RESET}$ input pin and the internal Power On Reset function each cause the program to vector to an initialization program. This vector is specified by the contents of memory locations $1FFE and $1FFF ($FFFE and $FFFF). The interrupt mask of the condition code register is also set. Refer to RESET section for details.



NOTE: The clear of TCR bit 7 must be accomplished with software.

FIGURE 15. INTERRUPT AND INSTRUCTION PROCESSING FLOWCHART

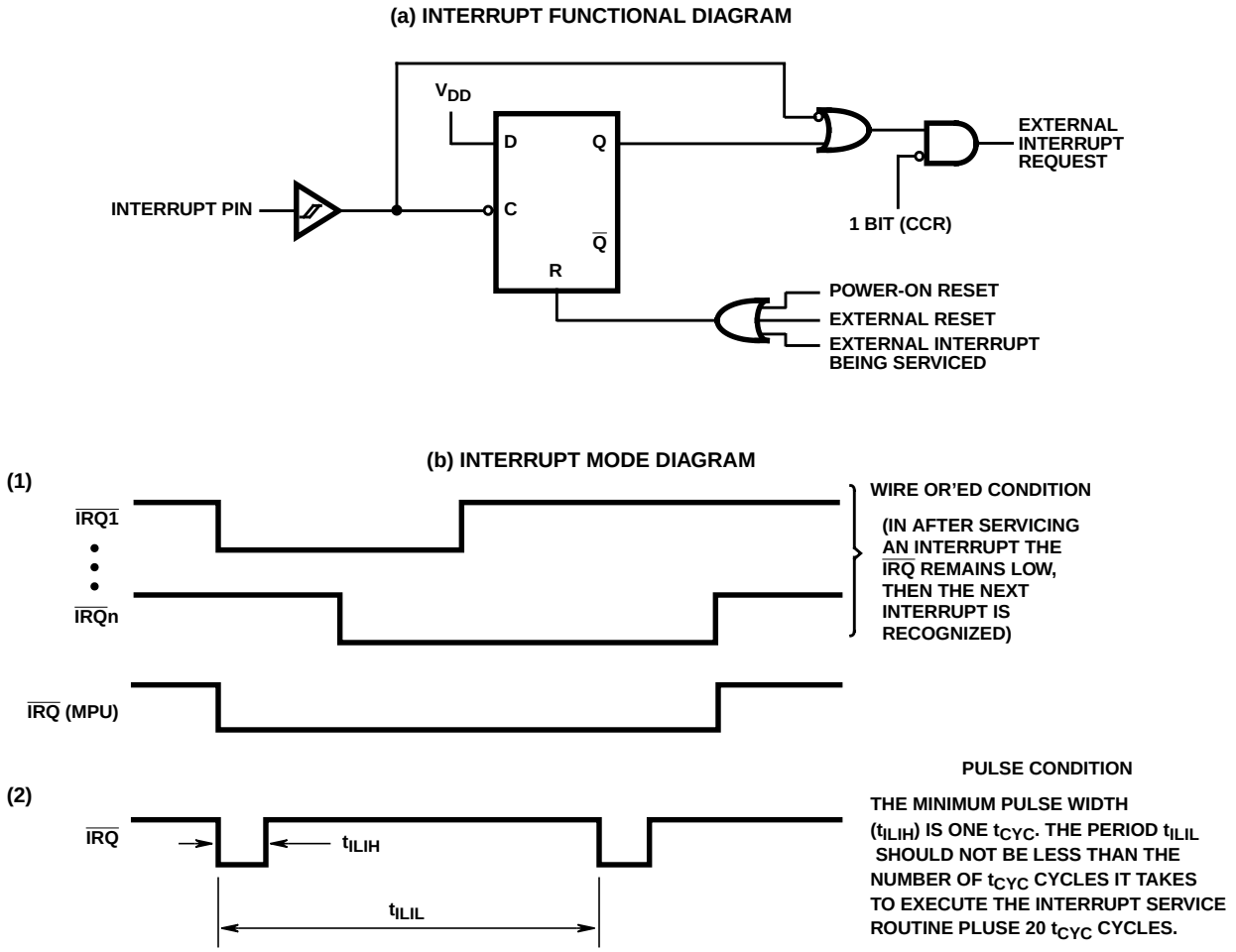


FIGURE 16. EXTERNAL INTERRUPT

STOP - The STOP instruction places the CDP6805E2 in a low power consumption mode. In the STOP function the internal oscillator is turned off, causing all internal processing and the timer to be halted; refer to Figure 17. The DS and AS lines go to a low state and the R/$\overline{W}$ line goes to a high state. The multiplexed address/data bus goes to the data input state. The high order address lines remain at the address of the next instruction. The MPU remains in the STOP mode until an external interrupt or reset occurs; refer to Figure 8 and 17.

During the STOP mode, timer control register (TCR) bits 6 and 7 are altered to remove any pending timer interrupt requests and to disable any further timer interrupts. External interrupts are enabled in the condition code register. All other registers and memory remain unaltered. All I/O lines remain unchanged.

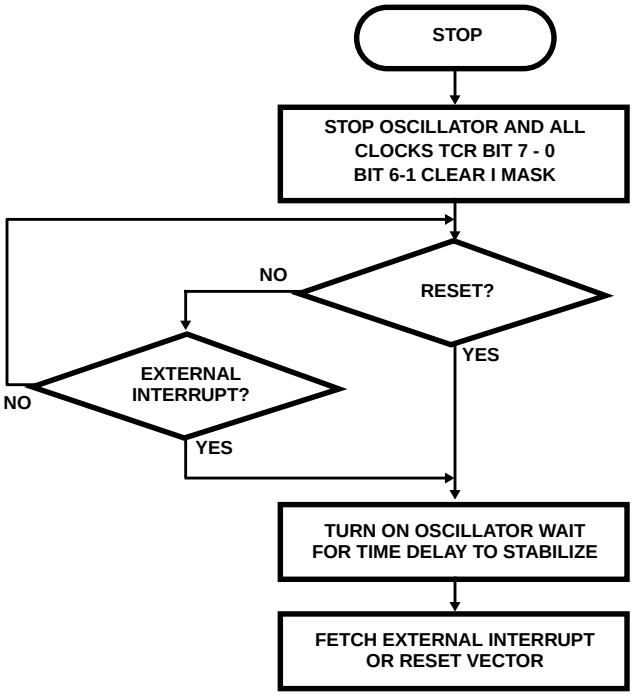


FIGURE 17. STOP FUNCTION FLOWCHART

WAIT - The WAIT instruction places the CDP6805E2 in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode; refer to Table 1. In the WAIT function, the internal clock is disabled from all internal circuitry except the Timer circuit, refer to Figure 18. Thus, all internal processing is halted except the Timer, which is allowed to count in a normal sequence. The R/$\overline{W}$ line goes to a high state, the multiplexed address/data bus goes to the data input state, and the DS and AS lines go to the low state. The high order address lines remain at the address of the next instruction. The MPU remains in this state until an external interrupt, timer interrupt, or a reset occurs; refer to Figures 7 and 18.

During the WAIT mode, the I-bit in the condition code register is cleared to enable interrupts. All other registers, memory, and I/O lines remain in their last state. The timer may be enabled to allow a periodic exit from the WAIT mode. If an external and a timer interrupt occur at the same time, the external interrupt is serviced first; then, if the timer interrupt request is not cleared in the external interrupt routine, the normal timer interrupt (not the timer WAIT interrupt) is serviced since the MCU is no longer in the WAIT mode.

Timer

The MPU timer contains a single 8-bit software programmable counter with 7-bit software selectable prescaler. The counter may be preset under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit, i.e., bit 7 of the Timer Control Register (TCR) is set. Then if the timer interrupt is not masked, i.e., bit 6 of the TCR and the I-bit in the Condition Code Register are both cleared, the processor receives an interrupt. After completion of the current instruction, the processor proceeds to the store the appropriate registers on the stack, and then fetches the timer vector address from locations $1FF8 and $1FF9 ($FFF8 and $FFF9) in order to begin servicing the interrupt, unless it was in locations $1FF6 and $1FF7 ($FFF6 and $FFF7) the WAIT mode.

The counter continues to count after it reaches zero, allowing the software to determine the number of internal or external input clocks since the timer interrupt request bit was set. The counter may read at any time by the processor without disturbing the count. The contents of the counter becomes stable prior to the read portion of a cycle and does not change during the read. The timer interrupt request bit remains set until cleared by the software. If this happens before the timer interrupt is serviced, the interrupt is lost. TCR7 may also be used as a scanned status bit in a non-interrupt mode of operation (TCR = 1).

The prescaler is a 7-bit divider which is used to extend the maximum length of the timer. Bit 0, bit 1, and bit 2 of the TCR are programmed to choose the appropriate prescaler output which is used as the counter input. The processor cannot write into or read from the prescaler; however, its contents are cleared to all “0’s” by the write operation into TCR when bit 3 of the written data equals 1, which allows for truncation free counting.

The Timer input can be configured for three different operating modes, plus a disable mode depending on the value written to the TCR4, TCR5 control bits. Refer to the Timer Control Register section.

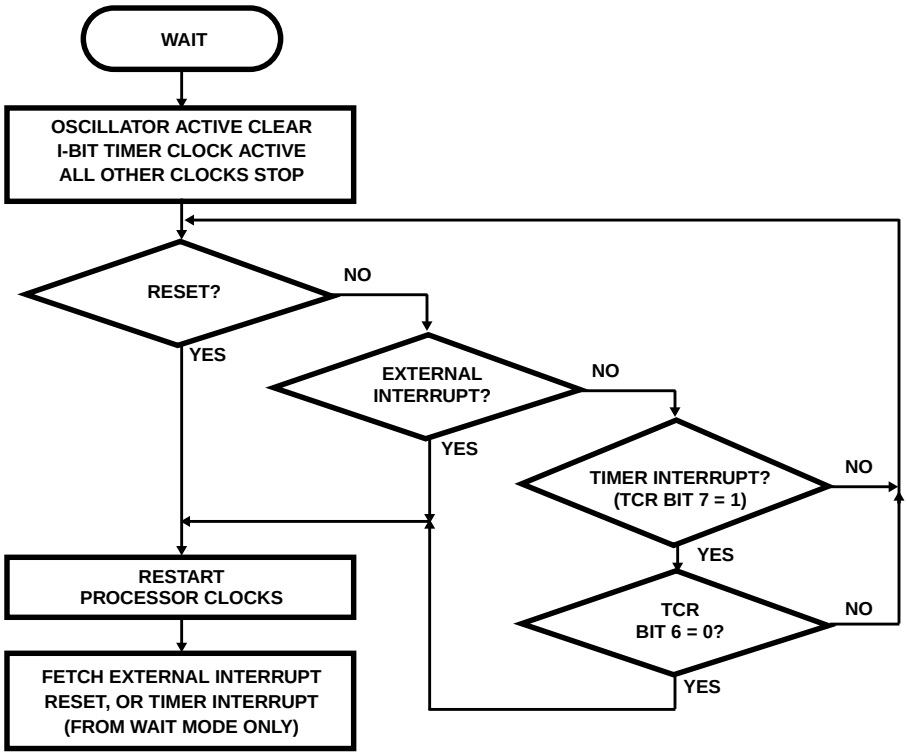
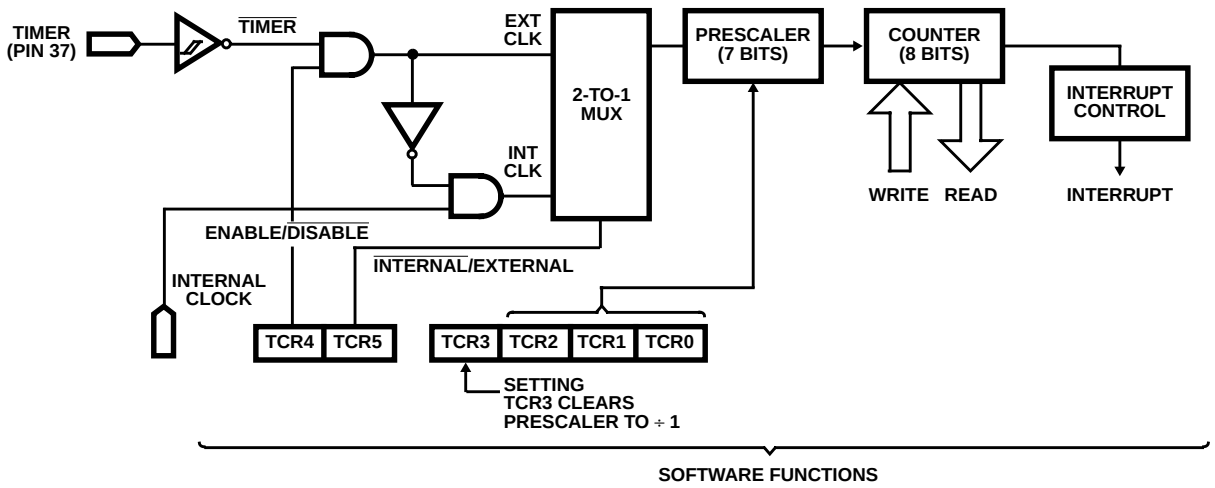


FIGURE 18. WAIT FUNCTION FLOW CHART



NOTES:

12. Prescaler and 8-bit counter are clocked falling edge of the internal clock (AS) or external input.

13. Counter is written to during Data Strobe (DS) and counts down continuously.

FIGURE 19. TIMER BLOCK DIAGRAM

Timer Input Mode 1 - If TCR4 and TCR5 are both programmed to a “0”, the input to the Timer is from an internal clock and the Timer input is disabled. The internal clock mode can be used for periodic interrupt generation, as well as a reference in frequency and event measurement. The internal clock is the instruction cycle clock and is coincident with Address Strobe (AS) except during a WAIT instruction. During a WAIT instruction the AS pin goes to a low state but the internal clock to the Timer continues to run at its normal rate.

Timer Input Mode 2 - With TCR4 = 1 and TCR5 = 0, the internal clock and the TIMER input pin are ANDed together to form the Timer input signal. This mode can be used to measure external pulse widths. The external pulse simply turns on the internal clock for the duration of the pulse. The resolution of the count in this mode is ±1 clock and therefore accuracy improves with longer input pulse widths.

Timer Input Mode 3 - If TCR4 = 0 and TCR5 = 1, then all inputs to the Timer are disabled.

Timer Input Mode 4 - If TCR4 = 1 and TCR5 = 1, the internal clock input to the Timer is disabled and the TIMER input pin becomes the input to the Timer. The external Timer pin can, in this mode, be used to count external events as well as external frequencies for generating periodic interrupts.

Figure 19 shows a block diagram of the Timer subsystem. Power-On-Reset and the STOP instruction cause the counter to be set to $F0.

TIMER CONTROL REGISTER (TCR)

7	6	5	4	3	2	1	0
TCR7	TCR6	TCR5	TCR4	TCR3	TCR2	TCR1	TCR0

All bits in this register except bit 3 are Read/Write bits.

TCR7 - Timer interrupt request bit: bit used to indicate the timer interrupt when it is logic “1”.

1 - Set whenever the counter decrements to zero, or under program control.

0 - Cleared on external reset, power-on-reset, STOP instruction, or program control.

TCR6 - Timer interrupt mask bit, when this bit is a logic “1” it inhibits the timer interrupt to the processor.

1 - Set on external reset, power-on-reset, STOP instruction, or program control.

0 - Cleared under program control.

TCR5 - External or internal bit: selects the input clock source to be either the external timer pin or the internal clock. (Unaffected by $\overline{\text{RESET}}$.)

1 - Select external clock source.

0 - Select internal clock source (AS).

TCR4 - External enable bit: control used to enable the external timer pin. (Unaffected by $\overline{\text{RESET}}$.)

1 - Enable external timer pin.

0 - Disable external timer pin.

TCR5	TCR4	
0	0	Internal Clock (AS) to Timer.
0	1	AND of Internal Clock (AS) and TIMER Pin to Timer.
1	0	Inputs to Timer Disabled.
1	1	TIMER Pin to Timer.

Refer to Figure 19 for Logic Representation.

TCR3 - Timer Prescaler Reset bit: writing a “1” to this bit resets the prescaler to zero. A read of this location always indicates a “0”. (Unaffected by $\overline{\text{RESET}}$.)

TCR2, TCR1, TCR0 - Prescaler address bits: decoded to select one of eight taps on the prescaler. (Unaffected by $\overline{\text{RESET}}$).

PRESCALER

TCR2	TCR1	TCR0	RESULT
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	÷ 128

System Configuration

Figures 20 through 24 show in general terms how the CDP6805E2 bus structure may be utilized. Specified interface details vary with the various peripheral and memory devices employed.

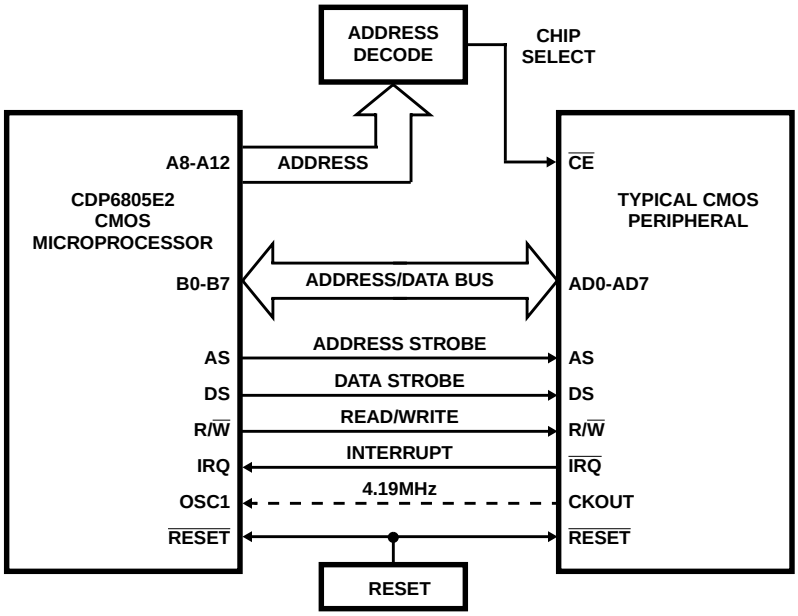
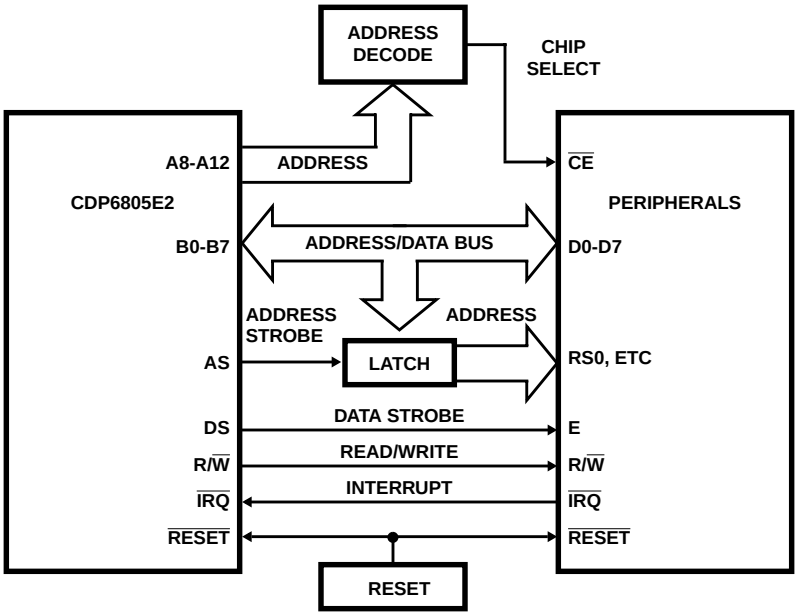


FIGURE 20. CONNECTION TO CMOS PERIPHERALS



NOTE: In some cases, pullup resistors or other level shifting techniques may be required on signals going from NMOS to CMOS parts.

FIGURE 21. CONNECTION TO PERIPHERALS

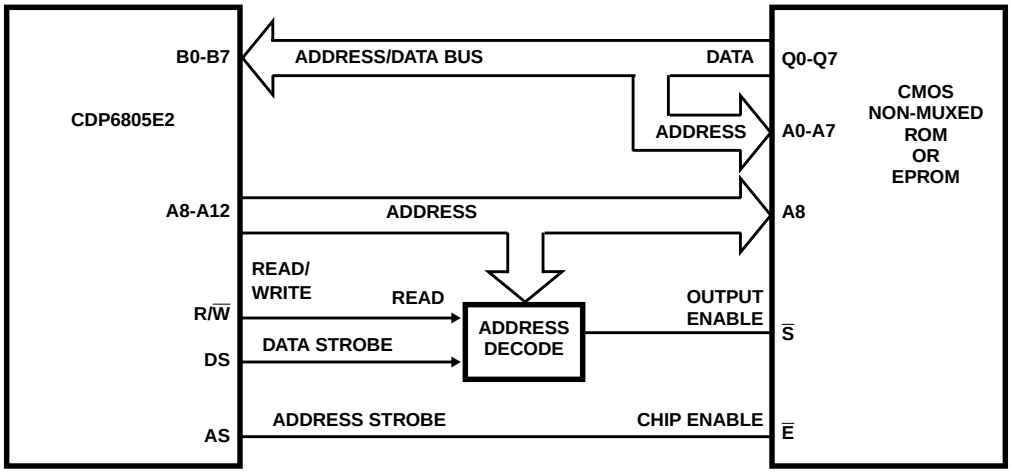


FIGURE 22. CONNECTION TO LATCH NON-MULTIPLEXED CMOS ROM OR EPROM

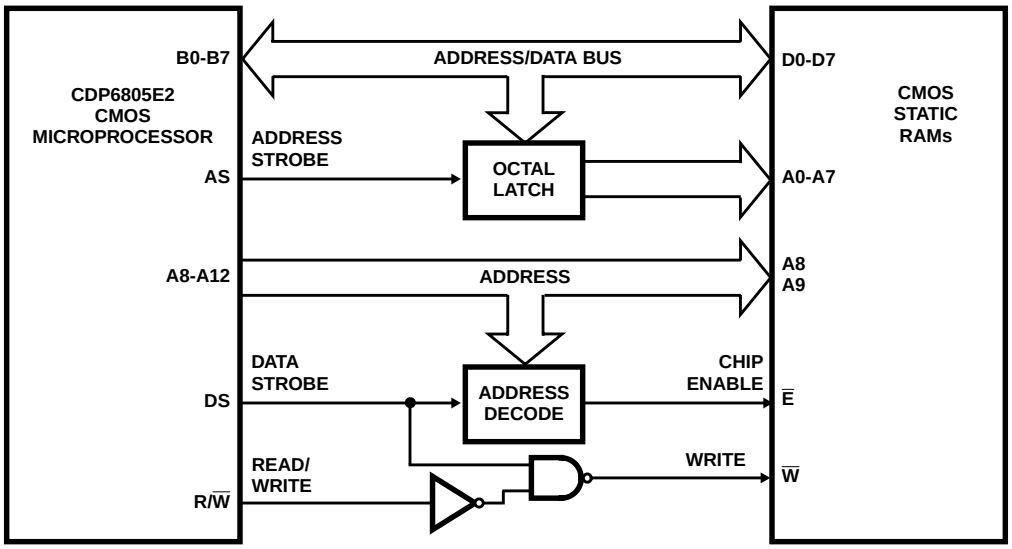


FIGURE 23. CONNECTION TO STATIC CMOS RAMs

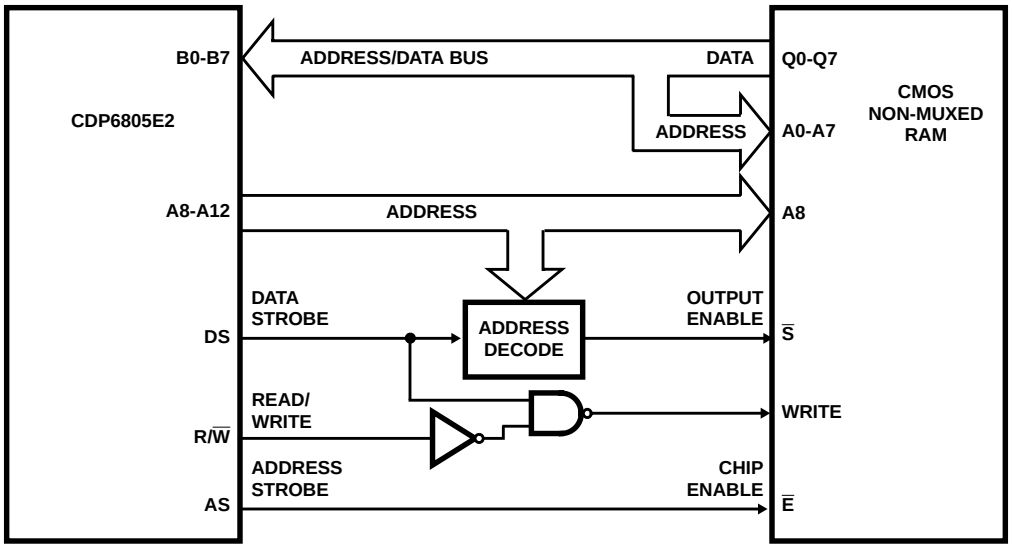


FIGURE 24. CONNECTION TO LATCHED NON-MULTIPLEXED CMOS RAM

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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