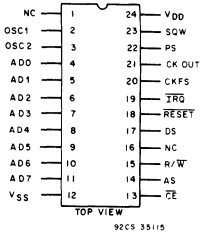
CDP6818



TERMINAL ASSIGNMENT

CMOS Real-Time Clock with RAM

Features:

- *Low-Power, High-Speed, High-Density CMOS*
- *Internal Time Base and Oscillator*
- *Counts Seconds, Minutes, and Hours of the Day*
- *Counts Days of the Week, Date, Month, and Year*
- *3 V to 6 V Operation*
- *Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz*
- *Time Base Oscillator for Parallel Resonant Crystals*
- *40 to 200 µW Typical Operating Power at Low Frequency Time Base*
- *4.0 to 20 mW Typical Operating Power at High Frequency Time Base*
- *Binary or BCD Representation of Time, Calendar, and Alarm*
- *12- or 24-Hour Clock with AM and PM in 12-Hour Mode*
- *Daylight Savings Time Option*
- *Automatic End of Month Recognition*
- *Automatic Leap Year Compensation*
- *Microprocessor Bus Compatible*
- *MOTEL Circuit for Bus Universality*
- *Multiplexed Bus for Pin Efficiency*
- *Interfaced with Software as 64 RAM Locations*
- *14 Bytes of Clock and Control Registers*
- *50 Bytes of General Purpose RAM*
- *Status Bit Indicates Data Integrity*
- *Bus Compatible Interrupt Signals (IRQ)*
- *Three Interrupts are Separately Software Maskable and Testable*
  - *Time-of-Day Alarm, Once-per-Second to Once-per-Day*
  - *Periodic Rates from 30.5 µs to 500 ms*
  - *End-of-Clock Update Cycle*
- *Programmable Square-Wave Output Signal*
- *Clock Output May Be Used as Microprocessor Clock Input*
  - *At Time Base Frequency +1 or +4*
- *24-Pin Dual-In-Line Package*

The CDP6818 Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with many 8-bit microprocessors, microcomputers, and larger computers. This device combines three unique features: a complete time-of-day clock with alarm and one hundred year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The CDP6818 uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS device (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the CDP6818 may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the CDP6805E2.

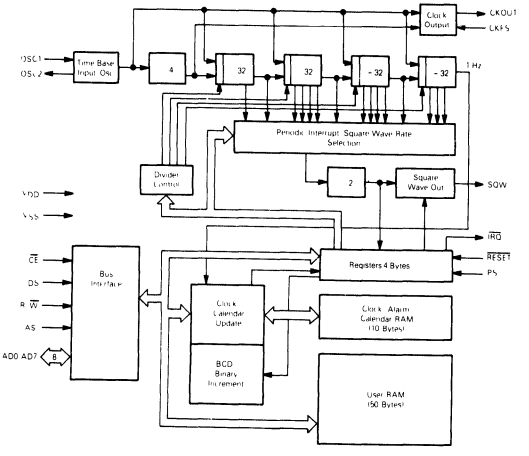


Fig. 1 - Block diagram.

File Number **1375**

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0 3 to +8	V
All Input Voltages	V_{in}	V_{SS}−0 5 to V_{DD}+0 5	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I	10	mA
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5 Vdc ±10%, V_{SS}=0 Vdc, T_A=0° to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Frequency of Operation	f_{osc}	32.768	4194.304	kHz
Output Voltage	V_{OL}	−	0.1	V
I_{Load}< 10 μA	V_{OH}	V_{DD}−0.1	−	
I_{DD} − Bus Idle (External clock) CKOUT=f_{osc}, C_L=15 pF; SQW Disabled, $\overline{CE}$=V_{DD}−0 2, C_L (OSC2)=10 pF				
f_{osc}=4 194304 MHz	I_{DD1}	−	3	mA
f_{osc}=1 048516 MHz	I_{DD2}	−	0.8	mA
f_{osc}=32 768 kHz	I_{DD3}	−	50	μA
I_{DD} − Quiescent f_{osc}=DC; OSC1=DC, All Other Inputs=V_{DD}−0 2 V, No Clock	I_{DD4}	−	50	μA
Output High Voltage AD0-AD7 CKOUT (I_{Load}=−1.6 mA, SQW, I_{Load}=−1.0 mA)	V_{OH}	4 1	−	V
Output Low Voltage AD0-AD7 CKOUT (I_{Load}=1 6 mA, $\overline{IRQ}$, and SQW, I_{Load}=1 0 mA)	V_{OL}	−	0.4	V
Input High Voltage — CKFS, AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$, PS	V_{IH}	V_{DD}−2	V_{DD}	V
$\overline{RESET}$		V_{DD}−0.8	V_{DD}	
OSC1		V_{DD}−1	V_{DD}	
Input Low Voltage — AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$	V_{IL}	V_{SS}	0.8	V
CKFS, PS, $\overline{RESET}$		V_{SS}	0.8	
OSC1		V_{SS}	0.8	
Input Current — All Inputs	I_{in}	−	±1	μA
Three-State Leakage — AD0-AD7	I_{TSL}	−	±10	μA

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3 Vdc, V_{SS} = 0 Voc, T_A = 0° to 70°C unless otherwise noted)

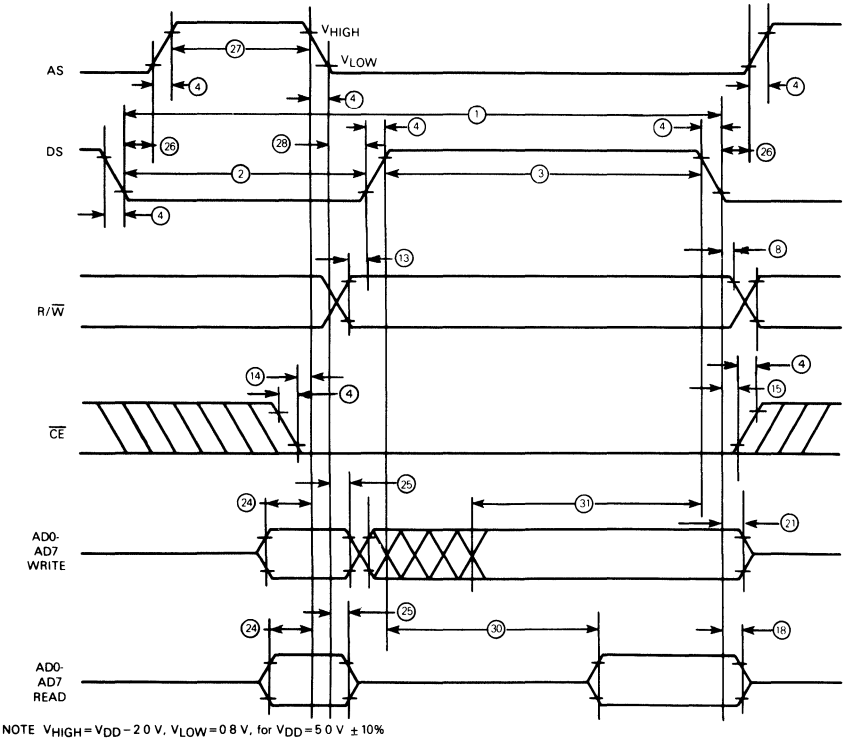
Characteristics	Symbol	Min	Max	Unit
Frequency of Operation	f_{OSC}	32.768	32.768	kHz
Output Voltage	V_{OL}	—	0.1	V
I_{LOAD} < 10 μ A	V_{OH}	V_{DD}-0.1	—	
I_{DD} — Bus Idle CKOUT = f_{osc}, C_L = 15 pF, SQW Disabled, $\overline{CE}$ = V_{DD}-0.2, C_L (OSC2) = 10 pF f_{osc} = 32.768 kHz	I_{DD3}	—	50	μA
I_{DD} — Quiscent f_{osc} = DS; OSC1=DC, All Other Inputs = V_{DD}-0 2 V, No Clock	I_{DD4}	—	50	μA
Output High Voltage (L_{Load} = -0.25 mA, All Outputs)	V_{OH}	2.7	—	V
Output Low Voltage (I_{Load} = 0 25 mA, All Outputs)	V_{OL}	—	0.3	V
Input High Voltage — AD0-AD7, DS, AS, R/$\overline{W}$, $\overline{CE}$,	V_{IH}	2.1	V_{DD}	V
$\overline{RESET}$, CKFS, PS, OSC1		2.5	V_{DD}	
Input Low Voltage (All Inputs)	V_{IL}	V_{SS}	0.5	V
Input Current — All Inputs	I_{in}	—	±1	μA
Three-State Leakage — $\overline{IRQ}$, AD0-AD7	I_{TSL}	—	±10	μA

CDP6818

BUS TIMING

Ident. Number	Characteristics	Symbol	V_{DD} = 3.0 V 50 pF Load		V_{DD} = 5.0 V ± 10% 2 TTL and 130 pF Load		Unit
			Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	5000	—	953	dc	ns
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	1000	—	300	—	ns
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	1500	—	325	—	ns
4	Input Rise and Fall Time	t_r, t_f	—	100	—	30	ns
8	R/$\overline{W}$ Hold Time	t_{RWH}	10	—	10	—	ns
13	R/$\overline{W}$ Setup Time Before DS/E	t_{RWS}	200	—	80	—	ns
14	Chip Enable Setup Time Before AS/ALE Fall	t_{CS}	200	★	55	★	ns
15	Chip Enable Hold Time	t_{CH}	10	—	0	—	ns
18	Read Data Hold Time	t_{DHR}	10	1000	10	100	ns
21	Write Data Hold Time	t_{DHW}	100	—	0	—	ns
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	200	—	50	—	ns
25	Muxed Address Hold Time	t_{AHL}	100	—	20	—	ns
26	Delay Time DS/E to AS/ALE Rise	t_{ASD}	500	—	50	—	ns
27	Pulse Width, AS/ALE High	PW_{ASH}	600	—	135	—	ns
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	500	—	60	—	ns
30	Peripheral Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	1300	—	20	240	ns
31	Peripheral Data Setup Time	t_{DSW}	1500	—	200	—	ns

NOTE: Designations E, ALE, $\overline{RD}$, and $\overline{WR}$ refer to signals from alternative microprocessor signals
★See Important Application Notice (refer to Fig 23)



NOTE $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10%

Fig. 2 — CDP6818 bus timing waveforms

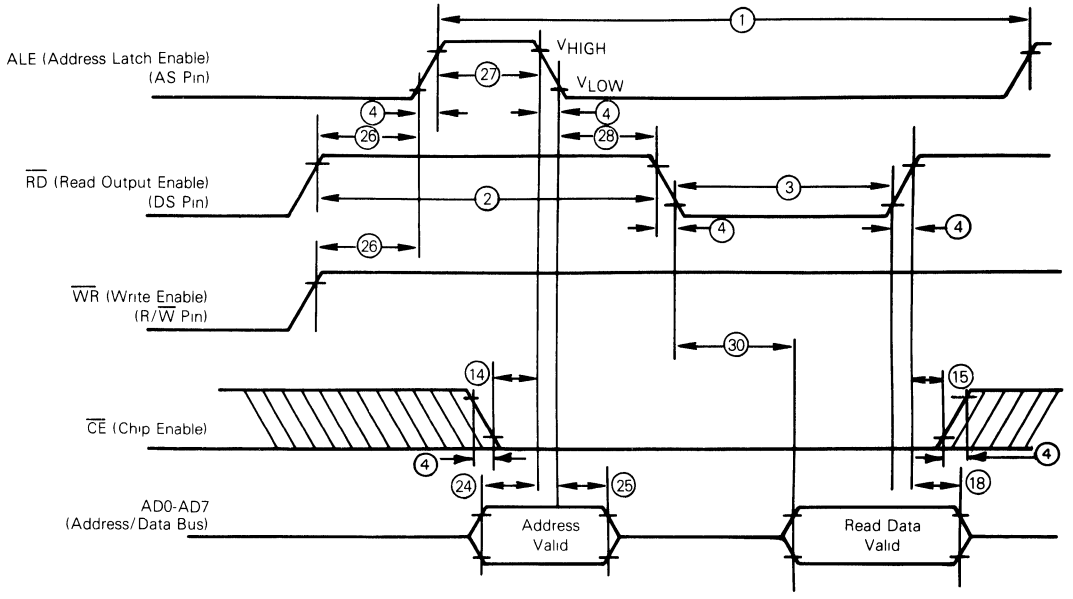
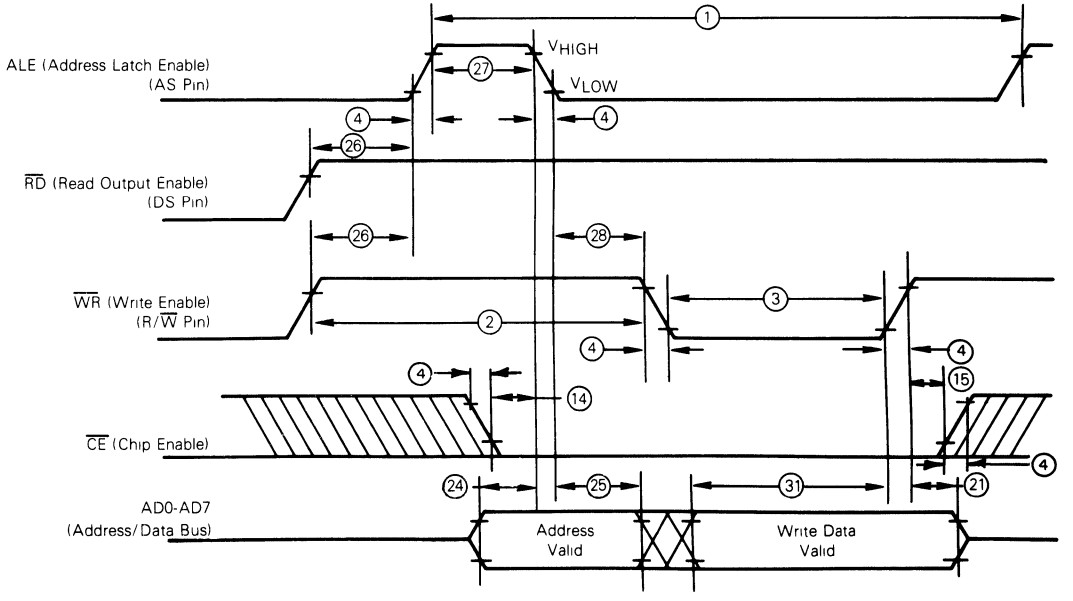


Fig 3 — Bus-read timing competitor multiplexed bus.



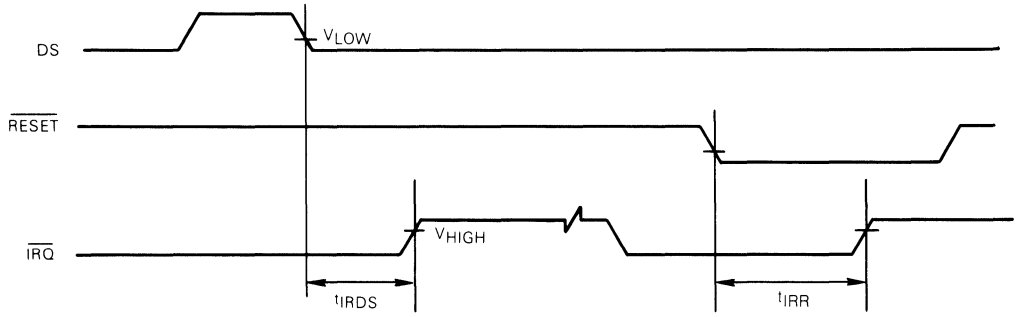
NOTE $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ±10%

Fig. 4 — Bus-write timing competitor multiplexed bus.

CDP6818

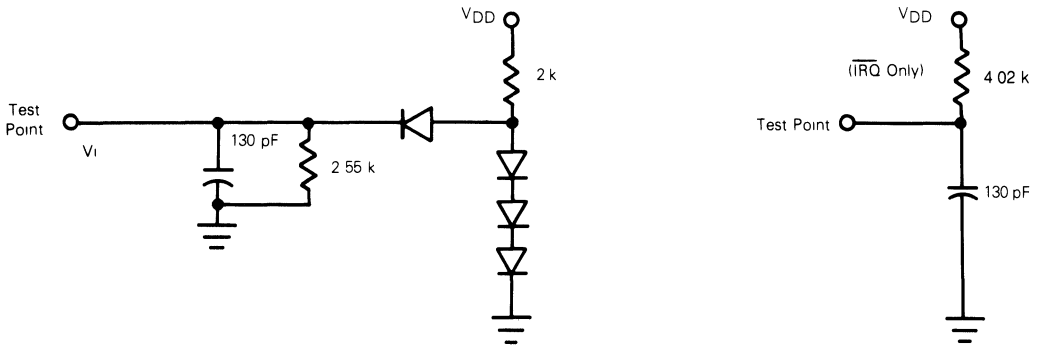
TABLE 1 — SWITCHING CHARACTERISTICS (V_{DD} = 5 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 0° to 70°C)

Description	Symbol	Min	Max	Unit
Oscillator Startup	t_{RC}	—	100	ms
Reset Pulse Width	t_{RWL}	5	—	μs
Reset Delay Time	t_{RLH}	5	—	μs
Power Sense Pulse Width	t_{PWL}	5	—	μs
Power Sense Delay Time	t_{PLH}	5	—	μs
$\overline{IRQ}$ Release from DS	t_{IRDS}	—	2	μs
$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}	—	2	μs
VRT Bit Delay	t_{VRTD}	—	2	μs



NOTE $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V, for $V_{DD} = 5.0$ V ± 10%

Fig. 5 — $\overline{IRQ}$ release delay timing waveforms.



All Outputs Except OSC2 (See Figure 10)

Fig. 6 — TTL equivalent test load.

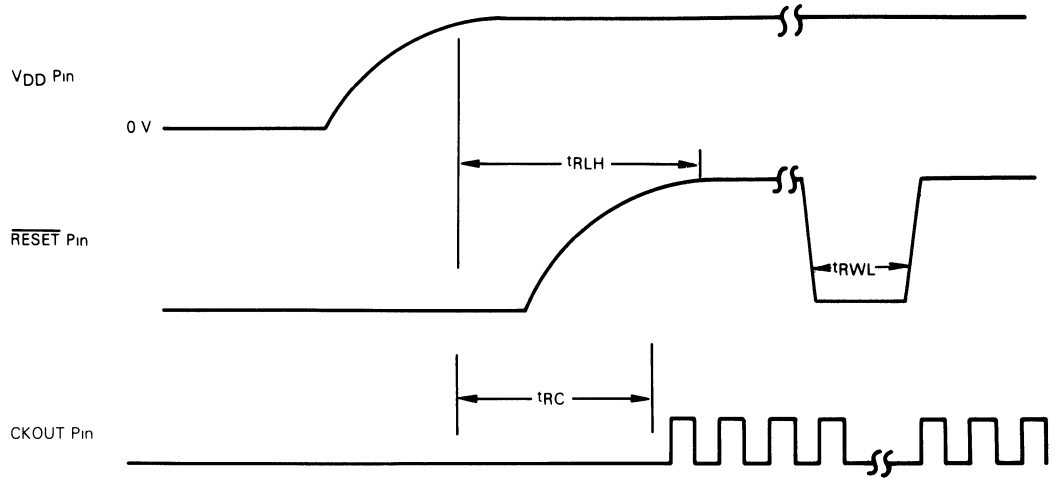
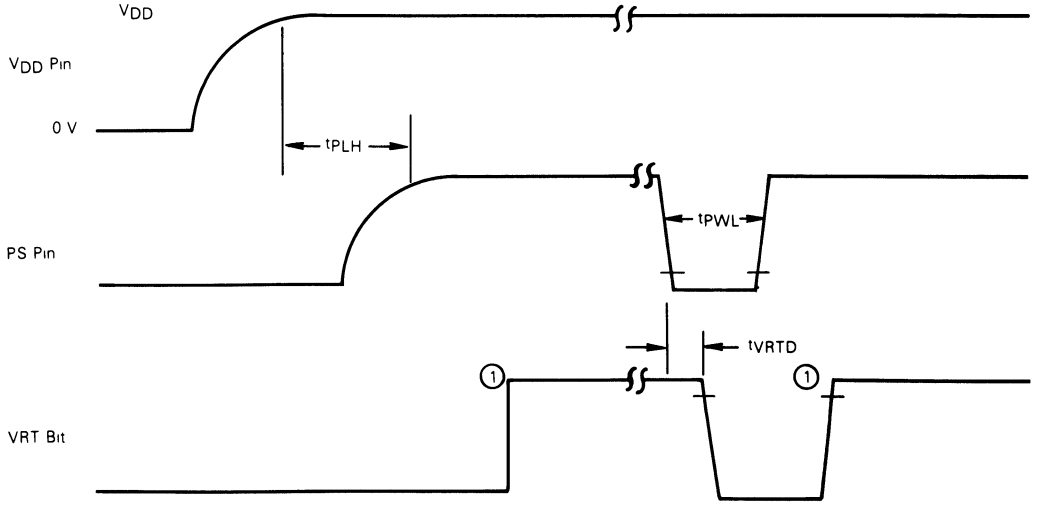


Fig. 7 — Power-up timing waveforms.



(1) The VRT bit is set to a "1" by reading Control Register #D The VRT Bit can only be cleared by pulling the PS Pin low (see REGISTER D ($OD))

Fig. 8 — Conditions that clear VRT bit timing waveforms.

CDP6818

MOTEL

The MOTEL circuit is a new concept that permits the CDP6818 to be directly interfaced with many types of microprocessors No external logic is needed to adapt to the differences in bus control signals from common multiplexed bus microprocessors

Practically all microprocessors interface with one of two synchronous bus structures

The MOTEL circuit is built into peripheral and memory ICs to permit direct connection to either type of bus An industry standard bus structure is now available The MOTEL concept is shown logically in Figure 9.

MOTEL selects one of two interpretations of two pins In the 6805 case, DS and R/$\overline{W}$ are gated together to produce the internal read enable The internal write enable is a similar gating of the inverse of R/$\overline{W}$ With competitor buses, the inversion of $\overline{RD}$ and $\overline{WR}$ create functionally identical internal read and write enable signals

The CDP6818 automatically selects the processor type by using AS/ALE to latch the state of the DS/$\overline{RD}$ pin Since DS is always low and $\overline{RD}$ is always high during AS and ALE, the latch automatically indicates which processor type is connected.

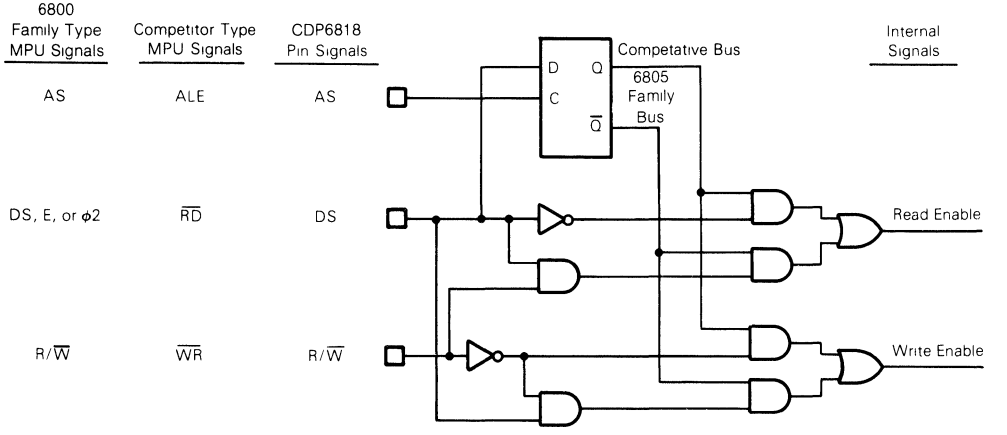


Fig. 9 — Functional diagram of MOTEL circuit

SIGNAL DESCRIPTIONS

The block diagram in Figure 1, shows the pin connection with the major internal functions of the CDP6818 Real-Time Clock plus RAM The following paragraphs describe the function of each pin

V_{DD}, V_{SS}

DC power is provided to the part on these two pins, V_{DD} being the most positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC1, OSC2 — TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1 as shown in Figure 10 The time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant AT cut crystal at 4 194304 MHz or 1.048576 MHz frequencies The crystal connections are shown in Figure 11 and the crystal characteristics in Figure 12

CKOUT — CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4 A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 2

CKFS — CLOCK OUT FREQUENCY SELECT, INPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4 CKFS tied to V_{DD} causes CKOUT to be the same frequency as the time base at the OSC1 pin When CKFS is at V_{SS}, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS

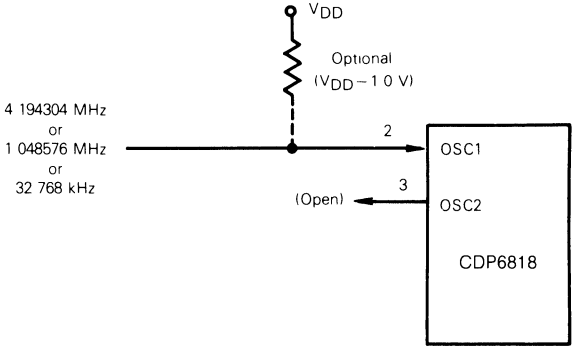
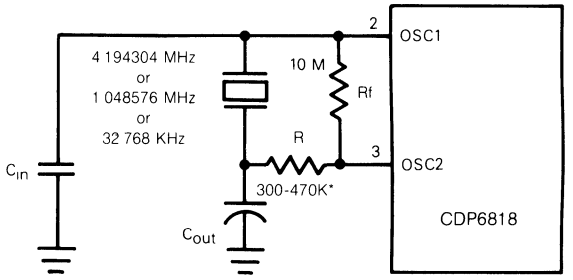
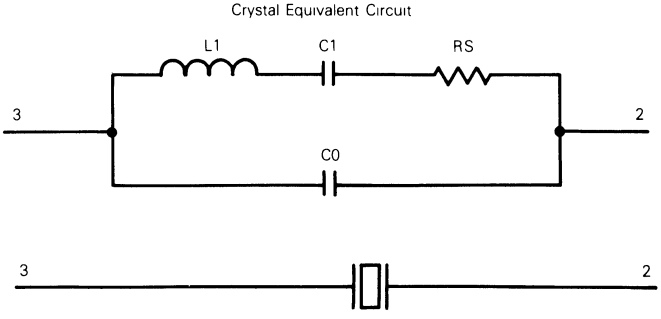


Fig 10 — External Time-base connection



*32 768 KHz — Consult manufacturers specification

Fig 11 — Crystal oscillator connection



f_{osc}	4.194304 MHz.	1.048576 MHz	32.768 KHz
Rs max	75 Ω	700 Ω	50 K
C0 max	7 pF	5 pF	1.7 pF
C1	0 012 pF	0.008 pF	0 003 pF
C_{in}/C_{out}	15-30 pF	15-40 pF	10-22 pF
Q	50 k	35 k	30 k
R	—	—	300-470 K
R_f	10M	10M	22M

Fig. 12 — Crystal parameters

TABLE 2 — CLOCK OUTPUT FREQUENCIES

Time Base (OSC1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4 194304 MHz	High	4 194304 MHz
4 194304 MHz	Low	1 048576 MHz
1 048576 MHz	High	1 048576 MHz
1 048576 MHz	Low	262 144 kHz
32 768 kHz	High	32 768 kHz
32 768 kHz	Low	8 192 kHz

SQW — SQUARE WAVE, OUTPUT

The SQW pin can output a signal one of 15 of the 22 internal-divider stages The frequency and output enable of the SQW may be altered by programming Register A, as shown in Table 5 The SQW signal may be turned on and off using a bit in Register B

AD0-AD7 — MULTIPLEXED BIDIRECTIONAL ADDRESS/DATA BUS

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data Address-then-data multiplexing does not slow the access time of the CDP6818 since the bus reversal from address to data is occurring during the internal RAM access time

The address must be valid just prior to the fall of AS/ALE at which time the CDP6818 latches the address from AD0 to AD5 Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses In a read cycle, the CDP6818 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in this case of MOTEL or $\overline{RD}$ rises in the other case

AS — MULTIPLEXED ADDRESS STROBE, INPUT

A positive going multiplexed address strobe pulse serves to demultiplex the bus The falling edge of AS or ALE causes the address to be latched within the CDP6818 The automatic MOTEL circuitry in the CDP6818 also latches the state of the DS pin with the falling edge of AS or ALE

DS — DATA STROBE OR READ, INPUT

The DS pin has two interpretations via the MOTEL circuit When emanating from a 6800 type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data

The second MOTEL interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from a competitor type processor In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data This interpretation of DS is also the same as an output-enable signal on a typical memory

The MOTEL circuit, within the CDP6818, latches the state of the DS pin on the falling edge of AS/ALE When the 6800 mode of MOTEL is desired DS must be low during AS/ALE, which is the case with the CDP6805 family of multiplexed bus processors To insure the competitor mode of MOTEL, the DS pin must remain high during the time AS/ALE is high

R/$\overline{W}$ — READ/WRITE, INPUT

The MOTEL circuit treats the R/$\overline{W}$ pin in one of two ways When a 6805 type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, whereas a write cycle is a low on R/$\overline{W}$ during DS

The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from competitor type processors The MOTEL circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMs

$\overline{CE}$ — CHIP ENABLE, INPUT

The chip-enable ($\overline{CE}$) signal must be asserted (low) for a bus cycle in which the CDP6818 is to be accessed $\overline{CE}$ is not latched and must be stable during DS and AS (in the 6805 mode of MOTEL) and during $\overline{RD}$ and $\overline{WR}$ (in the competitor mode) Bus cycles which take place without asserting $\overline{CE}$ cause no actions to take place within the CDP6818 When $\overline{CE}$ is high, the multiplexed bus output is in a high-impedance state

When $\overline{CE}$ is high, all address, data, DS, and R/$\overline{W}$ inputs from the processor are disconnected within the CDP6818 This permits the CDP6818 to be isolated from a powered-down processor When $\overline{CE}$ is held high, an unpowered device cannot receive power through the input pins from the real-time clock power source Battery power consumption can thus be reduced by using a pullup resistor or active clamp on $\overline{CE}$ when the main power is off

$\overline{IRQ}$ — INTERRUPT REQUEST, OUTPUT

The $\overline{IRQ}$ pin is an active low output of the CDP6818 that may be used as an interrupt input to a processor The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C The $\overline{RESET}$ pin also clears pending interrupts

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor

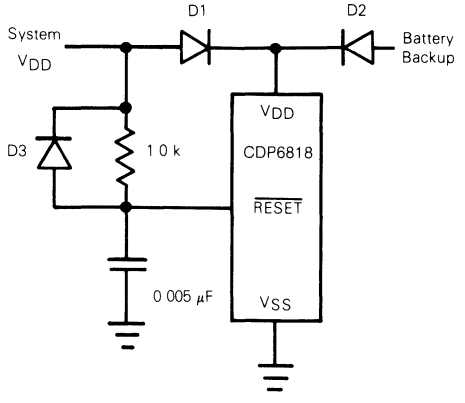
$\overline{RESET}$ — RESET, INPUT

The $\overline{RESET}$ pin does not affect the clock, calendar, or RAM functions On the powerup, the $\overline{RESET}$ pin must be held low for the specified time, t_{RLH}, in order to allow the power supply to stabilize Figure 13 shows a typical representation of the $\overline{RESET}$ pin circuit

When $\overline{RESET}$ is low the following occurs

a) Periodic Interrupt Enable (PIE) bit is cleared to zero,
b) Alarm Interrupt Enable (AIE) bit is cleared to zero,
c) Update ended Interrupt Enable (UIE) bit is cleared to zero,
d) Update ended Interrupt Flag (UF) bit is cleared to zero,
e) Interrupt Request status Flag (IRQF) bit is cleared to zero,
f) Periodic Interrupt Flag (PF) bit is cleared to zero,

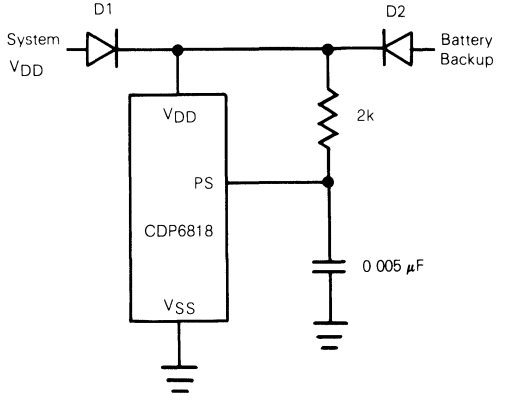
g) Alarm Interrupt Flag (AF) bit is cleared to zero,
h) $\overline{IRQ}$ pin is in high-impedance state, and
i) Square Wave output Enable (SQWE) bit is cleared to zero



D1 = D2 = D3 = 1N4148 or Equivalent

Note If the RTC is isolated from the MPU or MCU power by a diode drop, care must be taken to meet V_{IN} requirements

Fig. 13 — Typical power-up delay circuit for $\overline{RESET}$



D1 = D2 = 1N4148 or Equivalent

Fig. 14 — Typical power-up delay circuit for POWER SENSE.

PS — POWER SENSE, INPUT

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register D. When the PS pin is low the VRT bit is cleared to zero

During powerup, the PS pin must be externally held low for the specified time, t_{PL} As power is applied the VTR bit remains low indicating that the contents of the RAM, time registers, and calendar are not guaranteed. When normal operation commences PS should be permitted to go high after a powerup to allow the VRT bit to be set by a read of Register D Figure 14 shows a typical circuit connection for the power-sense pin

POWER-DOWN CONSIDERATIONS

In most systems, the CDP6818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability.

The chip enable ($\overline{CE}$) pin controls all bus inputs (R/$\overline{W}$, DS, AS, AD0-AD7) $\overline{CE}$, when negated, disallows any unintended modification of the RTC data by the bus. $\overline{CE}$ also reduces power consumption by reducing the number of transitions seen internally

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part

ADDRESS MAP

Figure 15 shows the address map of the CDP6818 The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes All 64 bytes are directly readable and writable by the processor program except Registers C and D which are read only Bit 7 of Register A and the high order bit of the seconds byte are also read only. Bit 7, of the second byte, always reads "0". The contents of the four control and status registers are described in the Register section

TIME, CALENDAR, AND ALARM LOCATIONS

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD)

CDP6818

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD The SET bit may now be cleared to allow updates Once initialized the real-time clock makes all updates in the selected data mode The data mode cannot be changed without reinitializing the 10 data bytes

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23 The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1"

The time, calendar, and alarm bytes are not always accessable by the processor program Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition If any of the 10 bytes are read at this time, the data outputs are undefined The update lockout time is 248 μs at the 4 194304 MHz and 1 048567 MHz time bases and 1948 μs for the 32 768 kHz time base The Update Cycle section shows how to accommodate the update cycle in the processor program

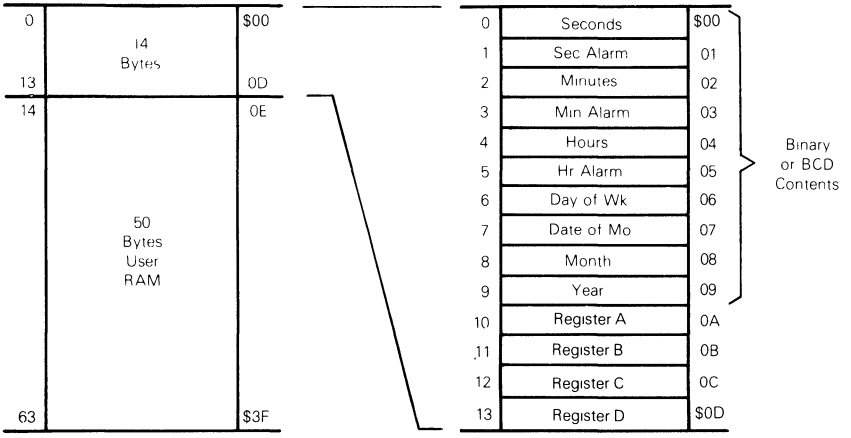


Fig. 15 — Address map.

TABLE 3 — TIME, CALENDAR, AND ALARM DATA MODES

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0-59	$00-$3B	$00-$59	15	21
1	Seconds Alarm	0-59	$00-$3B	$00-$59	15	21
2	Minutes	0-59	$00-$3B	$00-$59	3A	58
3	Minutes Alarm	0-59	$00-$3B	$00-$59	3A	58
4	Hours (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours (24 Hour Mode)	0-23	$00-$17	$00-$23	05	05
5	Hours Alarm (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0-23	$00-$17	$00-23	05	05
6	Day of the Week Sunday = 1	1-7	$01-$07	$01-$07	05	05
7	Day of the Month	1-31	$01-$1F	$01-$31	0F	15
8	Month	1-12	$01-$0C	$01-$12	02	02
9	Year	0-99	$00-$63	$00-$99	4F	79

*Example 5 58 21 Thursday February 15 1979 (Time is A M)

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

STATIC CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the CDP6818. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional CDP6818S may be included in the system. The time/calendar functions may be disabled by holding the DV0-DV2 dividers, in Register A, in the reset state or by setting the SET bit in CR2 Register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. Bit 7 of Register A, Registers C and D, and the high-order Bit of the seconds byte cannot effectively be used as general purpose RAM.

INTERRUPTS

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 μs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to a interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the IRQ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{IRQ}$ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One, two, or three flag bits may be found to be set when Register C is read. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the $\overline{IRQ}$ pin is being driven low.

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

DIVIDER STAGES

The CDP6818 has 22 binary-divider stages following the time base as shown in Figure 1. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controlled by three divider bits (DV2, DV1, and DV0) in Register A.

DIVIDER CONTROL

The divider-control bits have three uses, as shown in Table 4. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz). The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later. The divider-control bits are also used to facilitate testing the CDP6818.

TABLE 4 — DIVIDER CONFIGURATIONS

Time-Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4 194304 MHz	0	0	0	Yes	–	N = 0
1 048576 MHz	0	0	1	Yes	–	N = 2
32 768 kHz	0	1	0	Yes	–	N = 7
Any	1	1	0	No	Yes	–
Any	1	1	1	No	Yes	–

Note Other combinations of divider bits are used for test purposes only

SQUARE-WAVE OUTPUT SELECTION

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 1 The first purpose of selecting a divider tap is to generate a square-wave output signal on the SQW pin Four bits in Register A establish the square-wave frequency as listed in Table 5 The SQW frequency selection shares the 1-of-15 selector with periodic interrupts

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymetrical waveform at the time of execution The square-wave output pin has a number of potential uses For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control

PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500 ms to once every 30 517 μs The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day

Table 5 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency Changing one also changes the other But each function may be separately enabled so that a program could switch between the two features or use both The SQW pin is enabled by the SQWE bit. Similarly the periodic interrupt is enabled by the PIE bit in Register B

Periodic interrupt is usable by practically all real-time systems It can be used to scan for all forms of inputs from contact closures to serial receive bits on bytes It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function

TABLE 5 — PERIODIC INTERRUPT RATE AND SQUARE WAVE OUTPUT FREQUENCY

Rate Select Control Register A				4.194304 or 1.048576 MHz Time Base		32.768 kHz Time Base	
RS3	RS2	RS1	RS0	Periodic Interrupt Rate t_{PI}	SQW Output Frequency	Periodic Interrupt Rate t_{PI}	SQW Output Frequency
0	0	0	0	None	None	None	None
0	0	0	1	30 517 μs	32 768 kHz	3 90625 ms	256 Hz
0	0	1	0	61 035 μs	16 384 kHz	7 8125 ms	128 Hz
0	0	1	1	122 070 μs	8 192 kHz	122 070 μs	8 192 kHz
0	1	0	0	244 141 μs	4 096 kHz	244 141 μs	4 096 kHz
0	1	0	1	488 281 μs	2 048 kHz	488 281 μs	2 048 kHz
0	1	1	0	976 562 μs	1 024 kHz	976 562 μs	1 024 kHz
0	1	1	1	1 953125 ms	512 Hz	1 953125 ms	512 Hz
1	0	0	0	3 90625 ms	256 Hz	3 90625 ms	256 Hz
1	0	0	1	7 8125 ms	128 Hz	7 8125 ms	128 Hz
1	0	1	0	15 625 ms	64 Hz	15 625 ms	64 Hz
1	0	1	1	31 25 ms	32 Hz	31 25 ms	32 Hz
1	1	0	0	62 5 ms	16 Hz	62 5 ms	16 Hz
1	1	0	1	125 ms	8 Hz	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz	500 ms	2 Hz

UPDATE CYCLE

The CDP6818 executes an update cycle once-per-second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in Register B is clear The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions

With a 4 194304 MHz or 1 048576 MHz time base the update cycle takes 248 μs while a 32 768 kHz time base update cycle takes 1984 μs During the update cycle, the time, calendar, and alarm bytes are not accessable by the processor program The CDP6818 protects the program from reading transitional data This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle If the processor reads these RAM locations before the update is complete the output will be undefined The update in progress (UIP) status bit is set during the interval

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts Three methods of accommodating nonavailability during update are usable by the program In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day

The first method of avoiding the update cycle uses the update-ended interrupt If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information During this time a display could be updated or the information could be transfered to continuously available RAM Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not The UIP bit will pulse once-per-second Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts After the UIP bit goes high, the update cycle begins 244 μs later Therefore, if a low is read on the UIP bit, the user has at least 244 μs before the time/calendar data will be changed If a "1" is read in the UIP bit, the time/calendar data may not be valid The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 μs

The third method uses a periodic interrupt to determine if an update cycle is in progress The UIP bit in Register A is set high between the setting of the PF bit on Register C (see Figure 16). Periodic interrupts that occur at intervals greater than $t_{BUC} + t_{UC}$ allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(T_{PI} \div 2) + t_{BUC}$ to insure that data is not read during the update cycle To properly set the internal counters for Daylight Savings Time operation, the user must set the time at least two seconds before the rollover will occur Likewise, the time must be set at least two seconds before the end of the 29th or 30th day of the month.

REGISTERS

The CDP6818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle

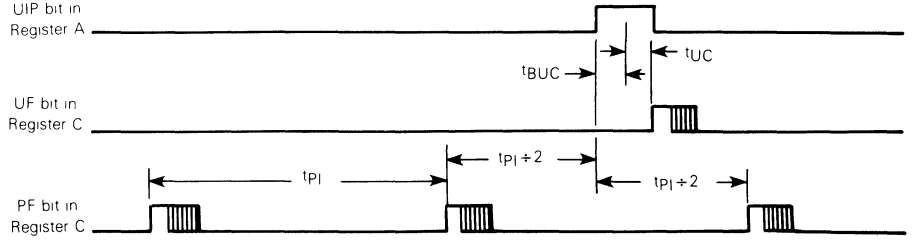
REGISTER A ($0A)

MSB							LSB	Read/Write
b7	b6	b5	b4	b3	b2	b1	b0	Register
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	except UIP

UIP — The update in progress (UIP) bit is a status flag that may be monitored by the program When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 μs (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero — it is not in transition The UIP bit is a read-only bit, and is not affected by Reset Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit.

TABLE 6 — UPDATE CYCLE TIMES

UIP Bit	Time Base (OSC1)	Update Cycle Time (t_{UC})	Minimum Time Before Update Cycle (t_{BUC})
1	4 194304 MHz	248 μs	–
1	1 048576 MHz	248 μs	–
1	32 768 kHz	1984 μs	–
0	4 194304 MHz	–	244 μs
0	1 048576 MHz	–	244 μs
0	32 768 kHz	–	244 μs



t_{PI} = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62 5 ms etc per Table 5)
t_{UC} = Update Cycle Time (248 μs or 1984 μs)
t_{BUC} = Delay Time Before Update Cycle (244 μs)

Fig. 16 — Update-ended and periodic interrupt relationships.

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DV2, DV1, DV0 – Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 4 shows that time bases of 4 194304 MHz, 1 048576 MHz, and 32 768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins one-half second later. These three read/write bits are not affected by $\overline{\text{RESET}}$.

RS3, RS2, RS1, RS0 – The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tape selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following. 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 5 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by $\overline{\text{RESET}}$.

REGISTER B ($0B)

MSB							LSB	Read/Write Register
b7	b6	b5	b4	b3	b2	b1	b0	
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	

SET – When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is read/write bit which is not modified but $\overline{\text{RESET}}$ or internal functions of the CDP6818.

PIE – The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the $\overline{\text{IRQ}}$ pin to be driven low. A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A zero in PIE blocks $\overline{\text{IRQ}}$ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal CDP6818 functions, but is cleared to "0" by a $\overline{\text{RESET}}$.

AIE – The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE – The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flage (UF) bit to assert $\overline{\text{IRQ}}$. The $\overline{\text{RESET}}$ pin going low or the SET bit going high clears the UIE bit.

SQWE – When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a zero the SQW pin is held low. The state of SQWE is cleared by the $\overline{\text{RESET}}$ pin. SQWE is a read/write bit.

DM – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{\text{RESET}}$. A "1" in DM signifies binary data, while a "0" in DM specifies binary-coded-decimal (BCD) data.

24/12 – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by the software.

DSE – The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1 59 59 AM to 3 00 00 AM. On the last Sunday in October when the time first reaches 1 59 59 AM it changes to 1 00 00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or $\overline{\text{RESET}}$.

REGISTER C ($0C)

MSB							LSB	Read-Only Register
b7	b6	b5	b4	b3	b	b1	b0	
IRQF	PF	AF	UF	0	0	0	0	

IRQF – The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = "1"

AF = AIE = "1"

UF = UIE = "1"

i e , IRQF = PF•PIE + AF•AIE + UF•UIE

Any time the IRQF bit is a "1", the $\overline{\text{IRQ}}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{\text{RESET}}$ pin is low.

PF – The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{\text{IRQ}}$ signal and sets the IRQF bit when PIE is also a "1 ". The PF bit is cleared by a $\overline{\text{RESET}}$ or a software read of Register C.

AF – A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{\text{IRQ}}$ pin to go low, and a "1" to appear in the IRQF bit, when the AIE bit also is a "1 " A $\overline{\text{RESET}}$ or a read of Register C clears AF.

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{\text{IRQ}}$. UF is cleared by a Register C read or a $\overline{\text{RESET}}$.

b3 TO b0 – The unused bits of Status Register 1 are read as "0's". They can not be written.

REGISTER D ($0D)

MSB							LSB	
b7	b6	b5	b4	b3	b2	b1	b0	Read Only
VRT	0	0	0	0	0	0	0	Register

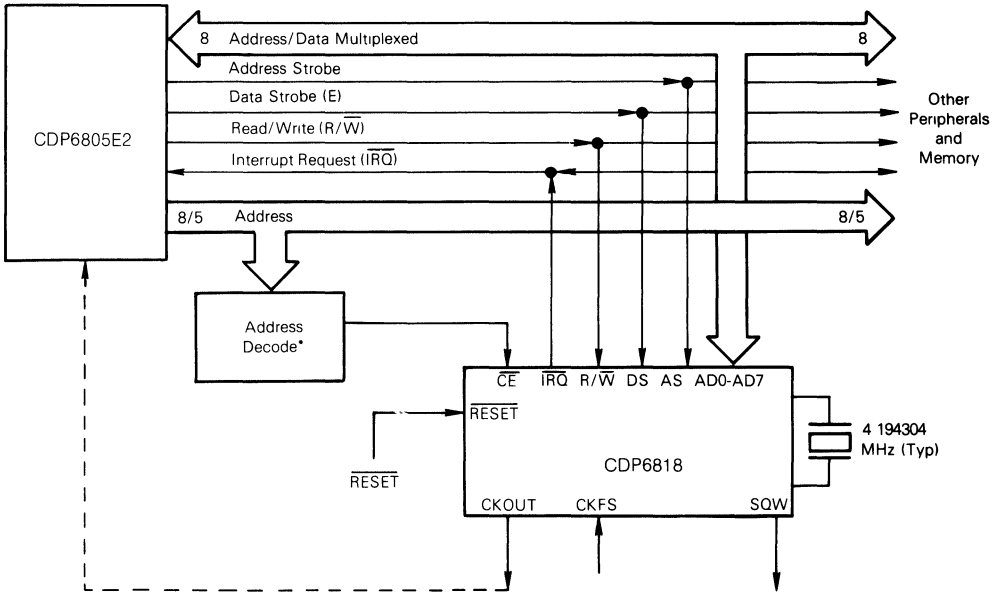
VRT – The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is low. The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read/only bit which is not modified by the $\overline{\text{RESET}}$ pin. The VRT bit can only be set by reading Register D.

b6 TO b0 – The remaining bits of Register D are unused. They cannot be written, but are always read as "0's."

TYPICAL INTERFACING

The CDP6818 is best suited for use with microprocessors which generate an address-then-data multiplexed bus. Figures 17 and 18 show typical interfaces to bus-compatible processors. These interfaces assume that the address decoding can be done quickly. However, if standard metal-gate CMOS gates are used the $\overline{\text{CE}}$ setup time may be violated. Figure 19 illustrates an alternative method of chip selection which will accommodate such slower decoding.

The CDP6818 can be interfaced to single-chip microcomputers (MCU) by using eleven port lines as shown in Figure 20. Non-multiplexed bus microprocessors can be interfaced with additional support.



*QMOS decoder

Fig. 17 — CDP6818 interfaced to CDP6805E2 compatible multiplexed bus microprocessors.

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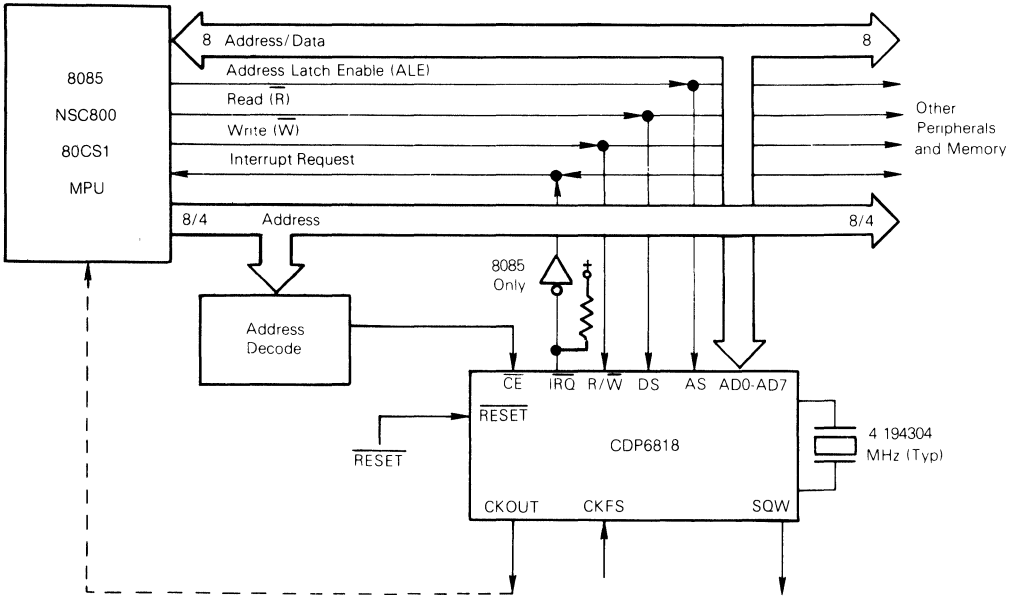

Fig. 18 — CDP6818 interfaced to competitor compatible multiplexed bus microprocessors

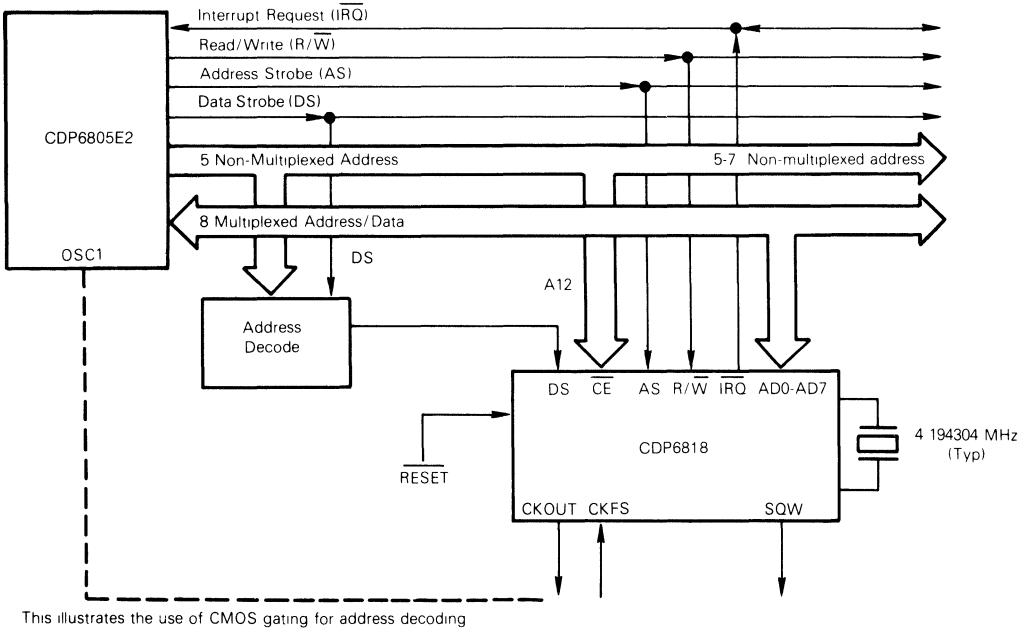

Fig. 19 — CDP6818 interface to CDP6805E2 CMOS multiplexed microprocessor with slow address decoding

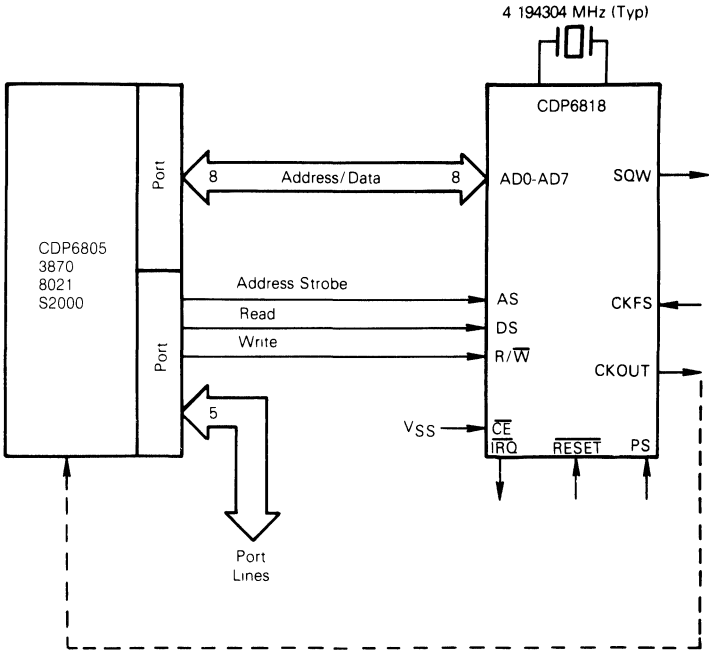

Fig. 20 — CDP6818 interfaced with the ports of a typical single-chip microcomputer.

There is one method of using the multiplexed bus CDP6818 with non-multiplexed bus processors The interface uses available bus control signals to multiplex the address and data bus together

An example using either the 6800, 6802, 6808, or 6809 microprocessor is shown in Figure 21

Figure 22 illustrates the subroutines which may be used for data transfers in a non-multiplexed system The subroutines should be entered with the registers containing the following data

Accumulator A The address of the RTC to be accessed.
Accumulator B Write The data to be written
Read. The data read from the RTC

The RTC is mapped to two consecutive memory locations RTC and RTC + 1 as shown in Figure 21

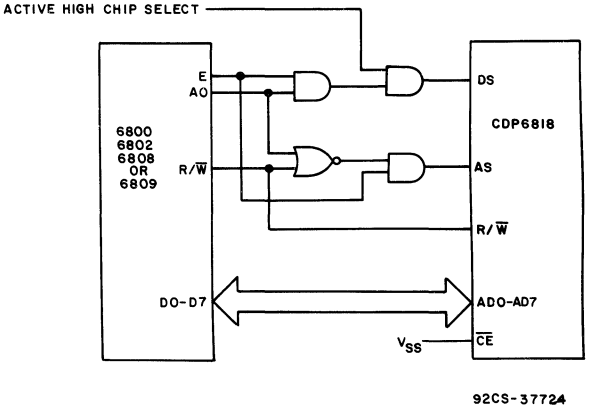

Fig. 21 — CDP6818 interfaced with Motorola type processors

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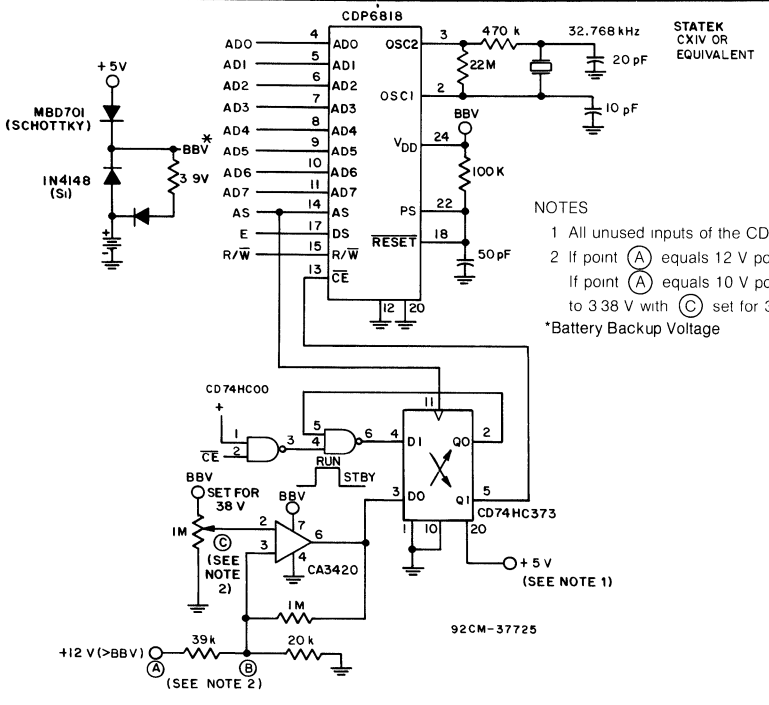
FIGURE 22 — SUBROUTINE FOR READING AND WRITING THE CDP6818 WITH A NON-MULTIPLEXED BUS

```
READ    STA   RTC     Generate AS and Latch Data from ACCA
        LDAB  RTC+1   Generate DS and Get Data
        RTS
WRITE   STA   RTC     Generate AS and Latch Data from ACCA
        STAB  RTC+1   Generate DS and Store Data
        RTS
```

IMPORTANT APPLICATION NOTICE

The CDP6818 with a bottom brand code of 6RR requires a synchronization of the $\overline{CE}$ pin with address strobe The following circuit will satisfy that condition and also shows a typical application of power down circuitry If $\overline{CE}$ is grounded at all times (no power down required) the following circuit need not be used



NOTES

1 All unused inputs of the CD74HC373 must be grounded

2 If point (A) equals 12 V point (B) should be equal to 4 06 V If point (A) equals 10 V point (B) should be equal to 3 38 V with (C) set for 3 18 V

*Battery Backup Voltage

Fig 23 — Typical Application Circuit