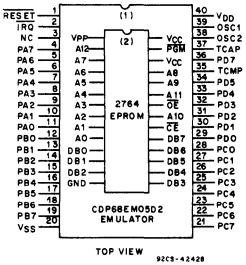
Product Preview

CDP68EM05D2

TERMINAL ASSIGNMENT



40-Lead Piggyback Package

CMOS High-Performance Silicon-Gate 8-Bit Microcomputer Piggyback Emulator

Features:

- *All CDP68HC05D2 hardware and software features*
- *Un-multiplexed external address, data, and READ control lines*
- *Full 8K byte address space available (8064 bytes available externally)*
- *96 bytes of on-chip RAM, no ROM*
- *Direct interface to industry standard EPROMs*
- *40-lead piggyback package (1) with 28-hole socket for 2764 EPROM (2)*

The CDP68EM05D2 Emulator device, a functional equivalent to the CDP68HC05D2 microcomputer, is designed to permit prototype development and preproduction of systems for mask-programmed applications. Data and address bus, as well as control signals are externally available.

In addition to this feature, the CDP68EM05D2 Emulator differs from the CDP68HC05D2 in the following ways:

1) Memory locations which are occupied by ROM on the CDP68HC05D2 are accessed as external locations with the CDP68EM05D2 Emulator intended to interface to a programmable ROM.

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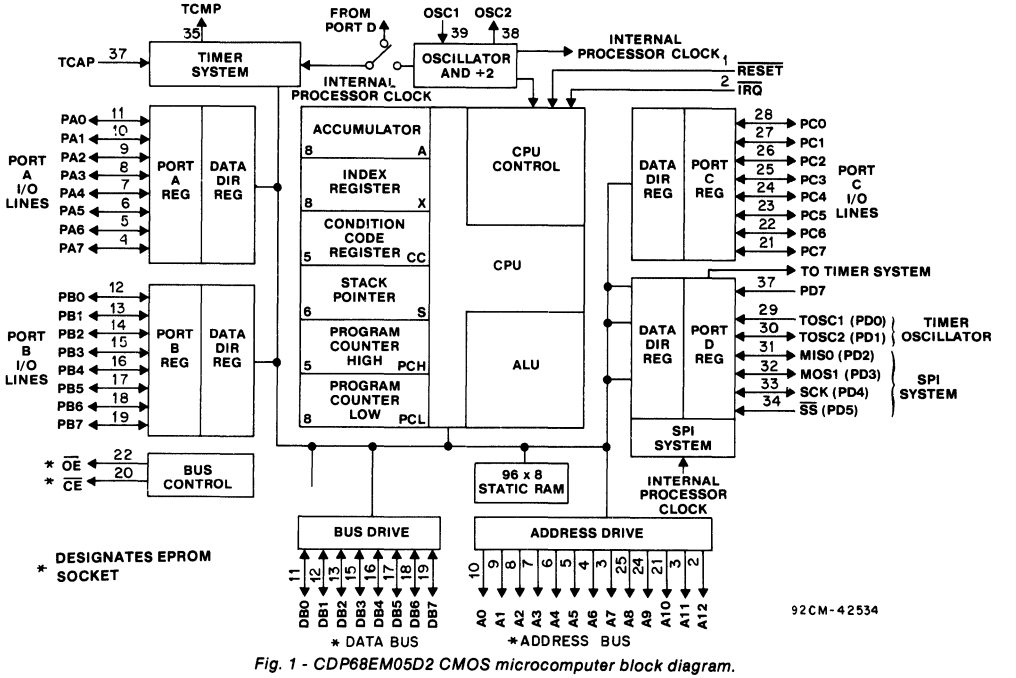

Fig. 1 - CDP68EM05D2 CMOS microcomputer block diagram.

File Number **1960**

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2) Mask-programmable options (CPU oscillator type and external interrupt sense) are fixed in hardware. Only one version of these options is available in the emulator. These are:
   a) CPU oscillator = crystal or ceramic resonator.
   b) External interrupt request = negative edge and level sensitive.
   c) Start-up delay for power-on RESET or exit from STOP mode = 4064 cycles.

Memory

The CDP68EM05D2 Emulator has a total address space of 8192 bytes. The CDP68EM05D2 Emulator has implemented 208 bytes of the address locations for I/O and internal RAM. The remainder is available for external memory. The first 256 bytes of memory (page zero) is comprised of the I/O port locations, timer locations, 48 bytes of external address space and 176 bytes of RAM. The next 7936 bytes are available to address external memory. The address map is shown in figure 2. The functions of the internally addressable peripherals can be found in the CDP68HC05D2 data sheet, File No. TSM-204.

Functional Pin Description

The following list includes only those additional pins that differ in function from those on the CDP68HC05D2 microcomputer. See the CDP68HC05D2 data sheet, File No. TSM-204, for the remaining pins which are common.

A0-A12 -Address lines 0 through 12.

DB0-BD7 -Bidirectional 8-bit non-multiplexed data bus with TTL inputs.

$\overline{OE}$ -Output Enable: An output signal used for selecting external memory space. A low level indicates when external ROM is being accessed. The Output Enable signal will not go true, however, when addressing the 10 unused locations in the 32 bytes of the I/O space even though the address lines will be valid.

$\overline{CE}$ -Chip Enable: A status output which indicates direction of data flow with respect to external or internal memory space). A read of internal memory or I/O will place data on the external data bus. When addressing external memory, this signal in conjunction with $\overline{OE}$, will enable a READ access from a piggyback EPROM.

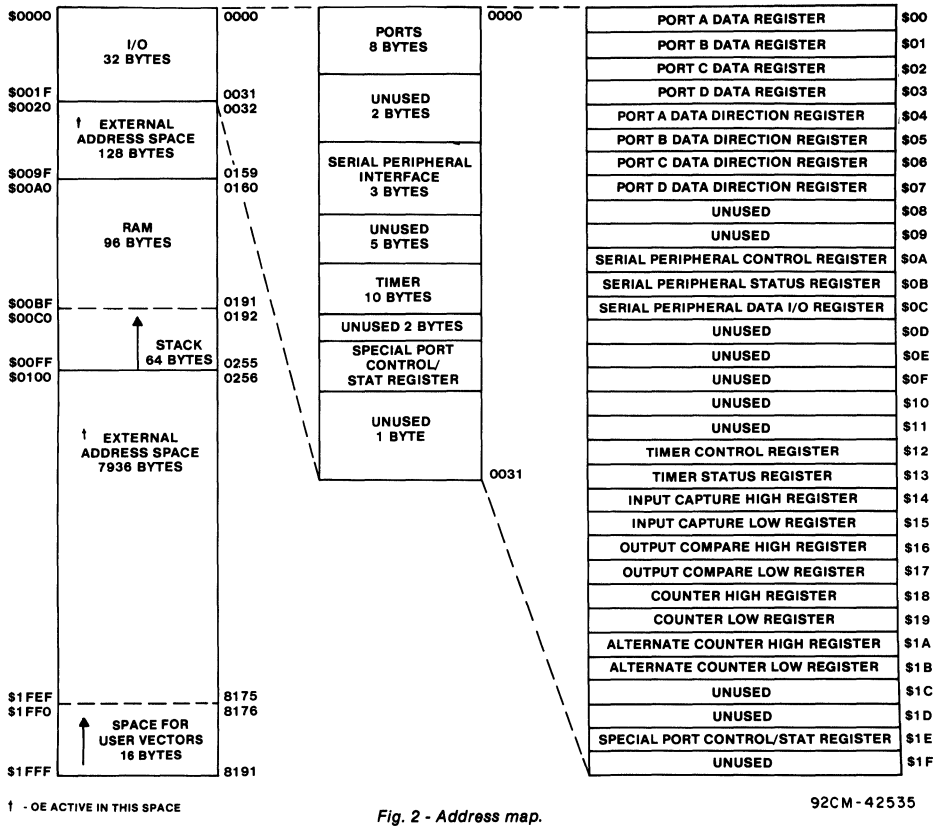

Fig. 2 - Address map.

$\overline{IRQ}$ (Maskable Interrupt Request)

Interrupt input which is negative edge and level sensitive. Either type of input to the $\overline{IRQ}$ pin will produce the interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the $\overline{IRQ}$ pin goes low for at least one t_{ILIH} as defined in the CDP68HC05D2 data sheet, a logic one is latched internally to signify that an interrupt has been requested. When the MCU completes it's current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence. The $\overline{IRQ}$ input requires an external resistor to V_{DD} for "wire-OR" operation.

OSC1, OSC2

A NAND gate is connected between these two pads (OSC2 = output) for use as a crystal or ceramic resonator oscillator with a STOP clock mode. The internal clocks are derived by a divide-by-2 of the internal oscillator frequency (f_{osc}). Alternatively, an external clock may be used by applying the external clock signal to the OSC1 input with the OSC2 input not connected.

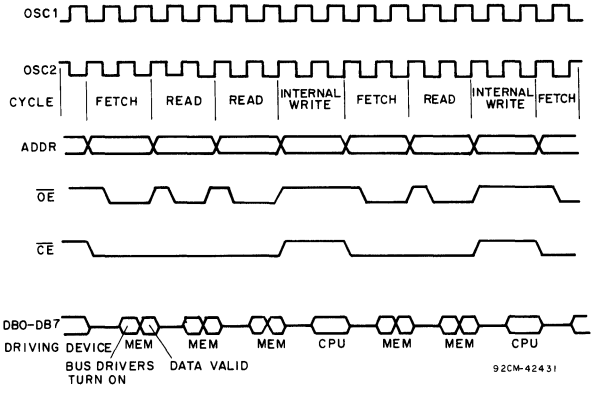

Fig. 3 - Typical cycle timing for the CDP68EM05D2 emulator.

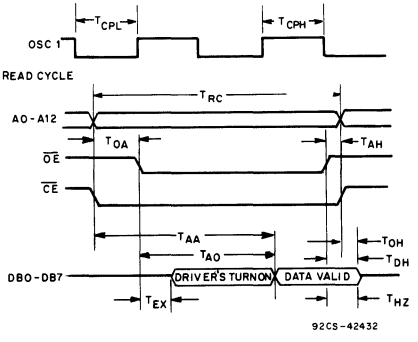

Fig. 4 - Control timing diagram for the CDP68EM05D2 emulator.

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CDP68EM05D2 EMULATION CHIP READ CYCLE TIMING OBJECTIVE SPECIFICATIONS:
V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 25°C

PARAMETER		LIMITS		UNITS
		MIN.	MAX.	
External Input Oscillator Pulse Width, Low or High	T_{CPL},T_{CPH}	90	—	ns
Read Cycle	TRC(P)	476	—	
Address Before $\overline{OE}$	TOA(P)	50	—	
Access Time From $\overline{OE}$	TAO(M)	—	200	
Access Time From Stable Address	TAA(M)	—	350	
Access Time From $\overline{CE}$	TAA(M)	—	350	
Data Bus Driven From $\overline{OE}$	TEX(M)	0	—	
Address Hold Time After $\overline{OE}$	TAH(P)	0	—	
Data Hold Time After Address	TOH(M)	0	—	
Data Hold Time After $\overline{OE}$	TDH(M)	0	—	
$\overline{OE}$ High to Data Bus Not Driven	THZ(M)	0	60	

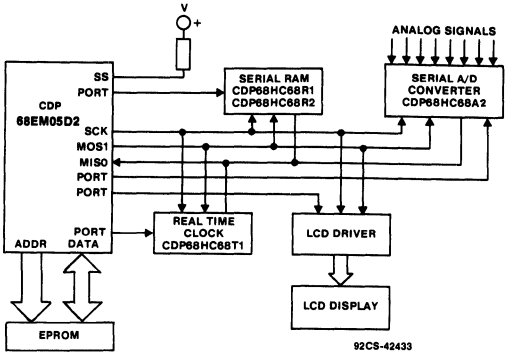

Fig. 5 - Emulation with the serial peripheral interface (SPI) bus system.

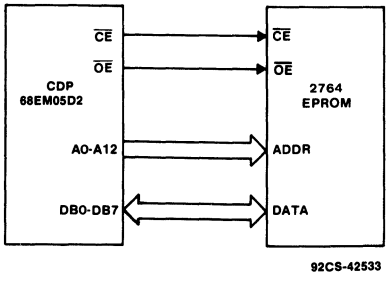

Fig. 6 - CDP68EM05D2 emulator interfaced with 2764 EPROM.

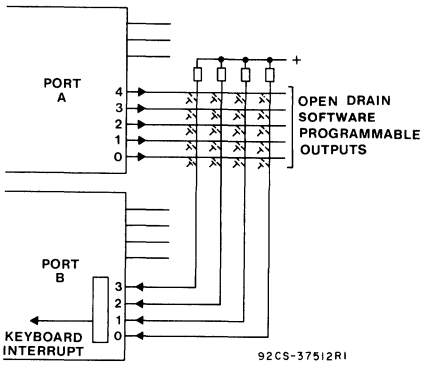

Fig. 7 - Keyboard interface to illustrate use of Open Drain Output Port.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} — V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD}, V_{CC} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.