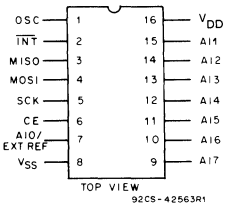
Advance Information

CDP68HC68A2



TERMINAL ASSIGNMENT

CMOS Serial 10-Bit A/D Converter

Features:

- *10-bit resolution*
- *8-bit mode for single data byte transfers*
- *SPI (Serial Peripheral Interface) compatible*
- *Operates ratiometrically referencing V_{DD} or an external source*
- *14 µs 10-bit conversion time*
- *8 multiplexed analog input channels*
- *Independent channel select*
- *Three modes of operation*
- *On chip oscillator*
- *Low power CMOS circuitry*
- *Intrinsic sample and hold*
- *16-lead dual-in-line plastic package*
- *20-lead dual-in-line small-outline plastic package*

The CDP68HC68A2 is a CMOS 8- or 10-bit successive approximation analog to digital converter (A/D) with a standard RCA/Motorola Serial Peripheral Interface (SPI) bus and eight multiplexed analog inputs Voltage referencing is obtained from either the V_{DD} pin or an external precision reference for the sacrifice of one channel when enabled. The operating range of the converter includes the entire V_{DD} to V_{SS} voltage range for each of the eight inputs.

The CDP68HC68A2 implements a switched capacitor, successive approximation A/D conversion technique which provides an inherent sample-and-hold function. An on-chip Schmitt oscillator provides the internal timing of the A/D converter It can be driven by an external oscillator or system clock in the external mode, or can be connected to a single external capacitor to provide an independent clock in the internal mode. The minimum 10-bit conversion time per input is 14-microseconds/channel. Each conversion in the 10-bit mode requires 14 oscillator clock pulses where 12 are required in the 8-bit mode allowing a 12-microsecond/-channel conversion time

A unique feature of the CDP68HC68A2 allows any combination of the eight input channels to be selected and converted in ascending channel order in any one of three modes. The mode selection enables single, multiple or continuous channel conversion operation. The device has three READ/WRITE registers which are used to select the mode of operation, input channels, and starting address. The 10-bit conversion data is stored (right justified) in two 8-bit bytes. The most significant byte contains two status bits which may be monitored by the microcomputer. An 8-bit mode is available which performs a faster eight bit

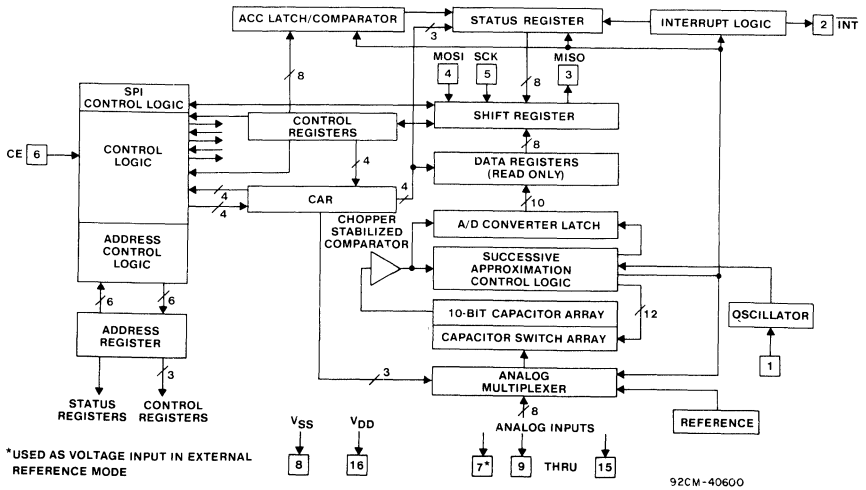


Fig. 1 - Block diagram of the CDP68HC68A2.

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CDP68HC68A2

conversion and stores the data in a single eight bit byte. In the 10-bit mode, all 16 data bytes are addressable and in the 8-bit mode only the eight bit data byte is accessible in each of eight data bytes. A READ only STATUS register is available to monitor the status of the Conversion and the current channel address. This register can be used for system polling or the $\overline{INT}$ pin can be used for interrupt driven communications.

The CDP68HC68A2 is available in a 16-lead dual-in-line plastic package (E suffix) and in a 20-lead dual-in-line small-outline plastic package (M suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -40° C to +70° C (PACKAGE TYPE M) * ..... 400 mW
For T_A = -70° C to +85° C (PACKAGE TYPE M) * ..... Derate Linearly at 6.0 mW/° C to 310 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 40 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E and M ..... -40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

OPERATING CONDITIONS at T_A = -40° to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
DC Operating Voltage Range	3	6	V

Pin Descriptions

OSC (1) — Oscillator Input

A Schmitt input which provides the timing for the A/D conversion. The mode of this pin is selected in the Mode Select Register (MSR) and is either internal or external clocking. In the internal mode, a capacitor is externally connected to this pin causing the Schmitt input gate to oscillate at a frequency inversely proportional to the capacitance. In the external mode, the input may be driven directly by an external oscillator or system clock.

$\overline{INT}$ (2) — Active Low Interrupt Output

This output is driven from a single NFET pulldown transistor. A bit in the MSR enables or disables the $\overline{INT}$ output. The output is driven to a logical LOW state while enabled and activated, otherwise it will remain in a tri-state condition. The $\overline{INT}$ output function is only deactivated upon addressing the Status Register. The tri-state function can be advantageous to wire NAND interrupts while a pullup resistor can be used to drive the output to the logical HIGH state while inactive. The interrupt function cannot be enabled in mode 3.

MISO (3) — Master-In-Slave-Out Output

Data is serially shifted out at this pin Most Significant Bit first.

MOSI (4) — Master-Out-Slave-In Input

Data is serially shifted in on this pin Most Significant Bit first.

SCK (5) — Serial Clock Input

Provides the timing for the synchronous SPI interface circuitry.

CE (6) — Chip Enable Input

An active HIGH device enable. The CDP68HC68A2 must be enabled preceding SPI communications. While deactivated, the SPI logic is placed in a RESET state and the MISO line is tristated from driving the SPI bus synchronous with SCK.

AIn (7, 9-15) — Analog Inputs

These are the eight analog input channels which are multiplexed to the internal A/D converter. Each channel is selected by a corresponding bit in the Channel Select Register (CSR). When the VR bit in the MSR is enabled, the device is in the external voltage referencing mode and channel A0 (pin 7) is used as a full scale reference input.

V_{SS} (8) — Negative Power Supply

This pin is connected to the ground and establishes the negative reference to the analog inputs.

V_{DD} (16) — Positive Power Supply

This pin establishes the full-scale voltage range of the A/D converter when operating ratiometrically in the internal reference mode.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V, except as noted.

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
ACCURACY					
Differential Linearity Error	10-Bit Mode		±1.25	±2	LSB
Integral Linear Error	10-Bit Mode		±1.25	±2	LSB
Offset Error	10-Bit Mode	-1	3	4	LSB
Gain Error	10-Bit Mode	-1	1	2	LSB
ANALOG INPUTS: A10 THRU A17					
Input Resistance	In Series With Sample Caps		85		Ohms
Sample Capacitance	During Sample State		400		pF
Input Capacitance	During Hold State		20		pF
Input Current	@ V_{IN} = V_{REF}+ During Sample		+30		μA
	During Hold or Standby State			±1	μA
Input + Full Scale Range		V_{SS}		V_{DD} +.3	V
Input Bandwidth (3 dB)	From Input RC Time Constant		4.68		MHz
DIGITAL INPUTS: MOSI, SCK, CE T_A = -40°C to +85°C					
High Input Voltage V_{IH}	Over V_{DD} = 3 to 6 V	70			% of V_{DD}
Low Input Voltage V_{IL}	Over V_{DD} = 3 to 6 V			30	% of V_{DD}
Input Leakage				±1	μA
Input Capacitance	Room Temperature			10	pF
DIGITAL OUTPUTS: MISO, $\overline{INT}$ T_A = -40°C to +85°C					
High Level Output V_{OH}, MISO	I_{SOURCE} = 6 mA	4.25			V
Low Level Output V_{OL}, MISO, $\overline{INT}$	I_{SINK} = 6 mA			0.4	V
3-State Output Leakage I_{OUT}, MISO, $\overline{INT}$				±10	μA
TIMING PARAMETERS T_A = -40°C to +85°C					
Oscillator Frequency, f_{sample}	10-Bit Mode			1	MHz
Conversion Time (Including Sample Time)	10-Bit Mode	14 Oscillator Cycles			
	8-Bit Mode	12 Oscillator Cycles			
Sample Time (Pre-Encode)	8 Time Constants (8τ) Required	First 1.5 Oscillator ≥ 8τ			
Serial Clock (SCK) Frequency				1.5	MHz
SCK Pulse Width, T_P	Either SCK_a or SCK_b	150			ns
MOSI Setup Time, T_{DSU}	Prior to Leading Edge of T_P	60			ns
MOSI Hold Time, T_{DH}	After Leading Edge of T_P	60			ns
MISO Rise & Fall Time	200 pF Load			100	ns
MISO Propagation Delay, T_{DOD}	From Trailing SCK Edge			100	ns
I_{DD}	V_{DD} = 5 Volts, Continuous Operation		1.4	2	mA

4

CDP68HC68A2

Serial Data Format, Device Communication and Operation

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1. Overview

To operate the CDP68HC68A2 A/D, it is required to access the control registers and program them for desired operation. This is performed serially over the SPI bus in a two phase sequence, each phase contains a minimum of one SPI transfer cycle. In phase I, the microcontrolling device sends an ADDRESS/CONTROL WRITE byte to initialize a register operation. This is followed by phase II, the REGISTER DATA ACCESS, which allows single or multiple byte READ or WRITE transfers depending on the state of the Chip Enable (CE). The following sections describe this operation in detail to more effectively use this SPI peripheral device.

2. SPI Logic

The Serial Peripheral Interface (SPI) on a peripheral device is used to communicate with a microcomputer, and was designed to meet timing specifications illustrated in figure 2. The bit order is MSB first and there are eight serial clock cycles to a SPI transfer cycle. A WRITE to the SPI peripheral is performed by generating data on the MOSI line synchronous to the SCK. A READ from the SPI peripheral requires a WRITE to be performed just to cycle the SCK input eight times, sometimes referred to as a 'DUMMY WRITE'. This is due to the full duplex nature of this SPI peripheral.

In the case of CDP6805 Microcontrollers, the Serial Clock Phase (CPHA) needs to be set to a logical HIGH, where a transition occurs before a strobe for valid data. As for the Serial Clock Polarity (CPOL) either (SCKa or SCKb) will be accepted, as the state of SCK is determined at the transition of Chip Enable (CE). The appropriate internal polarity of SCK is selected and maintained for the duration of the SPI transfer cycle (till CE is deasserted).

3. Addressing Modes

Following the initial ADDRESS/CONTROL WRITE transfer of phase I, there are two modes available to accessing registers during phase II. These are single byte transfers and multiple byte or burst type transfers. The more applicable method should be apparent based on system objectives. For example, where minimum communication overhead is a consideration, burst mode is used wherever possible.

Single byte transfers address a single register and perform a REGISTER DATA ACCESS to or from that register. Burst transfers are used to access one register followed by accesses to or from registers in ascending consecutive order. These accesses, will be READ or WRITE operations but not both. Single byte transfers are usually made where just one register need be accessed, in general, where burst transfers are not possible due to the addressing order or if accesses mix READ and WRITE operations. Single byte transfers access one register and require exactly two SPI transfers. Burst transfers access N registers and require N+1 SPI transfers.

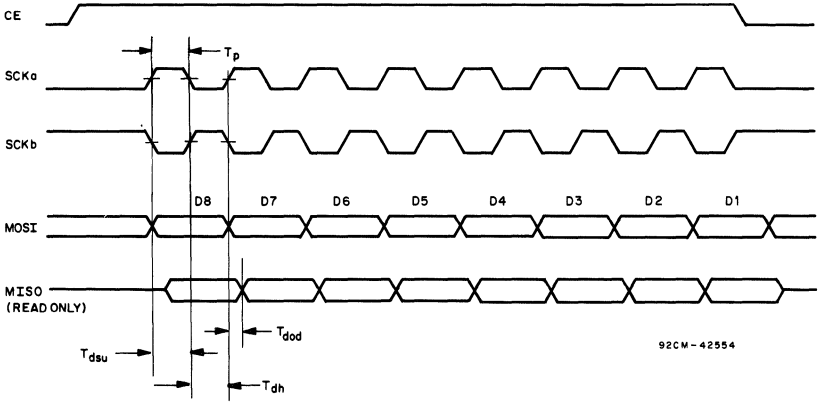
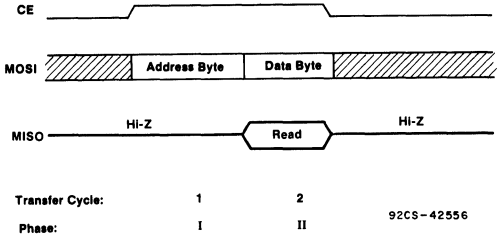


Fig. 2 - Timing diagram for serial peripheral interface.

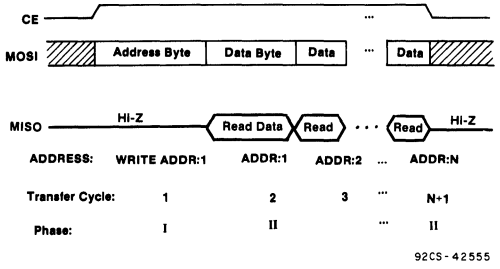
3.1 Device Addressing

To address the A/D registers internally, the A/D device first needs to be addressed externally by the microcontroller activating the Chip Enable of the A/D. After activating CE the A/D device awaits SPI transfer cycles for phase I, followed by phase II, see figure 3a and b for timing of the Single Byte or Burst Modes of communication. Refer to Note 1 for CE.

MISO always Hi Impedance during Phase I, Phase II WRITE operations and when CE is inactive. Phase II READ operations will have valid READ Data on the MISO.



(a) *Single byte transfer.*
(Requires 2 SPI transfers)



(b) *Multiple (N) byte transfer.*
(Efficient device communication requiring N+1 SPI transfers)

Fig. 3 - Timing diagrams for (a) single byte transfer and (b) multiple (N) byte transfer.

During the (N+1) 'th Burst Mode Transfer, the address transferred will be N and is advanced internally to N+1 at the completion of that cycle. For example, if the initial address was 00 and N was desired to be 06, the address accessed in the 7th burst mode transfer will be address 06, yet internally the address will point to address 07 after transferring the contents of 06, see section 3.1.1 for details on the ADDRESS/CONTROL WRITE. The previous example applies to Control, Status and selected consecutive Data Registers. It does not apply to Data Registers which are not selected since they are skipped entirely, or not consecutive since the address is advanced more than an increment until the next selected channel is addressed, see Note 5 on Data Registers in Register allocation map, appendix, section 5.3.

3.1.1 ADDRESS/CONTROL WRITE (Phase I)

The ADDRESS/CONTROL WRITE phase is a dual purpose WRITE only operation that performs register addressing and READ/WRITE control. Phase I is invoked by the first SPI Transfer at the onset of activated CE. Both address and control are performed using eight bits, refer to figure 4 for bit descriptions. One of these bits (MSB) is used to designate READ or WRITE Phase II operations to follow. The remaining seven bits are used to designate a register address of which the following READ or WRITE operation is to be performed upon, see address map in appendix, section 5.3 for register allocation. To follow are details on bit descriptions.

BIT SIGNIFICANCE, most to least from left to right:

$\overline{R}$/W	0	0	A4	A3	A2	A1	A0

Fig. 4 - Address/Control write byte.

$\overline{R}$/W ($\overline{READ}$/WRITE)

This bit is used to control the data direction during the following SPI REGISTER DATA ACCESS (Phase II cycles). The bit is logically set HIGH or cleared LOW to initiate one or more REGISTER DATA ACCESS - WRITE or READ operations respectively. Either mode, once designated, will be maintained until CE is deactivated and a new ADDRESS/CONTROL WRITE (Phase I) is invoked.

UNUSED

The two unused bits must be cleared to the logical LOW state to address any of the internal registers of the CDP68HC68A2.

An:

The five ADDRESS bits A4-A0 are used to address the registers in accordance with the address allocation table of appendix, section 5.3. When addressing READ only Data Registers it should be noted that when in 10-bit mode, the A0 addresses the MOST/LEAST SIGNIFICANT DATA REGISTER bytes when logically LOW and HIGH respectively. In the 8-bit mode the data register bytes are LOW byte only (Since there is no HIGH byte A0 is a 'don't care').

3.1.2 REGISTER DATA ACCESS (Phase II)

The ADDRESS/CONTROL WRITE in Phase I (one SPI transfer cycle) is followed by REGISTER DATA ACCESS during Phase II of the SPI transfers. This operation is either a READ or a WRITE depending on the operation previously designated by the ADDRESS/CONTROL WRITE byte. CE determines whether Phase II is to be a Single Byte or Burst transfer and when transfers terminate, see Note 1.

If CE is active for just one Phase II SPI transfer, it will only be a Single Byte transfer; however, if it remains asserted after the first Phase II SPI transfer, multiple byte transfers will proceed to occur. This is the Burst Mode. While in this mode, the address written in Phase I is incremented automatically at the completion of each register access. The CONTROL and STATUS Registers are accessed directly, and advanced by single address increments. Data Registers are advanced to the NEXT selected channel in the CSR. See Note 5 for limitations of Data and Control/Status accesses.

4. Control and Status Registers

There are three $\overline{READ}$/WRITE control registers and one READ only STATUS Register in the CDP68HC68A2. They are described in detail here and shown in the register allocation table in appendix section 5.3.

4.1 Mode Select Register (MSR)

ADDRESS: ($\overline{R}$/W)0001000	X	X	$\overline{EXT}$	VR	M8	IE	M1	M0

This READ/WRITE register is used to select the mode of operation as well as various functions of the device. Data is maintained in this register until new data is written, initially powers up with all bits cleared to logical zero. A WRITE to the MSR will clear the $\overline{INT}$ output and all STATUS bits.

CDP68HC68A2

Individual bits are described here:

TWO X BITS

Are "don't care" bits and can be in any state.

$\overline{\text{EXT}}$ (External Oscillator)

This bit selects the internal oscillator with a logical HIGH, or a logical LOW selects the external clock on pin 1.

VR (Voltage Reference)

This control bit is used to determine the voltage reference source of the A/D converter. A logical HIGH in this bit selects pin 7 (AI0) as the external reference input. A logical LOW in this bit establishes the V_{DD} voltage level as the reference for ratiometric operation.

M8 (Eight Bit Mode)

This bit selects either the 10-bit or 8-bit mode of operation. A logical LOW in this bit enables the 10-bit mode, while a logical HIGH enables the 8-bit mode.

IE (Interrupt Enable)

This control bit is used to enable or disable the $\overline{\text{INT}}$ output function. A logical HIGH in this bit enables the $\overline{\text{INT}}$ output function when operating in either modes 1 and 2. A logical low in this bit disables $\overline{\text{INT}}$ output function, maintaining pin 2 to a tristate condition. The status bits in the DATA and STATUS registers are not affected by the state of the IE control bit.

M1, M0 (Mode Select)

These two bits are set to select the mode of operation of the A/D converter. These modes are tabulated:

MODE SELECT

M1	M0	Mode	Function
0	0	0	IDLE
0	1	1	SINGLE CONVERSION
1	0	2	SINGLE SCANNING CONVERSION
1	1	3	CONTINUOUS SCANNING CONVERSION

4.2 Conversion Mode Descriptions

Operating the CDP68HC68A2 in these modes is generally performed by a WRITE sequence to the Mode Select Register (MSR), Channel Select Register (CSR) and Starting Address Register (SAR) with the desired Starting Channel Address. This is most efficient in the Burst Transfer mode, see appendix, section 5.3.2.1 dedicated to this topic. Conversions are invoked, following a WRITE to the SAR, on the addressed channel in the Channel Address Register (CAR).

4.2.1 IDLE

In this mode the internal A/D oscillator is disabled. Data is maintained from previous conversions in the STATUS and DATA registers and may be accessed. The IDLE mode can be invoked by a single (two Phase) WRITE to the MSR. If it is desired to access the control registers they should be written to in a burst sequence to set the Mode, and the SAR, and clear any status bits that may be set, see appendix, section 5.3.2.1.

4.2.2 SINGLE CONVERSION

Upon completion of any single conversion in mode 1, all status bits are set and the $\overline{\text{INT}}$ output activated (if enabled) and the converter interrupts awaiting a Data Register Access. The corresponding Data Register may then be read. In both 8- and 10-bit modes, this mode of operation will continue until a new command is issued by a WRITE to the MSR, CSR or conversions are aborted.

The first conversion will occur on the analog channel and digital address in the CAR after the SAR WRITE with the ENC bit set. Following conversions will be determined by selected channels and the Data Register access sequence controlling the CAR. After initially invoking this mode, the STATUS should be polled or hardware interruption can be used to wait for conversion completion before issueing a data retrieve sequence. Data conversions can be interleaved with Data Register READS along with the wait requirement. If hardware interrupts are dedicated to this process, conversions can be made and Data retrieved, all while maintaining CE active.

In the 8-bit mode there is only one Data Register byte associated with each channel; thus the channel address is automatically incremented after reading that register to the next selected, sequential channel and the next conversion initiated.

In the 10-bit mode, upon completion of reading the Most Significant Byte (MSB) of the appropriate channel address, the Channel Address is automatically incremented to the Least Significant Byte (LSB) at which time a conversion is initiated on the next selected channel. Reading the LSB Data Registers (invoking an automatic conversion) should be performed in the sequence: first the MSB then the LSB.

The Channel sequence is important in 8- or 10-bit modes in the burst mode, see Note 5. When in the Single Transfer mode, care should be taken to address the sequence of represented Channel Addresses, in the order which selected channels were converted. Since conversions occur after a READ of the previous channel converted, the NEXT channel read should be the latest one converted, a conversion is invoked on the NEXT selected channel when finished reading the current one.

An example, WRITE three control registers with SAR = 90 for ENC, SAE, with a CAR = 000 for channel zero, CSR must have CS0 = 1. After retrieving channel zero data, if CS1 = 0 (deselected) and CS2 = 1 (selected) (for instance CSR = FD), simply by waiting for the status INT bit to set (should read: 84 assuming that other channels are selected ACC will be clear) followed by writing address 04 will access the channel two data just converted.

4.2.3 SINGLE SCANNING CONVERSION

In mode 2, the first conversion, determined by the contents of the internal CAR, is initiated as described in the SINGLE CONVERSION mode description. Upon completion of the first conversion in this mode there is no interrupt, the channel address is automatically advanced to the next selected channel and a conversion initiated. Conversions continue until all of the selected channels have been converted. At that time the DV (10-bit mode only), INT, ACC status bits are updated and the $\overline{INT}$ output activated if enabled.

If hardware interrupts are not desired, polling of either the ACC or INT bits in the STATUS REGISTER will ensure conversions are complete. Functional differences in these bits are times at which they are cleared: The INT bit is cleared on a READ of the STATUS Register while the ACC is cleared after access to the associated Data Register. After conversion completion, the data registers may then be read. This sequence should be performed in the Burst Mode for simplicity, this will ensure the data read is truly the next selected channel without calculation due to this automatic addressing feature. In this fashion, less total SPI transfer cycles are necessary. Burst mode is absolutely necessary in the 10-bit mode. See Note 4 on 10-bit Data Register READS. Be aware of Note 2 when reading back Data.

4.2.4 CONTINUOUS SCANNING

In mode 3 all of the selected channels are continuously converted in sequence, beginning with the channel addressed by the SAR. The INT status bit and $\overline{INT}$ output are not valid in this mode and remain in a reset state. The conversions are initiated with a WRITE to the SAR. This mode is useful to convert, on short notice, analog channels which have been sampling in the background before attempting to read back the digital data; although when retrieving data the conversions will stop.

When in mode 3, the converter will run free and when data is accessed it will abort the operation. Conversion termination can be performed manually before read back and can be any one of the abort conditions. Writing to the SAR with SAE and ENC bits cleared to a logical LOW level, will wait to allow a conversion in progress to complete before termination. The CIP bit will clear after the current conversion has been terminated. See other abort conditions in appendix, section 5.2. If a conversion is terminated on a channel other than the highest selected one in a frame, there is a chance that some higher channels may actually be from the previous sample frame. More control of data retrieval can be gotten from monitoring of the converter Status Register.

The ACC, CIP, and CAR status bits (all in the STATUS REGISTER) can be monitored to determine the status of the converter, see Note 3. These status bits can be accessed and tested by polling the STATUS REGISTER over the SPI bus, see STATUS REGISTER, section 4.5. After the first pass through a frame of channel conversions, the ACC bit will be set. If the ACC bit has not yet been set, then less than all selected channels will have been converted. Reading the Status Register does not affect the converter. This allows the CIP bit (or any STATUS Register bits) to be polled awaiting the last conversion completion, or upon any desired conditions as best for the application, the proper sequence can be executed for DATA REGISTER access.

After invoking the CONTINUOUS MODE then aborting, monitoring the STATUS register can also supplement mode 3 termination by indicating the first channel converted. The NEXT selected channel in the CSR, following the last conversion, can be observed in the CAR. This happens to be the first channel converted and can be sent back as the first Data Register address for Data retrieval. A test for minimum of one full frame converted is made by testing ACC to be set to a logical HIGH in the CONTINUOUS SCANNING MODE. Knowing that all channels have been converted at least once, allows one to deduce that valid sample data will be read back. The remaining channels can be recovered in the burst mode. This allows fast data retrieval with the earliest channel converted recovered first. Use the burst mode for proper 10-bit operation, see Note 4. Be aware of Note 2 when reading back any data.

4.3 Channel Select Register (CSR)

ADDRESS: ($\overline{R}$/W)0010001	C7	C6	C5	C4	C3	C2	C1	C0

This READ/WRITE register is used to select the analog input channels. Each of the Cn bits is used to select the corresponding analog input channels, AIn. If the Cn bit is set to a logical HIGH, the corresponding input channel is selected. A logical LOW in a Channel Select bit deselects that channel. Data is maintained in the CSR until new data is written to this register. It is recommended to write to the CSR and reset all status bits whenever invoking conversion operations preceding a write to the SAR. This ensures proper CAR loading if the previous sequence was altered. This can be done in the burst mode, see appendix, section 5.3.2.1.

4.4 Starting Address Register (SAR)

ADDRESS: ($\overline{R}$/W)0010010	ENC	X	X	SAE	CA2	CA1	CA0	$\overline{M}$/L

This READ/WRITE register is used to initiate as well as abort conversions and access the Channel Address Register (CAR). Individual bits are described here:

ENC (Enable Conversion)

This bit is used to enable an A/D conversion. If this bit is HIGH, an applicable conversion operation is initiated upon completion of the WRITE to the SAR. If the bit is set to a logical LOW, no conversion is initiated. If a conversion is in progress and the SAR is written to with the ENC and the SAE bit set to a logical LOW, the current conversion will complete and subsequent conversions are inhibited. Useful for continuous mode.

Two "Don't Care" Bits XX

Are just that and are ignored when writing to the SAR. When reading these bits, they will always be at a logical LOW level.

SAE (Starting Address Enable bit)

A HIGH in this bit will allow the contents of the CAR to be set to the address determined by the three Channel Address bits in the SAR. If the bit is at a logical LOW, the channel address bits are not transferred to the internal Channel Address Register (CAR) and the CAR is maintained by the

operation of the selected mode. After writing to the SAR once, this bit has no effect until written again; although it stays in the logical active HIGH state.

CAn (Write Binary Encoded Channel Address)

See appendix, section 5.1. These three bits, when written to, determine the new contents internal channel address register. It is usually loaded with the lowest selected channel, but may be loaded with another selected channel, causing that channel to be converted first; hence, the Starting Address Register or SAR, for which this register is named. Subsequent conversions will be performed on channels determined by the CSR. Reading the CAn bits will only indicate what was previously written to this register or if a Data Register access was made, it will be set to that channel address and can change as the Channel Address Increment logic causes the effect of writing to the CAR in the SAR.

$\overline{M}$/L (The MSByte/LSByte Bit)

This bit is used internally to address the MSB or LSB of 10-bit data registers. This is a READ/WRITE bit which can be set along with the CAR on an SAR WRITE or by addressing a Data Register. This bit can be read to request the current CAR byte order significance following a write to the SAR or a Data Register access when invoking 10-bit conversion (SAE and ENC bits set) or when in the 8-bit mode this bit functions but is not used.

4.5 Status Register

ADDRESS: 00010011

INT	ACC	CIP	0	CA2	CA1	CA0	0

This is a read only register used to monitor the status of the A/D converter. If the STATUS REGISTER is addressed in a read burst operation, the STATUS REGISTER remains selected as long as the CE is active, allowing continuous monitoring of the SPI I/O updates in a polling fashion. The internal Channel Address Register (CAR) is unaffected by reading the STATUS REGISTER; it is incremented in accordance with the mode and channels selected. The contents of the STATUS REGISTER are updated upon the completion of each conversion. If the status of the converter changes while the STATUS REGISTER is being read, the register is not updated until the completion of the read.

INT (Interrupt)

This status bit (active HIGH) provides an equivalent function as the $\overline{INT}$ pin (active LOW). The bit is set HIGH in modes 1 and 2 as described in the mode select register description. The INT bit is reset to a logical LOW by reading the STATUS REGISTER or writing to the MSR or CSR.

ACC (All Conversions Complete)

This Status bit indicates that conversions have been completed on all of the selected channels or a 'data frame'. The bit is set to logical HIGH when a data frame has been converted. It is reset to a logical LOW by reading any of the data registers or writing to either the MSR or CSR, and remains reset until a subsequent conversion is completed on a all selected channels. In 10-bit mode all DVn bits of selected channel Data Registers are active when this bit is active. It is unaffected by reading the STATUS REGISTER. Useful in modes 2 and 3. This bit will only set in mode 1 if conversions are invoked on all selected channels before there are any data register accesses.

CIP (Conversion In Progress)

This bit is set logically HIGH when a conversion is initiated and reset logically LOW upon completion of a conversion or by writing to either the MSR or CSR. It is unaffected by reading the STATUS REGISTER. Until termination, this bit will remain set in mode three while conversions are enabled.

CAn (Read-Only Channel Address)

These three binary encoded bits represent the current CAR. These address bits are set to the corresponding channel address after activating the internal auto-channel-increment logic. This happens at the end of each conversion and any time following a Register is accessed. Reading these bits while in the CONTINUOUS SCANNING mode will display the changing Channel Addresses of the converter. If the STATUS REGISTER is read while a conversion is initiated, the CAR is unaffected and the address bits are set to the new value upon completion of the read.

Two Zero Bits

These bits are always cleared to a logical LOW and do not function.

5. Appendix

To follow are various references from the preceeding Data Sheet:

5.1 Channel Address Register (CAR)

The channel address is stored and sequenced in the internal CAR. Although this register is not directly accessible, it can be written to by either the SAR or an access to a Data Register. It can be read through the STATUS REGISTER. The CAR has two purposes: it selects the appropriate analog input channel for the analog multiplexer and addresses the corresponding Data Register to be updated. It can be read to determine the $\overline{MOST}$/LEAST significant byte in the 10-bit mode. To follow is a table of channels of the CAR as seen in the STATUS Register and SAR.

Channel Map

CA2	CA1	CA0	Channel	Pin No.
0	0	0	0	7
0	0	1	1	15
0	1	0	2	14
0	1	1	3	13
1	0	0	4	12
1	0	1	5	11
1	1	0	6	10
1	1	1	7	9

5.1.1 SAR WRITE to the CAR

Writing to the CAR is possible by a direct WRITE to the SAR as noted above. If ENC is logically LOW and SAE is logically HIGH, the auto-increment logic will not be activated and the CAR will be loaded with the three bits of the SAR address and byte significance. This may be verified with a read of the STATUS REGISTER CAR set to the current value (not

incremented to the NEXT selected channel address.) If conversions are enabled increment logic will be activated depending on the mode of operation and a selected channel will be pointed to. A read of the SAR will only reflect the value of the last update written to the CAR through one of the two methods of a direct SAR WRITE or a Data Register Access. The $\overline{M}$/L bit in this register is updated and can be read to request byte order status in the 10-bit mode.

Since the Channel Address Register (CAR) is the internal Data Register sequencer and multiplexer, the value of the CAR will be affected by a Data Register read sequence. This is most important in modes two and three where conversions and Data Retrieval are in two distinct phases of their own both dependent on the inital value of the CAR. In fact, an access to any Data Register will be equivalent to a WRITE to the CAR through the SAR. A complete Data Register READ sequence constitutes reading all selected channels, in this case the CAR value will return to the initial address position. The Burst Transfer mode will automatically perform this on the N+1'th cycle of the readback sequence following N channels converted. This is done by Phase I addressing of the first converted channel followed by N Phase II transfer cycles. Refer to Note 2 concerning incomplete READ sequences.

5.1.2 STATUS Register and SAR READ from CAR

The STATUS REGISTER can be read at any time to determine the Channel Address Register contents. Following a WRITE to the SAR with the SAE bit set, the CAR will be loaded with the start channel address. The actual value observed in the STATUS Register will depend on the state of the auto-increment logic since it is current. The auto-increment function depends on the conversion mode and the operation performed following an SAR WRITE. For instance, if in mode 1, a conversion resulted from the SAR WRITE (ENC set), the channel converted first was the Start Address. The observed address will be the NEXT selected channel (simultaneously initiating a conversion on it) following the channel written in the SAR. In mode 2 the entire frame of data (all selected channels) will have been converted and the CAR will contain the Start Address again ready to repeat the cycle, the last channel is incremented to the next or start channel, see Note 5. The current Most Significant or Least Significant Byte status is contained in the $\overline{MOST}$/LEAST bit in the SAR for monitoring.

5.2 Abort Conditions

Several illegal operations initiated while a conversion is in progress will cause the current conversion to abort. The data contained in the Data Register corresponding to the current channel conversion may or may not be preserved. The DV and DOV Status bits must be examined to determine the data integrity. The following table lists the conditions which will cause a conversion to abort immediately.

1. WRITE to the MSR.
2. WRITE to the CSR.
3. WRITE to SAR with SAE and/or ENC set to a logical HIGH.
4. Attempt to access any Data Register through the MISO pin. For example, transmitting a valid Read/Data register address control byte.

The exception of the abort conditions, which allows completion of a current conversion in progress, can be excuted by a WRITE to the SAR with the SAE and the ENC bits cleared to a logical LOW.

5.3 Register Allocation Table

This section describes the address map for the internal registers in the CDP68HC68A2. Special instructions are mentioned here for reading data registers. The address maps are also depicted here for clarity.

CDP68HC68A2

5.3.1 READ-ONLY DATA REGISTER ALLOCATION TABLE

	ADDRESS							CHANNEL	
$\overline{R}$	0	0	A4	A3	A2	A1	A0	10-Bit Mode	8-Bit Mode
0	0	0	0	0	0	0	0	MSB - 0	0
0	0	0	0	0	0	0	1	LSB - 0	
0	0	0	0	0	0	1	0	MSB - 1	1
0	0	0	0	0	0	1	1	LSB - 1	
0	0	0	0	0	1	0	0	MSB - 2	2
0	0	0	0	0	1	0	1	LSB - 2	
0	0	0	0	0	1	1	0	MSB - 3	3
0	0	0	0	0	1	1	1	LSB - 3	
0	0	0	0	1	0	0	0	MSB - 4	4
0	0	0	0	1	0	0	1	LSB - 4	
0	0	0	0	1	0	1	0	MSB - 5	5
0	0	0	0	1	0	1	1	LSB - 5	
0	0	0	0	1	1	0	0	MSB - 6	6
0	0	0	0	1	1	0	1	LSB - 6	
0	0	0	0	1	1	1	0	MSB - 7	7
0	0	0	0	1	1	1	1	LSB - 7	

5.3.1.1 Data Register Access

After invoking conversions in any mode without hardware interrupts, deassertion of CE will be necessary to read the STATUS Register then again to address the Data Registers. Converted Digital Data is retrieved (and validated in 10-bit mode only) from the Data Registers. After a conversion is complete or terminated, the Starting Address (which should have been a selected channel) should be the first Data Register address read. The SAR can initially be set to any of the selected channels to affect the order in which the channel data is retrieved.

5.3.1.1.1 10-bit Mode

In the 10-bit mode, two data registers are associated with each analog input channel. Upon completion of the first conversion, the data is internally stored at the addresses designated by the CAR written in the SAR before converting. The most Significant Byte (MSB) contains the two status bits and the two most significant bits of the 10-bit A/D conversion data. The eight least significant data bits are stored in the Least Significant Byte (LSB). These sixteen registers are read only registers.

The following is the format of the Data Registers in the 10-bit Mode (refer to the register allocation table in appendix, section 5.3.1):

ADDRESS: 00000000(MSB)	DV0	DOV0	0	0	0	0	D9	D8
ADDRESS: 00000001(LSB)	D7	D6	D5	D4	D3	D2	D1	D0
. . .								
ADDRESS: 00001110(MSB)	DV7	DOV7	0	0	0	0	D9	D8
ADDRESS: 00001111(LSB)	D7	D6	D5	D4	D3	D2	D1	D0

The bits in these registers are described here in more detail:

DVn (Data Valid)

This status bit is used to determine the validity of the conversion stored in the data data register. The DV bit is set HIGH upon completion of an A/D conversion to the corresponding channel. The bit is reset to a logical LOW level when the register is read (see Note 4), or if the MSR, CSR, or SAR is written to. It is also possible for the DV bit to be reset if an abort condition arises while a register is being loaded.

Dn (Data bits)

These ten data bits represent the 10-bit conversion data for the corresponding input channel. The bits are stored (Right Justified) in the two, corresponding eight bit bytes upon completion of the conversion. The data is maintained in the register only until another conversion is completed.

DOVn (Data Overrun)

This status bit is set to a logical HIGH level upon completion of a data conversion to a channel already containing valid data which has not been read. It indicates whether or not the previous data has been overwritten. The bit is reset LOW by reading the register or performing a WRITE to the MSR, CSR or both.

5.3.1.1.2 8-bit Mode

In the 8-bit mode, an 8-bit conversion is performed on the selected channels and stored in the corresponding data register. The status bits associated with Data Registers in the 10-bit mode are not included in the 8-bit mode, thus the STATUS REGISTER must be monitored to determine the status of the conversions. Since the conversion data is stored in a single 8-bit byte in the 8-bit mode, the data for each channel can be obtained with a single read cycle, as compared to two read cycles required in the 10-bit mode. The $\overline{\text{MOST}}$/LEAST bit is a don't care when written to in the 8-bit mode. When reading the Data Registers in the burst mode, the address is automatically incremented to the next selected channel. The read sequence should be complete, see Note 2.

The following is the format of the Data Registers in the 8-bit Mode:

ADDRESS: 0000111X	D7	D6	D5	D4	D3	D2	D1	D0
. . .								
ADDRESS. 0000000X	D7	D6	D5	D4	D3	D2	D1	D0

The bits in these registers are described here in more detail:

Dn (Data bits)

These eight data bits represent the 8-bit conversion data for the corresponding input channel. The bits are stored in a single eight bit byte upon completion of the conversion. The data is maintained in the register only until another conversion is completed.

5.3.1.1.3 Data Recovery Examples

A general method of implementation for any mode, single transfer or burst transfer is to build external software counter routines in the microcontroller. This method can require more code for more sophisticated designs, but works well when multiple modes are used. In this manner, channel activity in the CDP68HC68A2 is reconstructed for the requesting of appropriate channels within the device.

For Mode 1, a STATUS Register polling routine can wait for proper completion, then yield the next address to be converted (channel in CAR) for anticipation of channel Data Register Address to follow.

A simple method in mode 2 is to load the SAR with the lowest enabled channel then retrieve data beginning with that same address. Continue Phase II implementing the burst mode anticipating the rest of the selected channels to follow. For example CSR = AA, SAR = 92 readback channels 1, 3, 5, 7 in the Burst Mode beginning with address 02 (Channel 1). Four channels are converted then read back. Counting the number of CSR bits can determine total number of channels to retrieve.

Another, more complicated mode 2 example follows: if converting channels 1, 3, 5, and 7 (SCR = AA), with SAR = 96. This starts conversions with channel 3. Upon completion, begin reading Data from Register address 06 (MSByte channel 3, possibly save CAn bits upon writing to the SAR) and retrieve channel 3 followed by 5, 7 then 1. On the readback in the burst mode the address logic is automatically incremented to the next selected channel.

5.3.2 CONTROL and READ ONLY STATUS REGISTER ALLOCATION

	ADDRESS							REGISTER	
R/W	0	0	A4	A3	A2	A1	A0		
0/1	0	0	1	0	0	0	0	MSR	MODE SELECT REGISTER
0/1	0	0	1	0	0	0	1	CSR	CHANNEL SELECT REGISTER
0/1	0	0	1	0	0	1	0	SAR	STARTING ADDRESS REGISTER
0	0	0	1	0	0	1	1	STATUS	STATUS REGISTER

5.3.2.1 Control and Status Register Burst Access

Control registers may be read or written to independently with Single Byte transfers, or sequentially with a Burst transfer. When WRITING to control registers for conversions, the initial address will be the MSR ($90) followed by SAR ($91) then the CAR ($92). Since they are ascending consecutive addresses, the WRITE Burst Mode can be used by addressing register $90 (Phase I) then perform three more SPI transfer cycles (Phase II) to get at the MSR, CSR and the SAR requiring four SPI cycles, If it were a read operation only, the address would change to ($10).

5.4 Analog Section

The purpose of this section is to familiarize the user with the analog interface circuitry necessary for proper operation as specified.

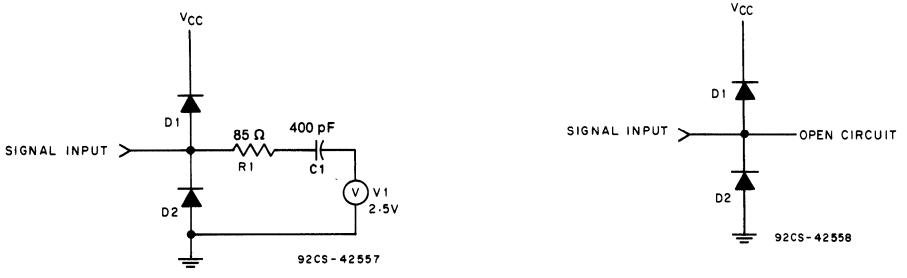
5.4.1 The Analog Input Mode

Shown here is a simplified equivalent circuit representing the input to the Analog to Digital Converter through the multiplexer as seen from each An pin.

Due to the nature of the switched capacitor array used for determination of the Digital Output Word, two important points are noted here:

1. A property of a capacitive input after sufficient charging (or discharging) has taken place, is the intrinsic sample and hold function, which is a feature in this case. This provides all that is necessary to accurately sample a point on an input waveform within the input bandwidth shown in the specifications, which is under 1.5 conversion oscillator cycles. If a resistor ladder A/D were used, an external sample and hold circuit would be required.
2. The input to the capacitor network appears as an RC network with a time constant and therefore places constraints on the source impedance. The charging time and therefore the accuracy of the conversion will be adversly affected by increasing the source impedance.

It is therefore recommended to set the conversion oscillator frequency in accordance with the input impedance in order to allow sufficient time (the 1.53 Tosc cycles) to sample a



(a) *During sample time.* (b) *During hold and idle time.*

Fig. 5 - Equivalent circuit for signal input (a) during sample time and (b) during hold and idle time.

changing waveform through the modeled input low pass filter network which includes the input source in a series circuit with the internal impedance. Combined, this is the effective impedance.

The time constant (τ) for the input network is $R_{eff}C_{net}$.

$R_{eff} = R_s + R_{net}$, $C_{net} = 400$ pF, and $R_{net} = 85\Omega$.

$\tau = R_{eff}C_{net} = (R_s + 85\Omega)$ 400 pF.

8τ is required during the first 1.5 sample clock cycles to sufficiently encode 10-bit conversion. Therefore, $1.5\,T_s \geq 8\tau$ and $T_s \geq 5.33\,R_{eff}C$.

$T_s = 1/f_{sample}$, then $f_{sample} \leq [5.33\,(R_s + 85\Omega)\,400\text{ pF}]^{-1}$, $f_{sample} \leq (4.688 \times 10^8)/(R_s + 85\Omega)$.

For example, $R_s = 1000\,f_{sample}$ must be less than 432 kHz.

$T_s = 2.3\,\mu$s, this yields a 10-bit conversion time of 32 μs. An internal $C_{osc} \geq 68$ pF, see chart.

The maximum frequency is limited by the device specification, see characteristics. Conversely, by limiting the (R_s) Series input resistance:

$R_s \leq [(4.688 \times 10^8)/f_{sample}] - 85\Omega$.

For example, for a 1 MHz sample clock R_s max = 385Ω. Consequently, the 10-bit conversion time is 14 T_s = 14 μs.

5.4.2 The Internal Schmitt Oscillator

Fig. 6 shows a simplified model of the Schmitt oscillator used to help familiarize the user with its operation. The following describes the characteristics of the internal oscillator frequency versus capacitance at 5 volts and 25° C

C (pF)	f (MHz)	C (pF)	f (MHz)
18.7	1.07	218.7	0.148
38.7	0.656	318.7	0.111
48.7	0.545	409.7	0.107
68.7	0.387	528.7	0.072
118.7	0.261	1018.7	0.040

Always remember, when measuring the oscillator, probe capacitance will affect frequency. An alternative to direct frequency measurement of the oscillator input is to measure the internal between successive interrupts in modes 1 and 2. A pullup-resistor on the $\overline{INT}$ pin will facilitate a positive swing.

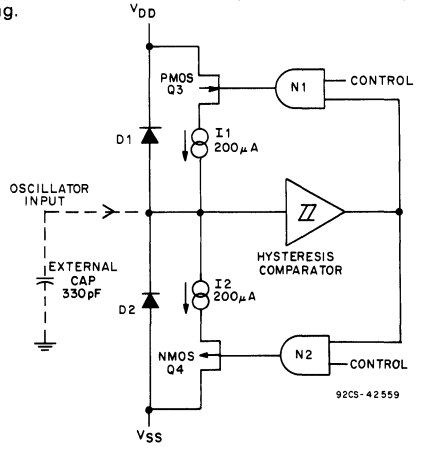


Fig. 6 - Equivalent circuit for oscillator input.

5.5 Notes

Note 1: When addressing the CDP68HC68A2, CE should always (especially important when more than one SPI peripheral are on the same SPI bus):

A) Be activated for the duration of both phases of a Single or Burst Mode transfer for a valid operation. This encompasses two SPI cycles for single byte transfers and greater than two SPI cycles for multiple byte transfer or burst mode.

B) Be deactivated some time before it is necessary to access the SPI bus for any other reason than to complete the last operation. This resets the SPI logic and tristates the MISO line from driving the SPI bus. Re-addressing will always be necessary after deassertion of the chip enable.

Note 2: The internal Channel Address Register (CAR) is affected by a Data Register access and will change the next START ADDRESS to be converted if the read sequence is incomplete. A READ sequence is complete when Data Registers READS exactly span all of the selected channels. Then, the CAR contents observed in the STATUS register will equal the initial value written to the SAR before Register Access and the SAE would not need to be activated. The effect of incomplete READ sequences can be avoided by always writing to all three of the CONTROL REGISTERS at the initialization of conversions. For example, addressing a WRITE to the MSR, CSR, then the SAR. This may be followed by addressing a read of the STATUS REGISTER if desired. Further conversions in the same mode may be initiated when the control register sequence is written with the CSR followed by the SAR. This sequence forces resetting of all status bits for successive operations.

Note 3: Status and Control Registers can be examined (read) without affecting the conversion.

Note 4: When in the burst mode, a Data Register, when first retrieved, will have already internally addressed the next corresponding selected channel Data Register. This occurs because the auto-increment logic activates at the end of a Data Register read. Because of this, it is necessary to complete the read of all valid channels in order to test the validity of the DV bit before the CE is deactivated. It appears most convenient and necessary in this case, to access channels from Starting Address to the last valid data conversion by the burst mode. Important in modes 2 and 3 since all conversions are complete when Data is retrieved and the DV bit cleared at the time of addressing.

Note 5: In the burst mode, the REGISTER ALLOCATION TABLES can be accessed and will auto-increment to sequential addresses and selected channels. While in the burst mode, both data register address and channel address beyond the highest selected channel is the lowest selected channel. This implies that re-addressing is necessary if control and status registers need to be accessed following data registers. For example, a READ of channel 7 (address 0F) will not be followed by a READ of the MSR, but Data Register 0 (address 00).

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