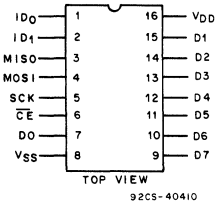
CDP68HC68P1

Advance Information



TERMINAL ASSIGNMENT

CMOS Single Port Input/Output

Features:

- *Fully static operation*
- *Operating voltage range 3-6 V*
- *Compatible with RCA/Motorola SPI bus*
- *2 external address pins tied to V_{DD} or V_{SS} to allow up to 4 devices to share the same chip enable*
- *Versatile bit-set and bit-clear capability*
- *Accepts either SCK clock polarity - SCK voltage level is latched when chip enable goes active*
- *All inputs are Schmitt-Trigger*
- *8-Bit I/O port - each bit can be individually programmed as an input or output via an 8-bit data direction register*
- *Programmable on-board comparator*
- *Simultaneous transfer of compare information to CPU during read or write - separate access not required*

The single port I/O is a serially addressed 8 bit Input/Output port that allows byte or individual bit control. It consists of three registers, an output buffer and control logic. Data is shifted in and out of the port via a shift register that utilizes the SPI (Serial Peripheral Interface) bus. The I/O port data flow is controlled by the Data Direction Register and data is stored in the Data Register that outputs or senses the logic levels at the buffered I/O pins. All inputs, including the serial interface are schmitt triggered. The device also features a compare function that compares the data register and port pin values for 4 programmable conditions and sets a software accessible flag if the condition is satisfied. The user also has the option of bit-set or bit-clear when writing to the data register.

The CDP68HC68P1 is supplied in 16-lead, hermetic, dual-in-line side-brazed ceramic (D suffix), 16-lead dual-in-line plastic (E suffix) and 16-lead, surface mount, (small outline), plastic (M suffix) packages.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)* ..... 400 mW
For T_A = +70 to +85°C (PACKAGE TYPE M)* ..... Derate Linearly at 6 mW/°C to 310 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent.

File Number **1858**

RECOMMENDED OPERATING CONDITIONS AT T_A = -40° to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS		UNITS
		ALL TYPES		
		MIN.	MAX.	
DC Operating Voltage Range		3	6	V
Serial Clock Frequency	f_{SCK}			
	V_{DD} = 3 V	—	1.05	MHz
	V_{DD} = 4.5 V	—	2.1	
Input Voltage Range				
	V_{IH}	—	V_{DD} + 0.3	V
	V_{IL}	-0.3	—	

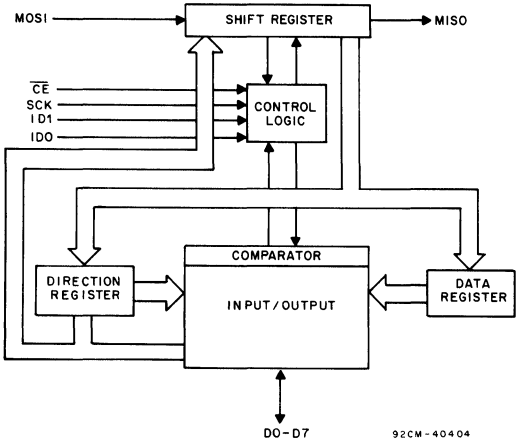


Fig. 1 - Single port I/O block diagram.

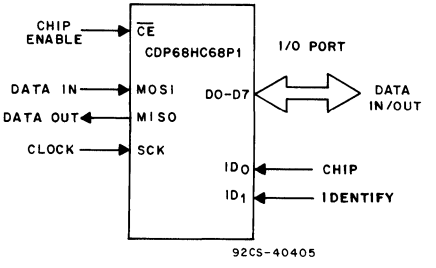


Fig. 2 - Single port I/O.

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STATIC ELECTRICAL CHARACTERISTICS AT T_A = -40 to +85° C, V_{DD} = 3.3 V ± 10%, Except as Noted

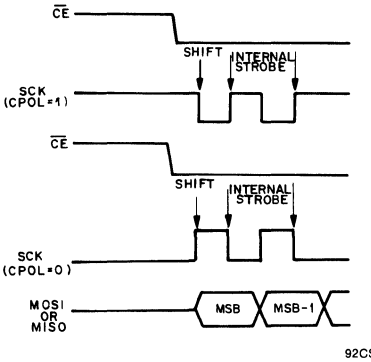
CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			MIN.	TYP. •	MAX.	
Standby Device Current	I_{DDS}	—	—	1	15	μA
Output Voltage High Level	V_{OH}	I_{OH} = -0.4 mA, V_{DD} = 3 V	2.7	—	—	V
Output Voltage Low Level	V_{OL}	I_{OL} = 0.4 mA, V_{DD} = 3 V	—	—	0.3	
Input Voltage D0-D7						
Positive Trigger Threshold	V_P	—	1.85	—	2.4	
Negative Trigger Threshold	V_N	—	0.85	—	1.35	
Hysteresis	V_{IH}	—	0.85	—	1.25	
Input Voltage ID0, ID1, MOSI, SCK, $\overline{CE}$						
Positive Trigger Threshold	V_P	—	1.3	—	1.9	
Negative Trigger Threshold	V_N	—	0.8	—	1.2	
Hysteresis	V_{IH}	—	0.5	—	0.95	
Input Leakage Current	I_{IN}	—	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	—	—	—	±10	μA
Operating Device Current	I_{OPER} #	V_{IN} = V_{IL}, V_{IH}	—	0.1	1	mA
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25° C	—	4	6	pF

• Typical values are for T_A = 25° C and nominal V_{DD}. # Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.

STATIC ELECTRICAL CHARACTERISTICS AT T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as Noted

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			MIN.	TYP. •	MAX.	
Standby Device Current	I_{DDS}	—	—	1	15	μA
Output Voltage High Level	V_{OH}	I_{OH} = -1.6 mA, V_{DD} = 4.5 V	3.7	—	—	V
Output Voltage Low Level	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = 4.5 V	—	—	0.4	
Output Voltage High Level	V_{OH}	$I_{OH} \leq 20\ \mu A$, V_{DD} = 4.5 V	4.4	—	—	
Output Voltage Low Level	V_{OL}	$I_{OL} \leq 20\ \mu A$, V_{DD} = 4.5 V	—	—	0.1	
Input Voltage D0-D7						
Positive Trigger Threshold	V_P	—	2.15	—	3.05	
Negative Trigger Threshold	V_N	—	1.35	—	2	
Hysteresis	V_{IH}	—	0.8	—	1.2	
Input Voltage ID0, ID1,MOSI, SCK, $\overline{CE}$						
Positive Trigger Threshold	V_P	—	3.15	—	3.85	
Negative Trigger Threshold	V_N	—	1.7	—	2.25	
Hysteresis	V_{IH}	—	1.3	—	1.7	
Input Leakage Current	I_{IN}	—	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	—	—	—	±10	μA
Operating Device Current	I_{OPER}#	V_{IN} = V_{IL}, V_{IH}	—	0.2	2	mA
Input Capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz, T_A = 25° C	—	4	6	pF

• Typical values are for T_A = 25° C and nominal V_{DD}. # Outputs open circuited; cycle time = Min. t_{cycle}, duty = 100%.



NOTE
CPOL AND CPHA ARE BITS IN THE CDP68HC05C4 and CDP68HC05D2 MCU CONTROL REGISTER AND DETERMINE INACTIVE CLOCK POLARITY AND PHASE CPHA MUST ALWAYS EQUAL 1

Fig. 3 - Data transfers utlizing clock input.

4

Introduction

The single port I/O is serially accessed via a 3 wire plus chip enable synchronous bus. It features 8 data pins that are programmed as inputs or outputs. Serial access consists of a two-byte operation. The first byte shifted in is the control byte that configures the device. The second byte transferred is the data byte that is read from or written to the data register or data direction register. This data byte can also be programmed to act as a mask to set or clear individual bits.

Functional Description

The single port I/O consists of three byte-wide registers, (data direction, data and shift) an input/output buffer and control logic circuitry. (See fig. 1, block diagram). Data is transferred between the I/O data and data direction registers via the shift register. Once the I/O port is selected, the first byte shifted in to the shift register is the control byte that register selects, (the Data or Data direction register), determines data transfer direction (read or write) and sets the compare feature and function (mask or data) of the byte immediately following the control byte, the data byte. (See Addressing the Single Port I/O) Each bit of the data register may be individually programmed as an input or output. A logic low in a data direction bit programs that pin as an input, a logic high makes it an output. A read operation of data register pins programmed as inputs reflects the current logic level present at the buffered port pins. A read operation of those data register pins programmed as outputs indicates the last value written to that location. At power-up, all port pins are configured as unterminated inputs. Two chip identify pins are used to allow up to 4 I/O ports to share the same chip enable signal. The first two bits shifted in are compared with the hardwired levels at the chip identify pins to enable the selected I/O for serial data transfer. Note that when chip enable becomes true, the compare flag is latched for all devices sharing the same chip enable.

Compare Function

The value of a port pin (D0-D7), configured as an input, is compared with the corresponding bit value (DR0-DR7) stored in the Data Register. Pins configured as outputs are assumed to have the same value as the corresponding bit stored in the Data Register. The compare function is programmed via C01 and C00 (CM1, CM0) of the Address Byte. The following values for CM1 and CM0 will sense one of four separate conditions:

CM1	CM0	Condition
0	0	- at least one non-match
0	1	- all match
1	0	- all are non-match
1	1	- at least one match

The compare flag is set to one when the programmed condition is satisfied. Otherwise, the flag is cleared to zero. The compare flag is latched when the device is enabled (a transition of $\overline{CE}$ from "High" to "Low").

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Data Format

During write operations, the data byte that follows the control byte is normally the data word that is transferred to the data or data direction register. Control bits 2 and 3 (DF0 and DF1) change the interpetation of this data as listed below. Note that one or more bits can be set or cleared in either register without having to write to bits not requiring change.

C03 DF1	C02 DF0	OPERATION
0	X	Data following the control word will be written to the selected register.
1	0	Data following the control word is a mask. Those bits which are a 1 will cause that register flip-flop to be cleared to 0. Those which are a 0 will cause that register flip-flop to be unchanged.
1	1	Data following the control word is a mask. Those bits which are a 1 will cause that register flip-flop to be set to 1; those which are a 0 will cause that register flip-flop to be unchanged.

for example,

CONTROL	DATA	PREVIOUS REGISTER VALUE	NEW REGISTER VALUE
C07 C06 C05 1 0 X C01 C00	11110000	10101010	11110000
C07 C06 C05 1 1 1 C01 C00	11110000	10101010	11111010
C07 C06 C05 1 1 0 C01 C00	11110000	10101010	00001010
C07 C06 C05 1 1 X C01 C00	00000000	10101010	10101010

X = Don't Care

Addressing the Single Port I/O

The Serial Peripheral Interface (SPI) utilized by the I/O Port is a serial synchronous bus for control and data transfers. It consists of a SCK clock input pin that shifts data out of the I/O port (MISO, MASTER IN, SLAVE OUT) and latches data presented at the input pin, MOSI (master out, slave in). Data is transferring in most significant bit first. There is one SCK clock for each bit transferred and bits are transferred in groups of eight.

When the I/O port is selected by bringing the chip enable pin low, the logic level at the SCK input is sampled to determine the internal latching and shift polarity for input and output signals on the SPI. (See Fig. 3).

The first byte shifted in when the chip is selected is always the control byte followed by one or more bytes that become data or a mask for the data and data direction register. As the control byte is being shifted in one the MOSI line, data on the MOSI line shifts out. (See Fig. 4).

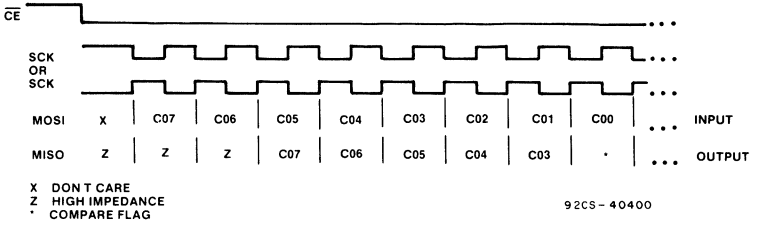


Fig. 4 - Control byte.

C07 (ID1), C06 (ID0): Chip-Identify bits

C05 (RS): Register Select. When RS is low, the data register is selected. When RS is high, the Direction Register is selected.

C04 ($\overline{R}$/W): $\overline{Read}$/Write. Low when data is to be transferred from the SPI I/O to the CPU (read) and high when the I/O is receiving data from the CPU (write).

C03 (DF1), C02 (DF0): Data Format Bits. These have meaning only when $\overline{R}$/W is high. During a write operation, DF1 and DF0 control how the byte following the control word is interpreted. See "DATA FORMAT".

C01 (CM1), C00 (CM0): Compare Mode Select. These bits select one of four events which will set the internal Condition Flag. (See "COMPARE OPERATION")

Read Operation

During a read operation, the CPU transfers data from the I/O by first sending a control byte on the MOSI line while the chip-selected I/O sends compare information followed by one or more data bytes on the MISO line.

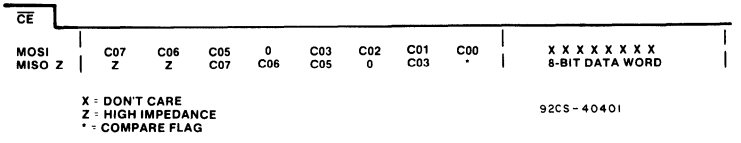
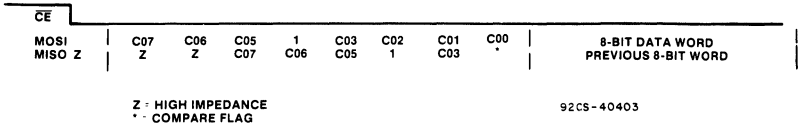


Fig. 5 - Read bytes.

The selected register will be continuously read if $\overline{CE}$ is held low after the first data byte is shifted out.

Write Operation

During a write operation, the data byte follows the control byte for the selected register. While this byte is being shifted in, old data from that register is shifted out. If CE remains low after the data byte is shifted in, MISO becomes high impedance and the new data is placed in the selected register.



At the time the eighth data bit is strobed into the data pins (D0-D7) will change as indicated in Fig. 7.

Fig. 6 - Write bytes.

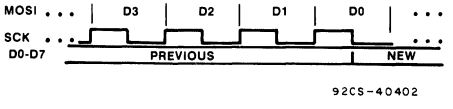


Fig. 7 - Port-pin data changes.

Pin Description

ID0, ID1

Chip identify pins, normally tied to V_{DD} or V_{SS}. The 4 possible combinations of these pins allow 4 I/Os to share a common chip enable. When the levels at these pins match those of the identify bits in the control word, the serial bus is enabled. The chip identify pins will retain their previous logic state if the lines driving them become Hi-Z.

MISO

Master-in, Slave out pin. Data bytes are shifted out at this pin most significant bit first. When the chip enable signal is high, this pin is Hi-Z.

MOSI

Master-out, Slave in pin. Data bytes are shifted in at this pin most significant bit first. This pin will retain its previous logic state if its driving line becomes Hi-Z.

SCK

Serial clock input. This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

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$\overline{CE}$

A negative chip enable input. A high to low transition on this pin latches the inactive SCK polarity and compare flag and indicates the start of a data transfer. The serial interface logic is enabled only when CE is low. This pin will retain its previous logic state if its driving line becomes Hi-Z.

D0-D7

I/O Port pins. Individual programmable inputs or outputs.

V_{DD} and V_{SS}

Positive and negative power supply line.

All pins except the power supply lines and MISO have Schmitt-trigger buffered inputs.

DYNAMIC ELECTRICAL CHARACTERISTICS - BUS TIMING V_{DD} ± 10%, V_{SS} = 0 V dc, T_A = -40° to +85°C, C_L = 200 pF. See Figs. 8 and 9.

CHARACTERISTIC		LIMITS (ALL TYPES)				UNITS
		V_{DD} = 3.3 V		V_{DD} = 5 V		
		MIN.	MAX.	MIN.	MAX.	
Chip Enable Set-Up Time	t_{EVCV}	200	—	100	—	ns
Chip Enable after Clock Hold Time	t_{CVEX}	250	—	125	—	
Clock Width High	t_{WH}	400	—	200	—	
Clock Width Low	t_{WL}	400	—	200	—	
Data In to Clock Set-Up Time	t_{DVCV}	200	—	100	—	
Data In after Clock Hold Time	t_{CVDX}	200	—	100	—	
Clock to Data Propagation Delay	t_{CVDV}	—	200	—	100	
Chip Disable to Output High Z	t_{EXQZ}	—	200	—	100	
Output Rise Time	t_r	—	200	—	100	
Output Fall Time	t_f	—	200	—	100	
Clock to Data Out Active	t_{CVQX}	—	200	—	100	
Clock Recovery Time	t_{REC}	200	—	200	—	

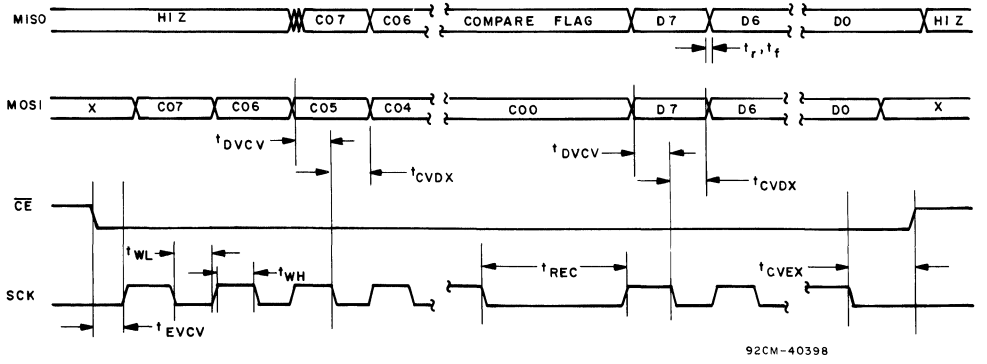

Fig. 8 - Write cycle timing waveforms.

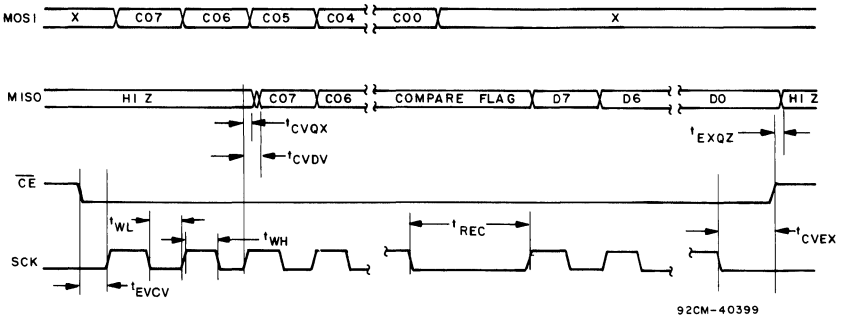

Fig. 9 - Read cycle timing waveforms.

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