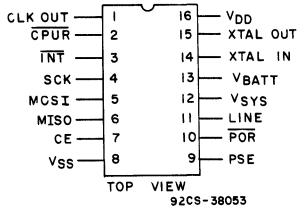
CDP68HC68T1

Advance Information



TERMINAL ASSIGNMENT

CMOS Real-Time Clock with RAM and Power Sense/Control

Features:

- *SPI (Serial Peripheral Interface)*
- *Full clock features: sec., min., hrs. (12/24, AM/PM), day of week, date, month, year, (0-99), auto leap year*
- *32-word x 8-bit RAM*
- *Seconds, minutes, hours alarm*
- *Automatic power loss detection*
- *Minimum standby (timekeeping) voltages: 2.2 volts*
- *Selectable crystal or 50/60-Hz line input*
- *Buffered clock output*
- *Battery input pin that powers oscillator and also connects to the V_{DD} pin when main power fails*
- *Three independent interrupt modes: alarm, periodic or power-down sense*

The CDP68HC68T1, real-time clock provides a time/calendar function, a 32 byte static RAM and a 3-wire serial peripheral interface (SPI bus). The primary function of the clock is to divide down a frequency input that can be supplied by the on-board oscillator in conjunction with an external crystal or by an external clock source. The clock either operates with a 32+kHz, 1+MHz, 2+MHz or 4+MHz crystal or it can be driven by an external clock source at the same frequencies. In addition, the frequency can be selected to allow operation from a 50 or 60-Hz input. The time registers furnish seconds, minutes, and hours data while the calendar registers offer day of week, date, month and year information. The data in the time/calendar registers is in BCD format. In addition, 12 or 24-hour operation can be selected with an AM-PM indicator available in the 12-hour mode. The T1 has a separate clock output that supplies one of 7 selectable frequencies.

Computer handshaking is established with a "wired or" interrupt output. The interrupt can be activated by any one of three separate internal sources. The first is an alarm circuit that consists of seconds, minutes and hours alarm latches that trigger the interrupt when they are in coincidence with the value in the seconds, minutes and hours time counters. The second interrupt source is one of 15 periodic signals that range from subsecond to daily intervals. The final interrupt source is from the power-sense circuit that is used with the LINE input pin to monitor power failures. Two other pins, the power supply enable (PSE) output and the V_{SYS} input are used for external power control. The $\overline{CPUR}$ reset output pin is available for power-down operation and is activated under software control. $\overline{CPUR}$ is also activated by a watchdog circuit that if enabled requires the CPU to toggle the CE pin periodically without a serial data transfer.

The CDP68HC68T1 is available in a 16-lead hermetic dual-in-line ceramic package (D suffix), in a 16-lead dual-in-line plastic package (E suffix), and in a 20-lead small-outline plastic package (M suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS EXCEPT LINE ..... -0.5 to V_{DD} +0.5 V
$V_{SYS} \leq V_{DD}$ + 1.5 V
DC INPUT CURRENT, ANY ONE INPUT (LINE INPUT, -10 mA) ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -40° to +70° C (PACKAGE TYPE M) * ..... 400 mW
For T_A = +70° to +85° C (PACKAGE TYPE M) * ..... Derate linearly at 6.0 mW/° C to 310 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 40 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125° C
PACKAGE TYPE E and M ..... -40 to +85° C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

* Printed-circuit board mount: 57 mm x 57 mm minimum area x 1.6 mm thick G10 epoxy glass, or equivalent

File Number **1547**

OPERATING CONDITIONS at T_A = -40° to +85°C
For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS		UNITS
		Min.	Max.	
DC Operating Voltage Range		3	6	V
DC Standby (Timekeeping) Voltage *	V_{STBY}	2.2	—	V
Input Voltage Range	V_{IH}	0.7 V_{DD}	V_{DD} + 0.3	V
(Except Line Input)	V_{IL}	-0.3	0.3 V_{DD}	V
Serial Clock Frequency (V_{DD} = 4.5 V)	f_{SCK}	—	2.1	MHz

* Timekeeping function only, no READ/WRITE accesses

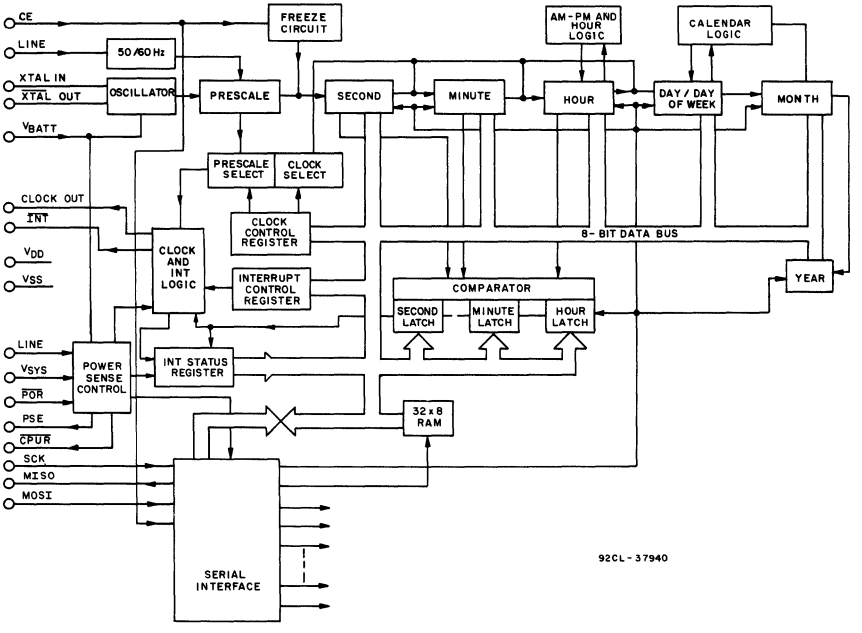


Fig. 1 - Real-time clock functional diagram.

CDP68HC68T1

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = V_{BATT} = 5 V ± 5%, Except as Noted

CHARACTERISTIC		CONDITIONS	LIMITS CDP68HC68T1 MIN.	TYP.•	MAX.	UNITS
Quiescent Device Current	I_{DD}	—	—	1	10	μA
Output Voltage High Level	V_{OH}	I_{OH} = -1.6 mA, V_{DD} = 4.5 V	3.7	—	—	V
Output Voltage Low Level	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = 4.5 V	—	—	0.4	V
Output Voltage High Level	V_{OH}	$I_{OH} \leq 10\ \mu A$, V_{DD} = 4.5 V	4.4	—	—	V
Output Voltage Low Level	V_{OL}	$I_{OL} \leq 10\ \mu A$, V_{DD} = 4.5 V	—	—	0.1	V
Input Leakage Current	I_{IN}	—	—	—	±1	μA
3-State Output Leakage Current	I_{OUT}	—	—	—	±10	μA
Operating Current# (I_D + I_b) V_{DD} = V_B = 5 V Crystal Operation		32 kHz	—	0.08	0.1	mA
		1 MHz	—	0.5	0.6	mA
		2 MHz	—	0.7	0.84	mA
		4 MHz	—	1	1.2	mA
Pin 14 External Clock (Squarewave)# (I_D + I_b) V_{DD} = V_B = 5 V		32 kHz	—	0.02	0.024	mA
		1 MHz	—	0.1	0.12	mA
		2 MHz	—	0.2	0.24	mA
		4 MHz	—	0.4	0.5	mA
Standby Current# V_B = 3 V Crystal Operation	I_b	32 kHz	—	20	25	μA
		1 MHz	—	200	250	μA
		2 MHz	—	300	360	μA
		4 MHz	—	500	600	μA
Operating Current# V_{DD} = 5 V, V_B = 3 V Crystal Operation				I_D / I_B		I_D / I_B	
		32 kHz	—	25 / 15		30 / 20	
		1 MHz	—	0.08 / 0.15		0.1 / 0.18	mA
		2 MHz	—	0.15 / 0.25		0.18 / 0.3	mA
		4 MHz	—	0.3 / 0.4		0.36 / 0.5	mA
Standby Current# V_B = 2.2 V Crystal Operation	I_b	32 kHz	—	10	12	μA
Input Capacitance	C_{IN}	V_{IN} = 0, T_A = 25°C	—	—	2	pF
Maximum Rise and Fall Times (Except XTAL Input and $\overline{POR}$ Pin 10)	t_r,t_f	—	—	—	2	μs
Input Voltage (Line Input Pin Only, Power-Sense Mode)		—	0	10	12	V
$V_{SYS} > V_B$ (For V_B Not Internally Connected to V_{DD})	V_t	—	—	0.7	—	V
Power-On Reset ($\overline{POR}$) Pulse Width			100	75	—	ns

• Typical values are for T_A = 25° C and nominal V_{DD}.

Clock Out (Pin 1) disabled, outputs open-circuited. No serial access cycles.

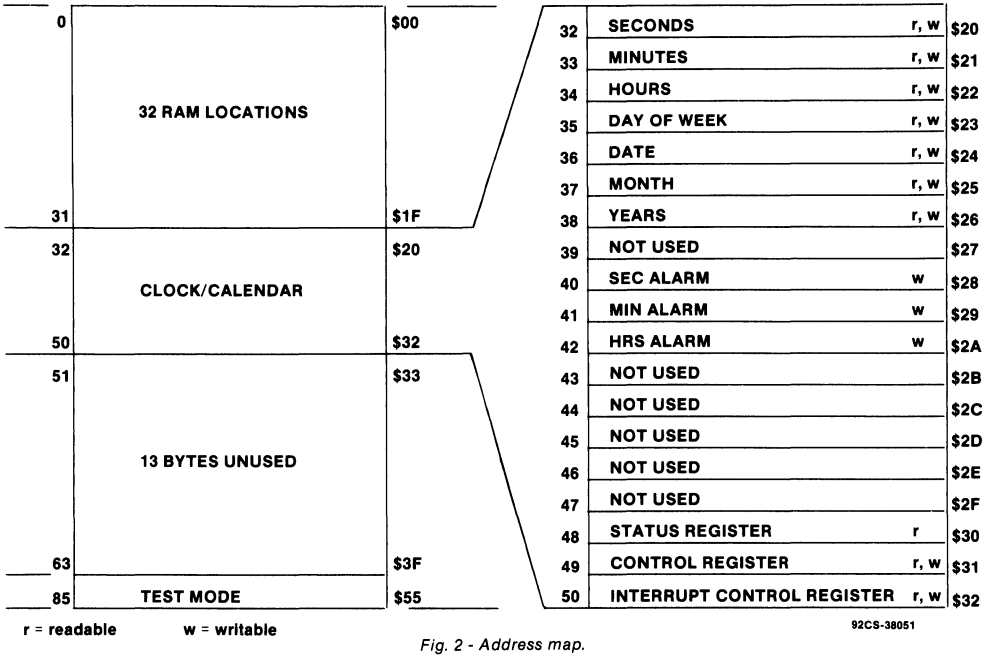


Fig. 2 - Address map.

TABLE I - Clock/Calendar and Alarm Data Modes

ADDRESS LOCATION (H)	FUNCTION	DECIMAL RANGE	BCD DATA RANGE	BCD DATE • EXAMPLE
20	Seconds	0-59	00-59	18
21	Minutes	0-59	00-59	49
22	* Hours 12 Hour Mode	1-12	81-92 (AM) A1-B2 (PM)	A3
	Hours 24 Hour Mode	0-23	00-23	15
23	Day of the Week (Sunday = 1)	1-7	01-07	03
24	Day of the Month (Date)	1-31	01-31	29
25	Month Jan = 1, Dec = 12	1-12	01-12	10
26	Years	0-99	00-99	85
28	Alarm Seconds	0-59	00-59	18
29	Alarm Minutes	0-59	00-59	49
2A	** Alarm Hours 12 Hour Mode	1-12	01-12 (AM) 21-32 (PM)	23
	Alarm Hours 24 Hour Mode	0-23	00-23	15

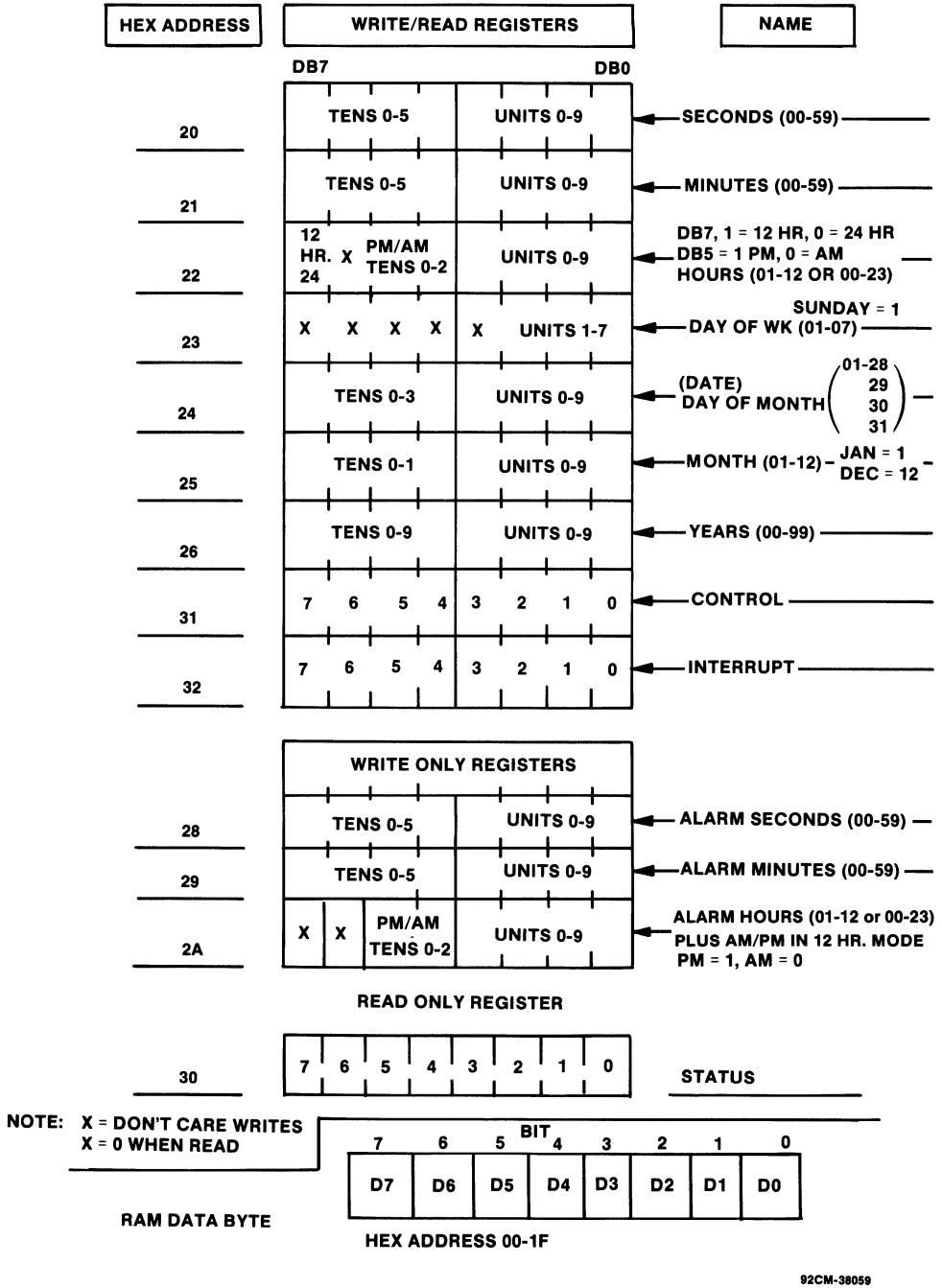
• Example 3:49:18, Tuesday, Oct. 29, 1985.

* Most significant Bit, D7, is "0" for 24 hours, and "1" for 12 hour mode. Data Bit D5 is "1" for P.M and "0" for A.M. in 12 hour mode.

** Alarm hours, Data Bit D5 is "1" for P.M and "0" for A M. in 12 hour mode. Data Bits D7 and D6 are DON'T CARE.

CDP68HC68T1

PROGRAMMERS MODEL - CLOCK REGISTERS



FUNCTIONAL DESCRIPTION

The SPI real-time clock consists of a clock/calendar and a 32 x 8 RAM. Communications is established via the SPI (Serial Peripheral Interface) bus. In addition to the clock/calendar data from seconds to years, and system flexibility provided by the 32-byte RAM, the clock features computer handshaking with an interrupt output and a separate squarewave clock output that can be one of 7 different frequencies. An alarm circuit is available that compares the alarm latches with the seconds, minutes and hours time counters and activates the interrupt output when they are equal. The clock is specifically designed to aid in power-down/up applications and offers several pins to aid the designer of battery back-up systems.

Mode Select

The voltage level that is present at the V_{SYS} input pin at the end of power-on-reset selects the device to be in the single supply or battery back-up mode.

Single-Supply Mode—If V_{SYS} is a logic high when power-on-reset is completed, CLK OUT, PSE and CPUR will be enabled and the device will be completely operational. CPUR will be placed low if the logic level at the V_{SYS} pin goes low. If the output signals CLK OUT, PSE and CPUR are disabled due to a power-down instruction, V_{SYS} brought to a logic low and then to a logic high will re-enable these outputs. An example of the single-supply mode is where only one supply is available and V_{DD}, V_{BATT} and V_{SYS} are tied together to the supply.

Battery Back-up Mode—If V_{SYS} is a logic low at the end of power-on-reset, CLK OUT, PSE and CPUR and the CE pin will be disabled (CLK OUT, PSE and CPUR low). This condition will be held until V_{SYS} rises to a threshold (about 0.7 volt) above V_{BATT}. The outputs CLK OUT, PSE and CPUR will then be enabled and the device will be operational. If V_{SYS} falls below a threshold above V_{BATT}, the outputs CLK OUT, PSE and CPUR will be disabled. An example of battery back-up operation occurs if V_{SYS} is tied to V_{DD} and V_{DD} is not connected to a supply when a battery is connected to the V_{BATT} pin. (See Pin Functions V_{BATT} for Battery Back-up Operation)

CLOCK/CALENDAR (See Figs. 1 and 2.)

The clock/calendar portion of this device consists of a long string of counters that is toggled by a 1-Hz input. The 1-Hz input is generated by a prescaler driven by an on-board oscillator that utilizes one of four possible external crystals or that can be driven by an external clock source. The 1-Hz trigger to the counters can also be supplied by a 50 or 60-Hz input source that is connected to the LINE input pin.

The time counters offer seconds, minutes and hours data in 12 or 24-hour format. An AM/PM indicator is available that once set, toggles every 12 hours. The calendar counters consist of day (day of week), date (day of month), month and years information. Data in the counters is in BCD format. The hours counter utilizes BCD for hour data plus bits for 12/24 hour and AM/PM. The 7 time counters are accessed serially at addresses 20H through 26H. (See Table I).

RAM

The real-time clock also has a static 32 x 8 RAM that is located at addresses 00-1FH. Transmitting the address/control word with bit 5 low selects RAM access. Bits 0 through 4 select the RAM location.

ALARM

The alarm is set by accessing the three alarm latches and loading the required data. The alarm latches consist of seconds, minutes and hours registers. When their outputs equal the values in the seconds, minutes and hours time counters, an interrupt is generated. The interrupt output will go low if the alarm bit in the Interrupt Control register is set high. The alarm interrupt bit in the Status register is set when the interrupt occurs.* To preclude a false interrupt when loading the time counters, the alarm interrupt bit should be set low in the Interrupt Control register. This procedure is not required when the alarm time is set.

WATCHDOG FUNCTION (See Fig. 6.)

When bit 7 in the Interrupt Control register is set high, the Clock's CE (chip enable) pin must be toggled at a regular interval without a serial data transfer. If the CE is not toggled, the clock will supply a CPU reset pulse and bit 6 in the Status Register will be set. Typical service and reset times are listed below.

	50 Hz		60 Hz		XTAL	
	Min.	Max.	Min.	Max.	Min.	Max.
Service Time	—	10ms	—	8.3ms	—	7.8ms
Reset Time	20	40ms	16.7	33.3ms	15.6	31.3ms

CLOCK OUT

The value in the 3 least significant bits of the Clock Control register selects one of seven possible output frequencies. (See Clock Control Register). This squarewave signal is available at the CLK OUT pin. When Power-Down operation is initiated, the output is set low.

CONTROL REGISTERS AND STATUS REGISTERS

The operation of the Real-Time Clock is controlled by the Clock Control and Interrupt Control registers. Both registers are read-write registers. Another register, the Status register, is available to indicate the operating conditions. The Status register is a read-only register.

POWER CONTROL

Power control is composed of two operations, Power Sense and Power Down/Up. Two pins are involved in power sensing, the LINE input pin and the $\overline{INT}$ output pin. Two additional pins are utilized during power-down/up operation. They are the PSE (Power Supply Enable) output pin and V_{SYS} input pin.

POWER SENSING (See Fig. 3.)

When Power Sensing is enabled (Bit 5 = 1 in Interrupt Control Register), AC transitions are sensed at the LINE input pin. Threshold detectors determine when transitions cease. After a delay of 2.68 to 4.64 ms plus the external input circuit RC time constant, an interrupt is generated and a bit is set in the status register. This bit can then be sampled to see if system power has turned back on. See PIN FUNCTIONS, LINE PIN. The power-sense circuitry operates by sensing the level of the voltage presented at the line input pin. This voltage is centered around V_{DD} and as long as it is either plus or minus a threshold (about 1 volt) from V_{DD} a power-sense failure will not be indicated. With an ac signal present, remaining in this V_{DD} window longer than a minimum of 2.68 ms will activate the power-sense circuit. The larger the amplitude of the ac signal, the less time it

*See PIN FUNCTIONS, $\overline{INT}$ PIN.

CDP68HC68T1

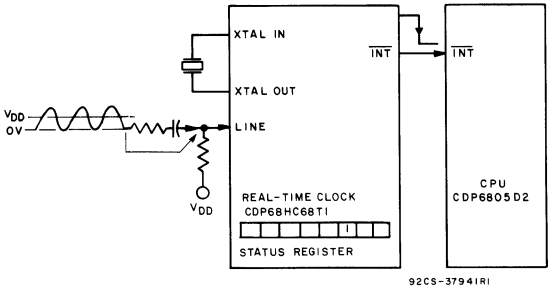


Fig. 3 - Power-sensing functional diagram.

spends in the V_{DD} window and the less likely a power failure will be detected. A 60-Hz, 10 V_{p-p} sinewave voltage is an applicable signal to present at the LINE input pin to set up the power-sense function.

POWER DOWN (See Fig. 4.)

Power down is a processor-directed operation. A bit is set in the Interrupt Control Register to initiate operation. 3 pins are affected. The PSE (Power Supply Enable) output, normally high, is placed low. The CLK OUT is placed low. The $\overline{CPUR}$ output, connected to the processors reset input is also placed low. In addition, the Serial Interface is disabled.

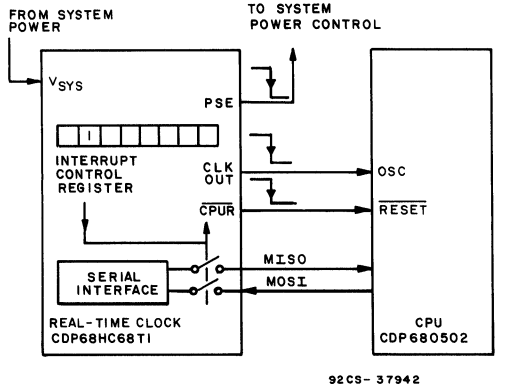


Fig. 4 - Power-down functional diagram.

POWER UP (See Figs. 5 and 6.)

Two conditions will terminate the Power-Down mode. The first condition (See Fig. 5) requires an interrupt. The interrupt can be generated by the alarm circuit, the programmable periodic interrupt signal, or the power-sense circuit.

The second condition that releases Power Down occurs when the level on the V_{SYS} pin rises about 1 volt above the level at the V_{BATT} input, after previously falling to the level of V_{BATT} (See Fig.6) in the Battery Back-up Mode or V_{SYS} falls to logic low and returns high in the Single Supply Mode.

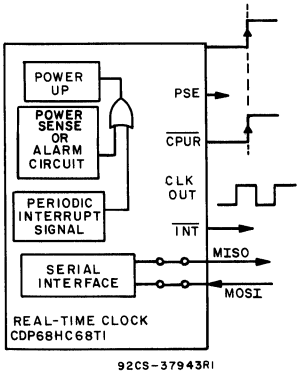


Fig. 5 - Power-up functional diagram (initiated by Interrupt Signal).

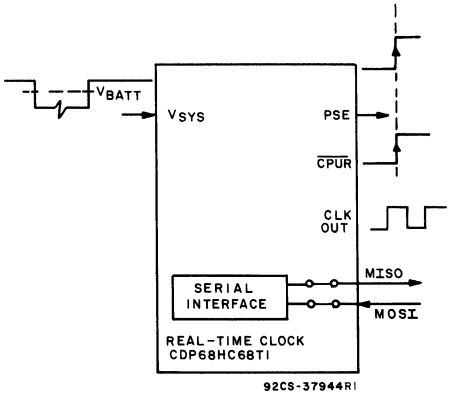


Fig. 6 - Power-up functional diagram (initiated by a rise in voltage on the "V_{SYS}" pin).

CDP68HC68T1

PIN FUNCTIONS

CLK OUT—Clock output pin. One of 7 frequencies can be selected (or this output can be set low) by the levels of the three LSB's in the clock-control register. If a frequency is selected, it will toggle with a 50% duty cycle except 2 Hz in the 50-Hz timebase mode. (Ex. if 1 Hz is selected, the output will be high for 500 ms and low for the same period.) During power-down operation (bit 6 in Interrupt Control Register set to "1"), the clock-output pin will be set low.

$\overline{\text{CPUR}}$—CPU reset output pin. This pin functions as an N-channel only, open-drain output and requires an external pull-up resistor.

$\overline{\text{INT}}$—Interrupt output pin. This output is driven from a single NFET pull-down transistor and must be tied to an external pull-up resistor. The output is activated to a low level when:

1. Power-sense operation is selected (B5 = 1 in Interrupt Control Register) and a power failure occurs.
2. A previously set alarm time occurs. The alarm bit in the status register and interrupt-out signal are delayed 30.5 μs when 32-kHz operation is selected and 15.3 μs for 2-MHz and 7.6 μs for 4-MHz. (See important application note.)
3. A previously selected periodic interrupt signal activates.

The status register must be read to set the Interrupt output high after the selected periodic interval occurs. This is also true when conditions 1 and 2 activate the interrupt. If power down had been previously selected, the interrupt will also reset the power-down functions.

SCK, MOSI, MISO—See Serial Peripheral Interface (SPI) section in this data sheet.

CE—A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state. This pin is also used for the watchdog function.

V_{SS}—The negative power-supply pin that is connected to ground.

PSE—Power-supply enable output pin. This pin is used to control power to the system. The pin is set high when:

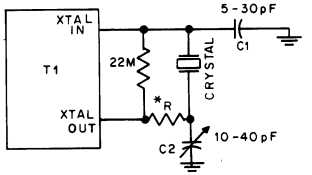
1. V_{SYS} rises above the V_{BATT} voltage after V_{SYS} was placed low by a system failure.
2. An interrupt occurs.
3. A power-on reset (if V_{SYS} is a logic high).

The PSE pin is set low by writing a high into bit 6 (power-down bit) in the Interrupt Control Register.

$\overline{\text{POR}}$—Power-on reset. A Schmitt-trigger input that generates a power-on internal reset signal using an external R-C network. Both control registers and frequency dividers for the oscillator and line input are reset. The status register is reset except for the first time up bit (B4), which is set. Single supply or battery back-up operation is selected at the end of $\overline{\text{POR}}$.

LINE—This input is used for two functions. The first function utilizes the input signal as the frequency source for the timekeeping counters. This function is selected by setting bit 6 in the Clock Control Register. The second function enables the line input to sense a power failure. Threshold detectors operating above and below V_{DD} sense an ac voltage loss. Bit 5 must be set to "1" in the Interrupt Control Register and crystal or external clock source operation is required. Bit 6 in the Clock Control Register must be low to select XTAL operation.

OSCILLATOR CIRCUIT—The CDP68HC68T1 has an on-board 150K resistor that is switched in series with its internal inverter when 32-kHz is selected via the clock-control register. Note: When first powered up the series resistor is not part of the oscillator circuit. (The CDP68HC68T1 sets up for a 4-MHz oscillator.)



ALL FREQUENCYS
RECOMMENDED OSCILLATOR CIRCUIT.
C1, C2 VALUES CRYSTAL DEPENDENT

*R USED FOR 32 KHz OPERATION ONLY
100 K - 300 K RANGE AS SPECIFIED
BY CRYSTAL MANUFACTURER.

92CS-42272

Fig. 7 - Oscillator circuit.

V_{SYS}—This input is connected to the system voltage. After the CPU initiates power down by setting bit 6 in the Interrupt Control Register to "1", the level on this pin will terminate power down if it rises about 0.7 volt above the level at the V_{BATT} input pin after previously falling below V_{BATT} + 0.7 volt. When power down is terminated, the PSE pin will return high and the Clock Output will be enabled. The $\overline{\text{CPUR}}$ output pin will also return high. The logic level present at this pin at the end of $\overline{\text{POR}}$ determines the CDP68HC68T1's operating mode.

V_{BATT}—The oscillator power source. The positive terminal of the battery should be connected to this pin. When the level on the V_{SYS} pin falls below V_{BATT} +0.7 volt, the V_{BATT} pin will be internally connected to the V_{DD} pin. When the voltage on V_{SYS} rises a threshold above (~ 0.7 V) the voltage on V_{BATT}, the connection from V_{BATT} to the V_{DD} pin is opened. When the "LINE" input is used as the frequency source, V_{BATT} may be tied to V_{DD} or V_{SS}. The "XTAL IN" pin must be at V_{SS} if V_{BATT} is at V_{SS}. If V_{BATT} is connected to V_{DD}, the "XTAL IN" pin can be tied to V_{SS} or V_{DD}.

XTAL IN, XTAL OUT—These pins are connected to a 32,768-Hz, 1.048576-MHz, 2.097152-MHz or 4.194304-MHz crystal. If an external clock is used, it should be connected to "XTAL IN" with "XTAL OUT" left open.

V_{DD}—The positive power-supply pin.

CDP68HC68T1

REGISTERS

CLOCK CONTROL REGISTER (Write/Read) - Address 31H

D7	D6	D5	D4	D3	D2	D1	D0
START $\overline{\text{STOP}}$	LINE $\overline{\text{XTAL}}$	XTAL SEL 1	XTAL SEL 0	50 Hz $\overline{60}$ Hz	CLK OUT 2	CLK OUT 1	CLK OUT 0

CLOCK CONTROL REGISTER

START-STOP—A high written into this bit will enable the counter stages of the clock circuitry. A low will hold all bits reset in the divider chain from 32 Hz to 1 Hz. A clock out selected by bits 0, 1 and 2 will not be affected by the stop function except the 1 and 2-Hz outputs.

LINE-XTAL—When this bit is set high, clock operation will use the 50 or 60-cycle input present at the LINE input pin. When the bit is low, the crystal input will generate the 1-Hz time update.

XTAL SELECT—One of 4 possible crystals is selected by value in these two bits.

0 = 4.194304 MHz
1 = 2.097152 MHz
2 = 1.048576 MHz
3 = 32,768 Hz

50-60 Hz—50 Hz is selected as the line input frequency when this bit is set high. A low will select 60 Hz. The power-sense bit in the Interrupt Control Register must be set low for line frequency operation.

CLOCK OUT—The three bits specify one of the 7 frequencies to be used as the squarewave clock output.

0 = XTAL
1 = XTAL/2
2 = XTAL/4
3 = XTAL/8
4 = Disable (low output)
5 = 1 Hz
6 = 2 Hz
7 = 50 or 60 Hz
XTAL Operation = 64 Hz

All bits are reset by a power-on reset. Therefore, the XTAL is selected as the clock output at this time.

INTERRUPT CONTROL REGISTER

WATCHDOG—When this bit is set high, the watchdog operation will be enabled. This function requires the CPU to toggle the CE pin periodically without a serial-transfer requirement. In the event this does not occur, a CPU reset will be issued. Status register must be read before re-enabling watchdog.

POWER DOWN—A high in this location will initiate a power down. A CPU reset will occur, the CLK OUT and PSE output pins will be set low and the serial interface will be disabled.

POWER SENSE—This bit is used to enable the line input pin to sense a power failure. It is set high for this function. When power sense is selected, the input to the 50/60-Hz prescaler is disconnected. Therefore, crystal operation is required when power sense is enabled. An interrupt is generated when a power failure is sensed and the power sense and Interrupt True bit in the Status Register are set. When power sense is activated, a "0" must be written to this location followed by a "1" to re-enable power sense.

ALARM—The output of the alarm comparator is enabled when this bit is set high. When a comparison occurs between the seconds, minutes and hours time and alarm counters, the interrupt output is activated. When loading the time counters, this bit should be set low to avoid a false interrupt. This is not required when loading the alarm counters. See PIN FUNCTIONS, $\overline{\text{INT}}$ for explanation of alarm delay.

PERIODIC SELECT—The value in these 4 bits will select the frequency of the periodic output. (See Table I).

INTERRUPT CONTROL REGISTER (Write/Read) - Address 32H

D7	D6	D5	D4	D3	D2	D1	D0
WATCHDOG	POWER DOWN	POWER SENSE	ALARM	PERIODIC SELECT			

All bits are reset by power-on reset.

Table I - Periodic Interrupt Output

D0-D3 VALUE	PERIODIC-INTERRUPT OUTPUT FREQUENCY	FREQUENCY TIMEBASE	
		XTAL	LINE
0	Disable		
1	2048 Hz	X	
2	1024 Hz	X	
3	512 Hz	X	
4	256 Hz	X	
5	128 Hz	X	
6	64 Hz	X	
	50 or 60 Hz		X
7	32 Hz	X	
8	16 Hz	X	
9	8 Hz	X	
10	4 Hz	X	
11	2 Hz	X	X
12	1 Hz	X	X
13	Minute	X	X
14	Hour	X	X
15	Day	X	X

STATUS REGISTER (Read Only) - Address 30H

D7	D6	D5	D4	D3	D2	D1	D0
0	WATCHDOG	TEST MODE	FIRST TIME UP	INTERRUPT TRUE	POWER SENSE INTERRUPT	ALARM INTERRUPT	CLOCK INTERRUPT

WATCHDOG - If this bit is set high, the watchdog circuit has detected a CPU failure.

TEST MODE - When this bit is set high, the device is in the TEST MODE.

FIRST-TIME UP - Power-on reset sets this bit high. This signifies that data in the RAM and Clock is not valid and should be initialized.

INTERRUPT TRUE - A high in this bit signifies that one of the three interrupts (Power Sense, Alarm, and Clock) is valid.

POWER-SENSE INTERRUPT - This bit set high signifies that the power-sense circuit has generated an interrupt.

ALARM INTERRUPT - When the seconds, minutes and hours time and alarm counter are equal, this bit will be set high. Status Register must be read before Loading Interrupt Control Register for valid alarm indication after alarm activates.

CLOCK INTERRUPT - A periodic interrupt will set this bit high.

All bits are reset by a power-on reset except the "FIRST-TIME UP" which is set. All bits except the power-sense bit are reset after a read of this register.

CDP68HC68T1

SERIAL PERIPHERAL INTERFACE (SPI)

PIN SIGNAL DESCRIPTION

SCK (Serial Clock Input)* - This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

MOSI (Master Out/Slave In)* - Data bytes are shifted in at this pin, most significant bit (MSB) first.

MISO (Master In/Slave Out) - Data bytes are shifted out at this pin, most signficant bit (MSB) first.

CE (Chip Enable)** - A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state, and disables the output driver at the MISO pin.

* These inputs will retain their previous state if the line driving them goes into a High-Z state.

** The CE input has as internal pull-down device—if the input is in a low state before going to a High Z, the input can be left in a High Z.

TRUTH TABLE

MODE	SIGNAL			
	CE	SCK	MOSI	MISO
DISABLED RESET	L	INPUT DISABLED	INPUT DISABLED	HIGH Z
WRITE	H	CPOL = 1  CPOL = 0	DATA BIT LATCH	HIGH Z
READ	H	CPOL = 1  CPOL = 0	X	NEXT DATA BIT SHIFTED OUT Δ

Δ MISO remains at a High Z until 8 bits of data are ready to be shifted out during a READ. It remains at a High Z during the entire WRITE cycle.

FUNCTIONAL DESCRIPTION

The Serial Peripheral Interface (SPI) utilized by the CDP68HC68T1 is a serial synchronous bus for address and data transfers. The clock, which is generated by the microcomputer, is active only during address and data transfers In systems using the CDP68HC05C4 or CDP68HC05D2, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. A unique feature of the CDP68HC68T1 is that it automatically determines the level of the inactive clock by sampling SCK when CE becomes active (see Fig. 8). Input data (MOSI) is latched internally on the Internal Strobe edge and output data (MISO) is shifted out on the Shift edge, as defined by Fig. 8. There is one clock for each data bit transferred (address as well as data bits are transferred in groups of 8).

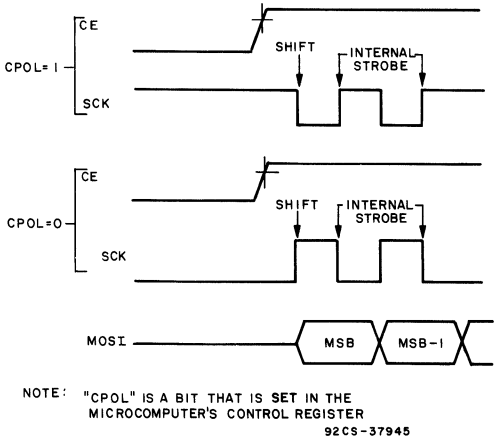


Fig. 8 - Serial RAM clock (SCK) as a function of MCU clock polarity (CPOL).

ADDRESS AND DATA FORMAT

There are three types of serial transfer.

1. Address Control - Fig. 9
2. READ or WRITE Data - Fig. 10
3. Watchdog Reset (actually a non-transfer) - Fig. 11

The Address/Control and Data bytes are shifted MSB first, into the serial data input (MOSI) and out of the serial data output (MISO).

Any transfer of data requires an Address/Control byte to specify a Write or Read operation and to select a Clock or RAM location, followed by one or more bytes of data.

Data is transferred out of MISO for a Read and into MOSI for a Write operation.

ADDRESS/CONTROL BYTE - Fig. 9

It is always the first byte received after CE goes true. To transmit a new address, CE must first go false and then true again. Bit 5 is used to select between Clock and RAM locations.

BIT→	7	6	5	4	3	2	1	0
	$W/\overline{R}$	0	CLK $\overline{RAM}$	A4	A3	A2	A1	A0

0-4	A0-A4	Selects 5-Bit HEX Address of RAM or specifies Clock Register.
5	CLOCK/$\overline{RAM}$	Most Significant Address Bit. If equal to "1", A0 through A4 selects a Clock Register. If equal to "0", A0 through A4 selects one of 32 RAM locations.
6	0	Must be set to "0" when not in Test Mode
7	W/R	W/R = "1" initiates one or more WRITE cycles. W/R = "0", initiates one or more READ cycles.

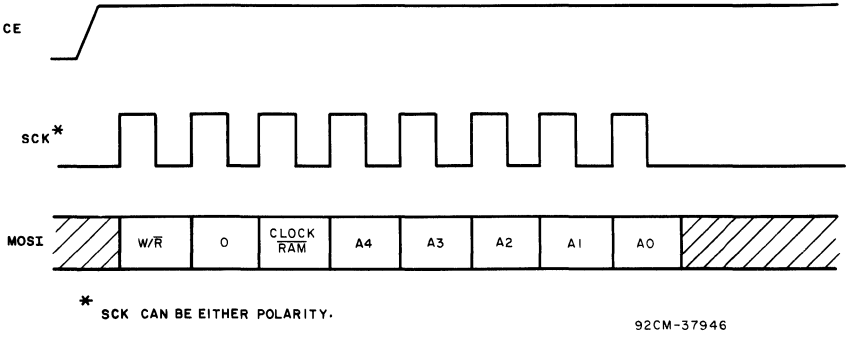


Fig. 9 - Address/Control byte-transfer waveforms.

READ/WRITE DATA - (See Fig. 10)

Read/Write data follows the Address/Control byte.

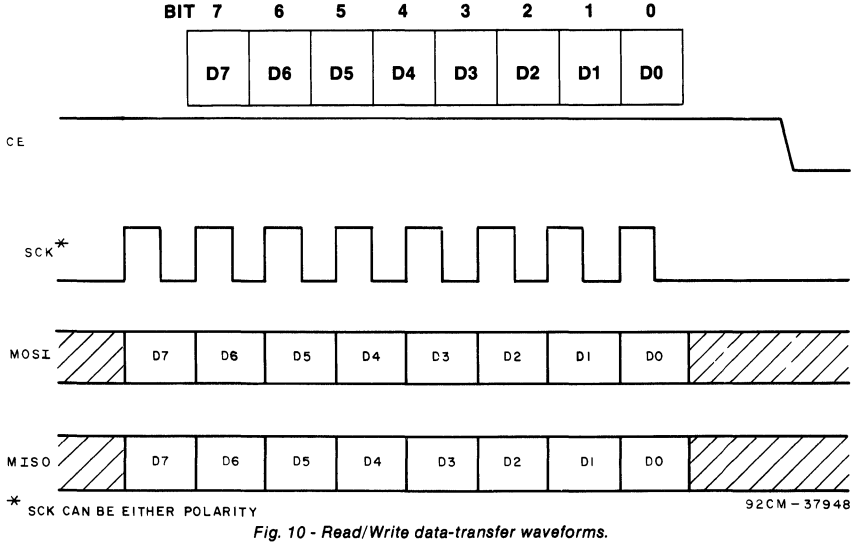


Fig. 10 - Read/Write data-transfer waveforms.

CDP68HC68T1

WATCHDOG RESET - (See Fig. 11)

When watchdog operation is selected, CE must be toggled periodically or a CPU reset will be outputted.

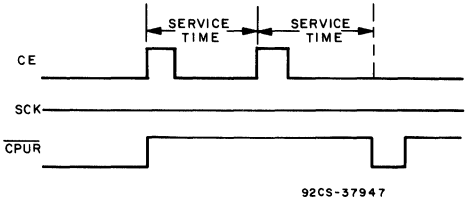


Fig. 11 - Watchdog operation waveforms.

ADDRESS AND DATA

Data transfers can occur one byte at a time (Fig. 12) or in a multibyte burst mode (Fig. 13). After the Real-Time Clock is enabled, an Address/Control word is sent to select the CLOCK or RAM and select the type of operation (i.e., Read or Write). For a single-byte Read or Write, one byte is transferred to or from the clock register or RAM location specified in the Address/Control byte and the Real-Time Clock is then disabled. Write cycle causes the latched clock register or RAM address to automatically increment. Incrementing continues after each transfer until the device is disabled. After incrementing to 1FH the address will "wrap" to 00H and continue. Therefore, when the RAM is selected the address will "wrap" to 00H and when the clock is selected the address will "wrap" 20H.

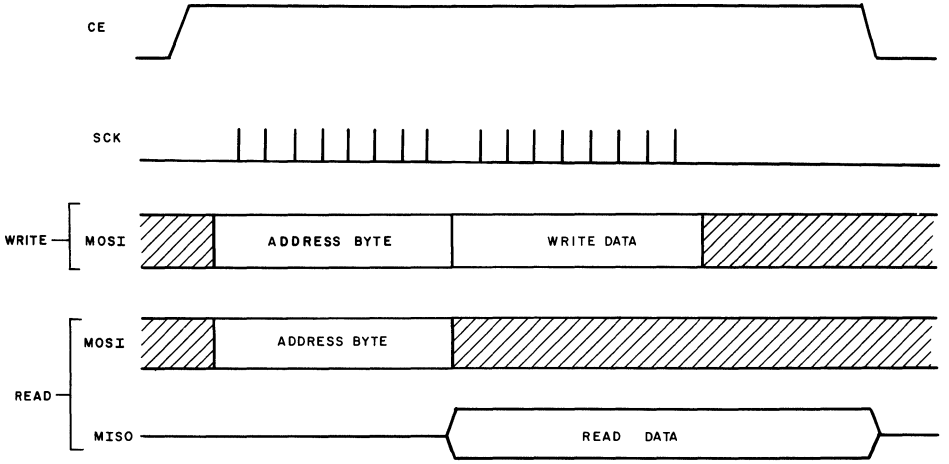


Fig. 12 - Single-byte transfer waveforms.

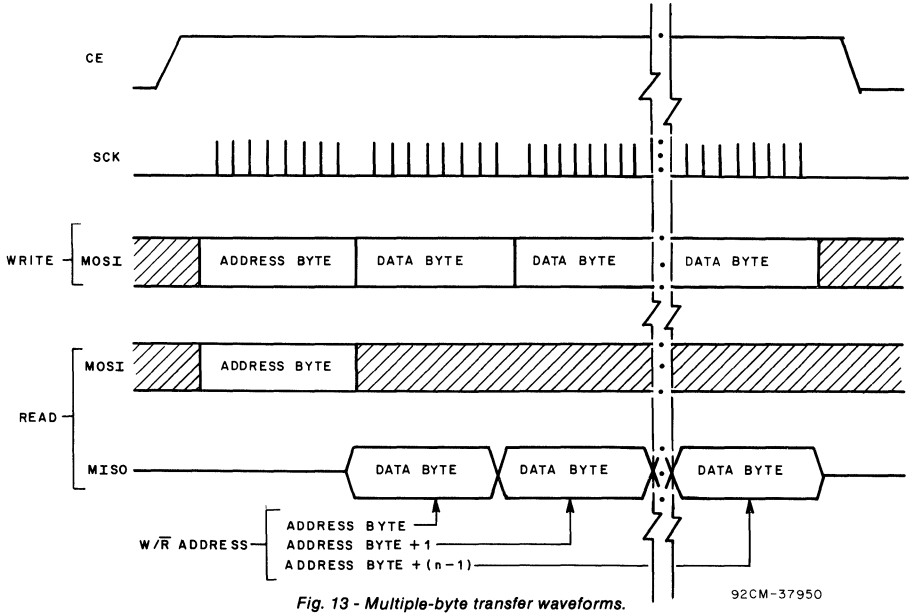


Fig. 13 - Multiple-byte transfer waveforms.

DYNAMIC CHARACTERISTICS

DYNAMIC ELECTRICAL CHARACTERISTICS-BUS TIMING V_{DD} ± 10%, V_{SS} = 0 V dc, T_A = -40° C to +85° C, C_L = 200 pF, see Figs. 14 and 15

IDENT. NO.	CHARACTERISTIC		LIMITS (ALL TYPES)				UNITS
			V_{DD} = 3.3 V		V_{DD} = 5 V		
			Min.	Max.	Min.	Max.	
①	Chip Enable Set-Up Time	t_{EVCV}	200	—	100	—	ns
②	Chip Enable After Clock Hold Time	t_{CVEX}	250	—	125	—	
③	Clock Width High	t_{WH}	400	—	200	—	
④	Clock Width Low	t_{WL}	400	—	200	—	
⑤	Data In to Clock Set-Up Time	t_{DVCV}	200	—	100	—	
⑦	Clock to Data Propagation Delay	t_{CVDV}	—	200	—	100	
⑧	Chip Disable to Output High Z	t_{EXQZ}	—	200	—	100	
⑪	Output Rise Time	t_r	—	200	—	100	
⑫	Output Fall Time	t_f	—	200	—	100	
Ⓐ	Data In After Clock Hold Time	t_{CVDX}	200	—	100	—	
Ⓑ	Clock to Data Out Active	t_{CVQX}	—	200	—	100	
Ⓒ	Clock Recovery Time	t_{REC}	200	—	200	—	

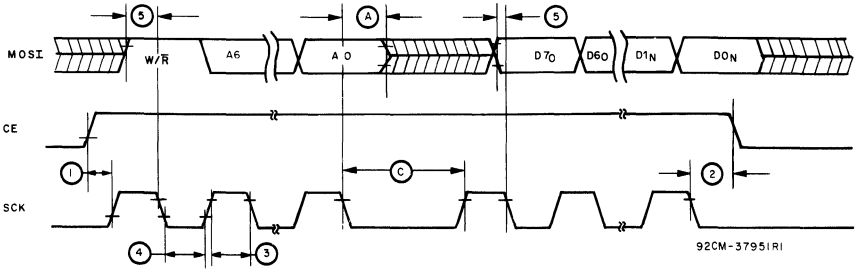


Fig. 14 - WRITE-cycle timing waveforms.

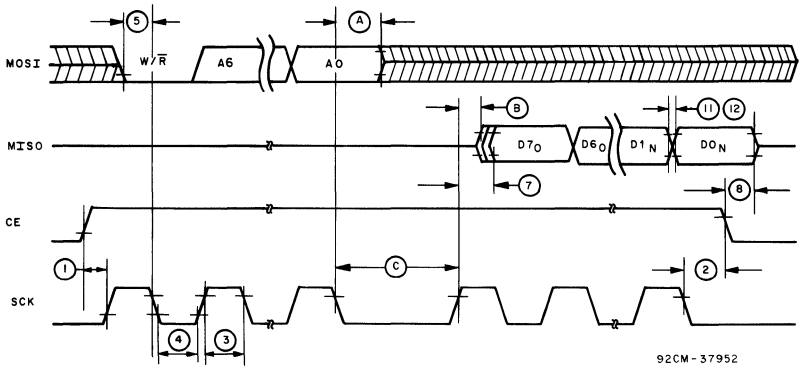
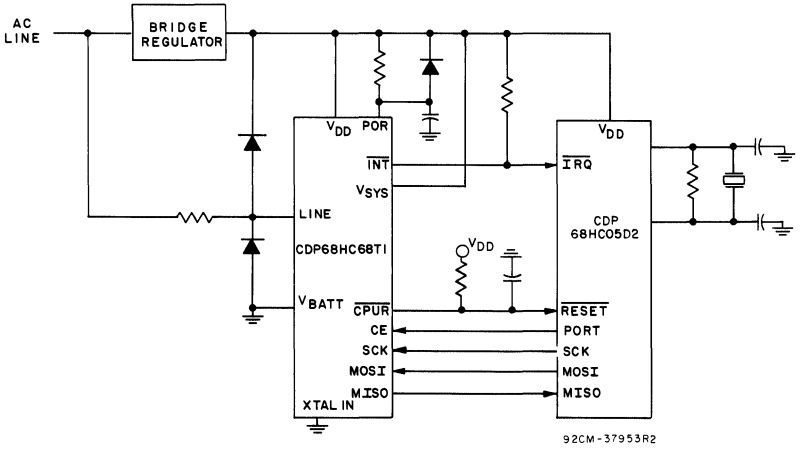


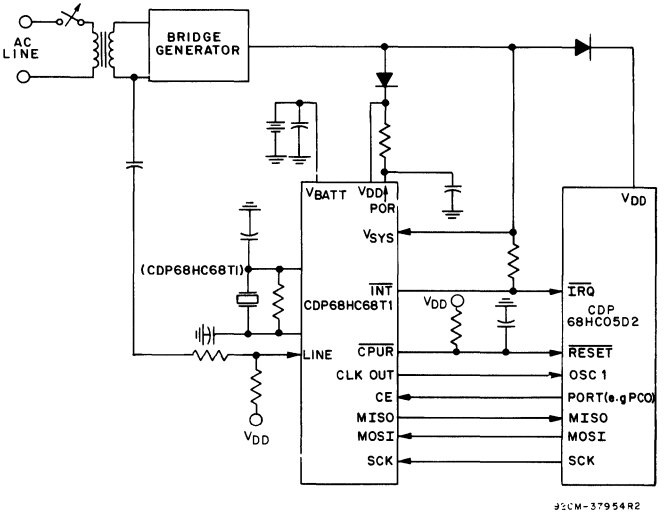
Fig. 15 - READ-cycle timing waveforms.

SYSTEM DIAGRAMS



Example of a system in which power is always on. Clock circuit driven by line input frequency.

Fig. 16 - Power-on always system diagram.



Example of a system in which the power is controlled by an external source. The LINE input pin can sense when the switch opens by use of the POWER-SENSE INTERRUPT. The CDP68HC68T1 crystal drives the clock input to the CPU using the CLK OUT pin. On power down when $V_{SYS} < V_{BATT} + 0.7$ V. V_{BATT} will power the CDP68HC68T1. A threshold detect activates a p-channel switch, connecting V_{BATT} to V_{DD}. V_{BATT} always supplies power to the oscillator, keeping voltage frequency variation to a minimum.

Fig. 17 - Externally-controlled power system diagram.

A Procedure for Power-Down Operation might consist of the following:

1. Set power-sense operation by writing bit 5 high in the Interrupt Control Register.
2. When an interrupt occurs, the CPU reads the status register to determine the interrupt source.
3. Sensing a power failure, the CPU does the necessary housekeeping to prepare for shutdown.
4. The CPU reads the status register again after several milliseconds to determine validity of power failure.
5. The CPU sets power-down bit 6 and disables all interrupts in the Interrupt Control Register when power down is verified. This causes the CPU reset and clock out to be held low and disconnects the serial interface.
6. When power returns and V_{SYS} rises above V_{BATT}, power down is terminated. The CPU reset is released and serial communication is established.

CDP68HC68T1

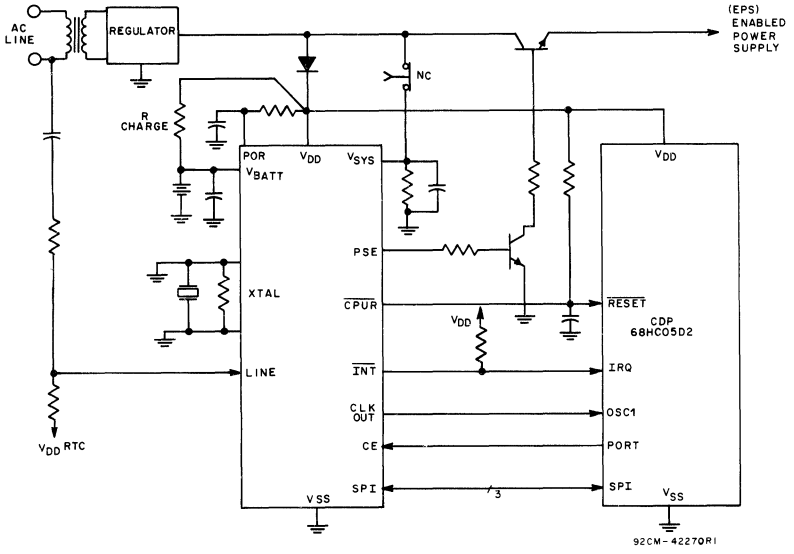
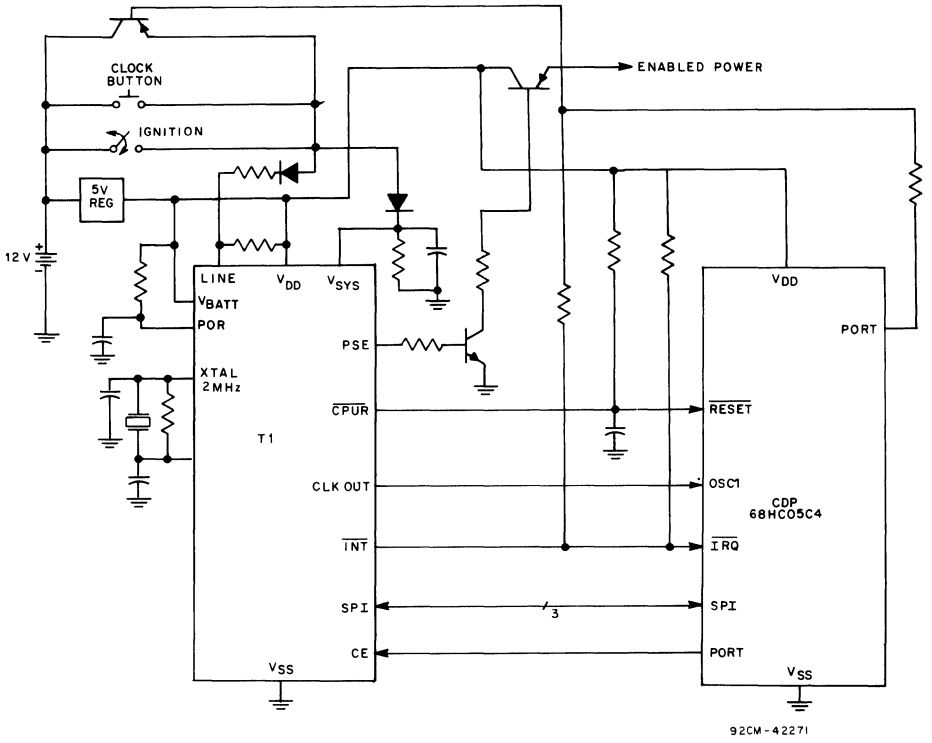


Fig. 18 - Example of a system with a battery back-up.



Example of an automotive system. The V_{SYS} and LINE inputs can be used to sense the ignition turning on and off. An external switch is included to activate the system without turning on the ignition. Also, the CMOS CPU is not powered down with the system V_{DD}, but is held in a low power reset mode during power down. When restoring power the CDP68HC68T1 will enable the CLK OUT pin and set the PSE and CPUR high.

Fig. 19 - Automotive system diagram.

IMPORTANT APPLICATION NOTE:

Those units with a code of 6 PG have delayed alarm interrupts of 8.3 ms regardless of CDP68HC68T1's operating frequency. (See PIN FUNCTIONS, $\overline{INT}$.) In addition, reading the status register before delayed alarm activates will disable alarm signal.