DESCRIPTION

The CE2632 is a mixed signal CMOS monolithic stereo audio ADC for consumer applications.

The ADC is 128-time oversampled. The sampled data are digital filtered and decimated before sent out. A switchabThe ADC utilizes 4-order ΣΔ architecture. The 1–bit ΣΔ converter offers superior differential linearity, with minimum distortion due to component mismatch, and high tolerance to clock jitter. The internal digital filter has a 20K bandwidth. The analog input is 1 vrms corresponding to digital full scale value. The value greater than full scale will be clipped.

FEATURES

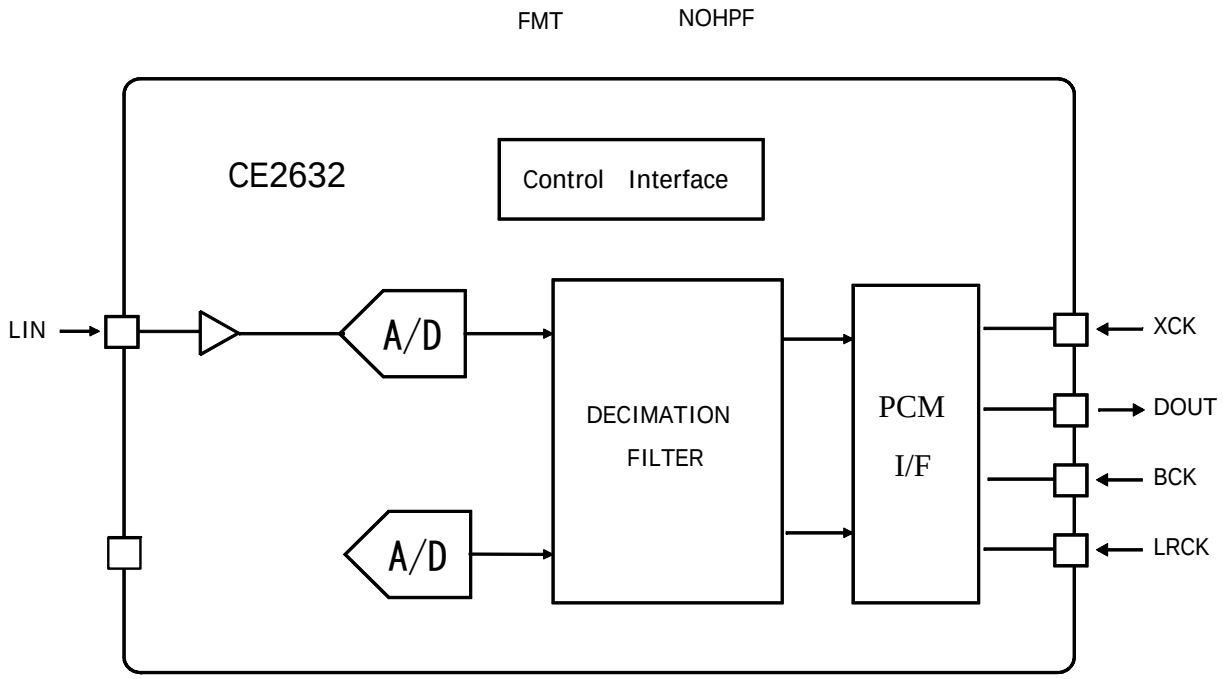
• Stereo Audio ADC.
  - 96dB SNR (A Weighted).
  - -82 dB THD + N Ratio (A Weighted).
  - 32K - 96 KHz. Sampling Rates.
  - 91 dB channel separation.

• I^2S, Left Justified Digital I/F Formats.

• 3.3 Volt Power Supply.

Applications

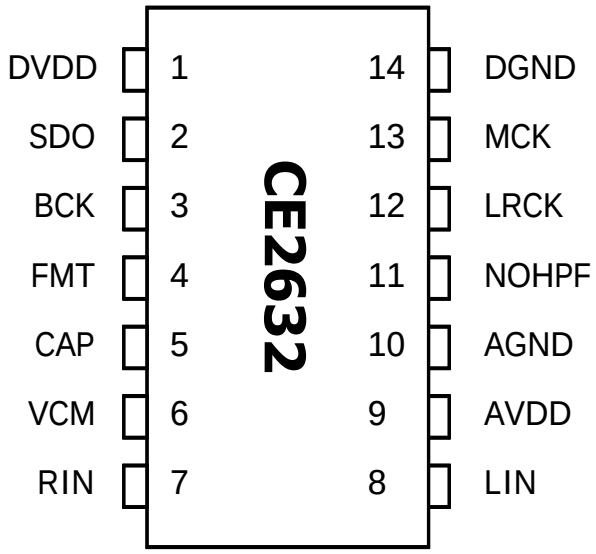
• Digital Surround Sound For Home Theatre
• AV Receiver
• Car Audio.



CE2632 Performance

Item	ADC PERFORMANCE SPECIFICATIONS	Spec.
1	Maximum Input Level	4 Vpp
2	0 dB Audio Input Level	1 Vrms
3	Audio Bandwidth 20Hz - 20 KHz	+/- 0.5 dB
4	SNR (A-weight)	>96 dB
5	THD + NOISE (A-weight, 0 dB input)	< -82 dB
6	Dynamic Range	89 dB
7	Channel Separation	< -90 dB
8	Nonlinear Distortion	< 0.5 dB
9	Channel Gain Error	< 0.5 dB

PIN ASSIGNMENT



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
DVDD	1	3.3 Volt	Analog power supply.
SDO	2	O	Serial audio PCM data output.
BCK	3	I	Audio Serial Data Clock.
FMT	4	I PD	PCM bus format selection. Internal has a 30K pulldown resistor. 1 = left justified. 0 = I^2S
CAP	5	I/O	Reference voltage output. It should be Connected to a 22 uF capacitor in parallel with a 0.1 uF. Signal level is AVDD/2.
VCM	6	I/O	Buffered reference voltage output. It should be Connected to a 22 uF capacitor in parallel with a 0.1 uF. Signal level is AVDD/2.
RIN	7	I	Right channel input.
LIN	8	I	Left channel input
AVDD	9	3.3 Volt	Analog power supply. It should be Connected to a 22 uF capacitor in parallel with a 0.1 uF.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
AGND	10	GND	Analog ground
NOHPF	11	I PD	High pass filter control. Internal has a 30K pulldown resistor. 1 = Disable high pass filter. 0 = Enable high pass filter.
LRCK	12	I	Left/Right channel indicator.
MCK	13	I	External Master Clock Input.
DGND	14	GND	Digital Ground

HIGH PASS FILTER

The processing path contain a switchable high pass filter. The function of this filter is to remove DC offset. The high pass filter can be turn off by tied the NPHPF pin to 'high'.

XCK REQUIREMENT

The CE2632 supports 384 and 256 times sampling clock for 32, 44.1, 48 Khz audio and 192 or 128 times for the 88.2 and 96 Khz audio. There is an clock frequency detection circuit to set up the system clock. .

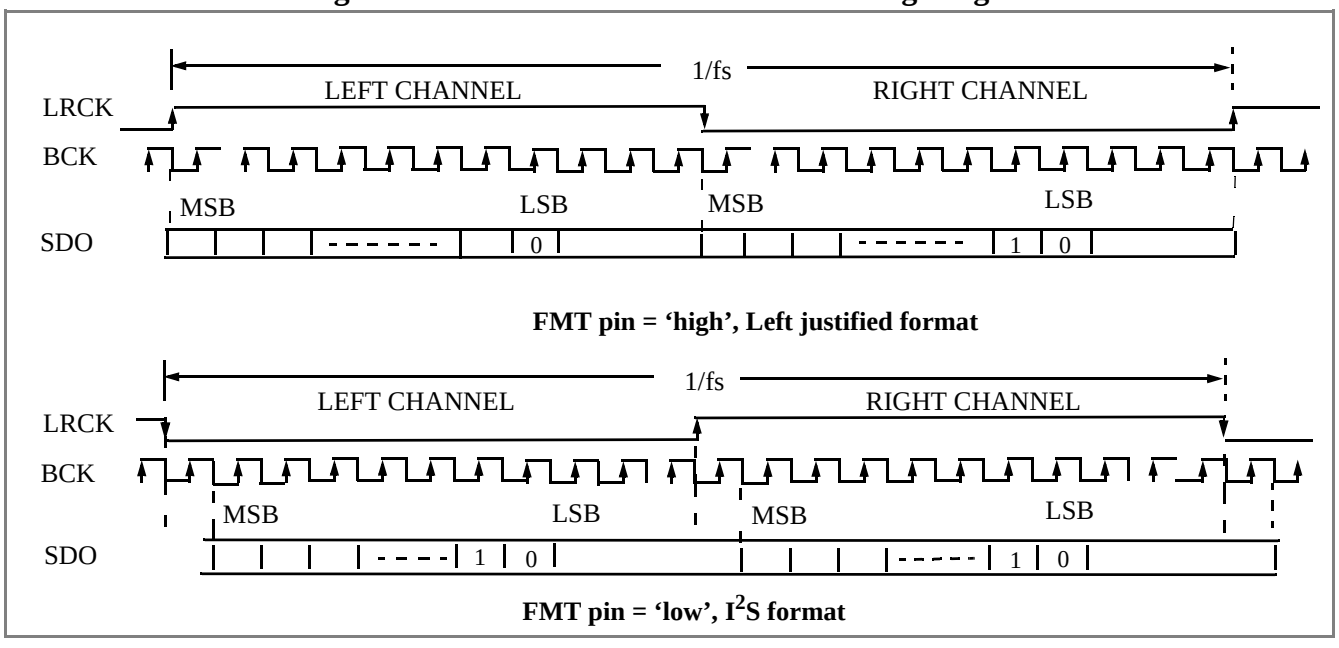
Table (1): XCK Requirement

Sampling Rate	XCK Freq.	
	384*fs	256*fs
32 K	12.288 MHz	8.192 MHz
44.1	16.934 Mhz	11.2896 Mhz.
48 K	18.432 MHz	12.288 Mhz.
96K	36.864 Mhz.	24.576 Mhz

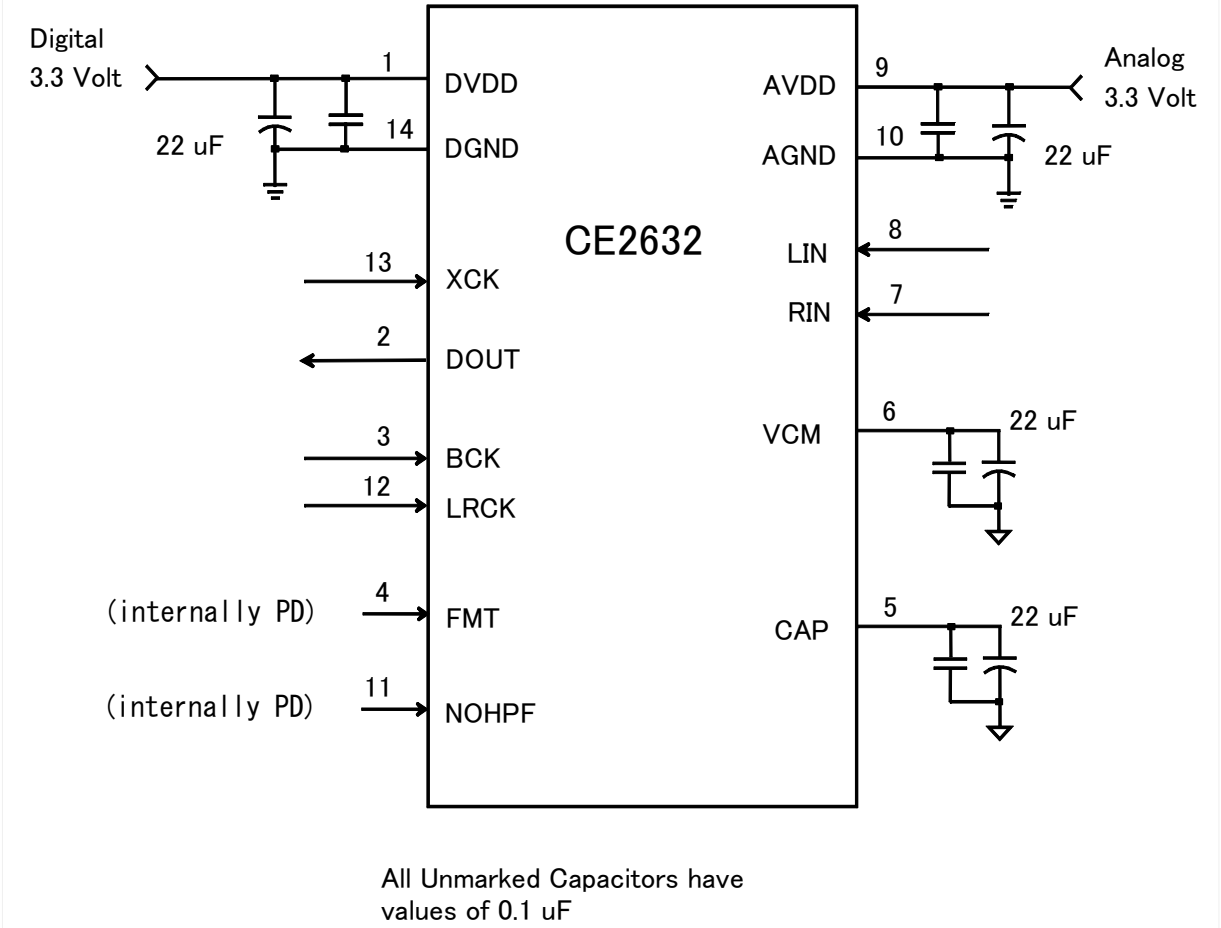
DIGITAL AUDIO SERIAL INTERFACE

The audio serial interface is configured by the FMT pin. When FMT is low I2S format supported. Conversely left justified format is supported. Figure 1 depicted the I2S and left justified formats.

Figure 1. Audio Serial Data Transfer Timing Diagram

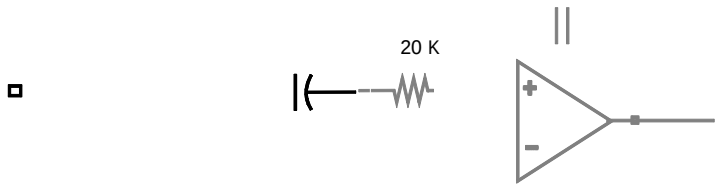


APPLICATION CONNECTION EXAMPLE:



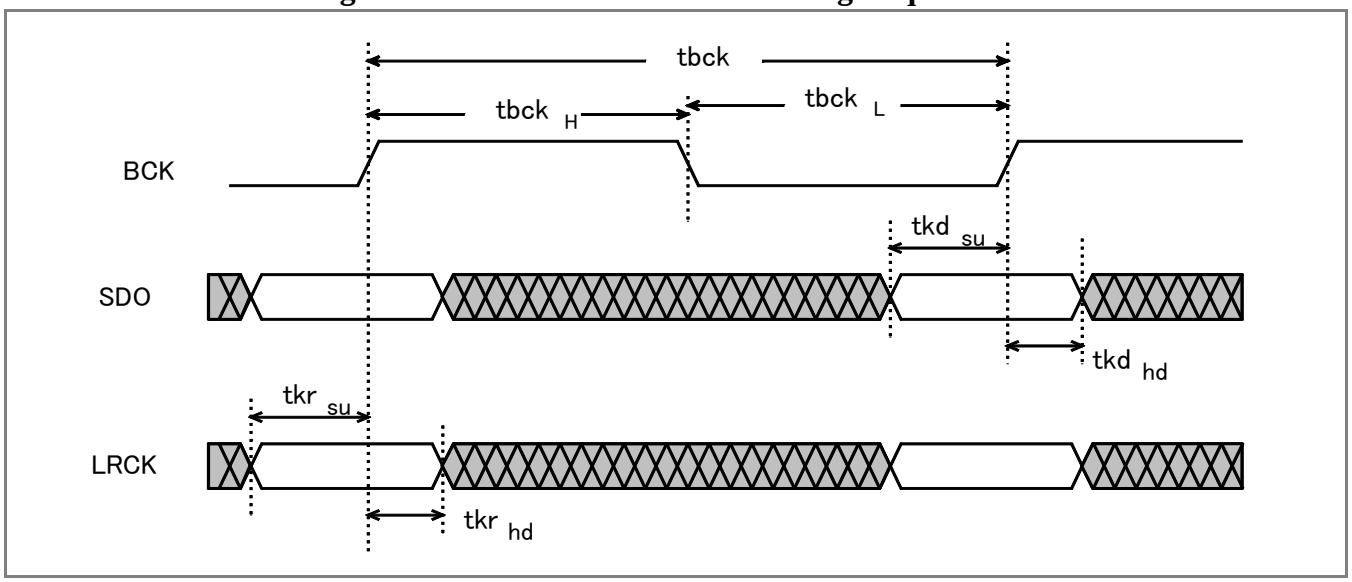
RECOMMENED ADC INPUT CIRCUIT

The ADC converters have a input buffer. The buffers have a equivalent input resistance of 20K ohm. To ensure the performance it is recommended that the applications should have a simple low pass filter to remove the high frequency noise.



TIMING DIAGRAM

Figure 2. Audio Serial Interface Timing Requirement



ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	^oC
T_j	Junction Temperature (Plastic Package)	-65	+150	^oC
Tsol	Lead Soldering Temperature (10 sec., 1/4” from pin)		280	^oC
Tvsol	Vapor Phase Soldering (1 minute)		220	^oC
Tstor	Storage Temperature	-65	+150	^oC

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

ELECTRICAL CHARACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Power Supply					
AVDD	Analog power supply voltage	2.6	3.3	3.6	V
DVDD	Digital power supply voltage	2.6	3.3	3.6	V
I_{DA}	Analog Current		50		mA
I_{DD}	Digital Current		16	18	mA

Audio ADC Characteristics					
	Full Scale Output Voltage to a 10K load	.98	1	1.02	Vrms
V_{VCM}	Reference voltage		VDD/2		V
Vmax	Input Level correspond to Full Scale Digital Output.		1.42		

Digital Characteristics					
V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
I_{OZH}	Hi-Z Leakage Current, HIGH, V_{DD}=Max, V_{IN}=3.3 Volt			33	μ A
I_{OZL}	Hi-Z Leakage Current, LOW, V_{DD}=Max, V_{IN}=$V_{SS)}$			-10	μ A
C_I	Digital Input Capacitance (T^A=25°C, f=1Mhz)			8	pF
C_O	Digital Output Capacitance (T^A=25°C, f=1Mhz)			10	pF

Audio Serial Interface Timing					
tbck	BCK Cycle Time	80			ns
$tbck_H$	BCK Pulse Width, HIGH	30			ns
$tbck_L$	BCK Pulse Width, LOW	30			ns
tkd_{su}	Audio Data Setup Time With Respect To Rising Edge of BCK	10			ns
tkd_{hd}	Audio Data Hold Time With Respect to Rising Edge of BCK	15			ns

Parameter	Characteristics	Min	Typ	Max	Units
tkr_{su}	Audio LRCK Setup Time With Respect To Rising Edge of BCK	10			ns
tkr_{hd}	Audio LRCK Hold Time With Respect To Rising Edge of BCK	15			ns

PACKAGING INFORMATION

Dimensions

	mm.				mm.		
	min	**norm**	**max**		**min**	**norm**	**max**
A	1.35	1.6	1.75	E1	3.8	3.9	4.0
A1	0.1	0.15	0.25	E2	5.8	6.0	6.20
b	0.33	0.406	0.51	e		1.27	
C	0.18	0.203	0.25	L	0.4	0.66	1.27
D	8.56	8.66	8.75				

14-Pin (SOP)