Microelectronics   **CE2826**

6-Channel Audio Codec, 24-bit, 192kHz

DESCRIPTION

The CE2826 is a mixed signal CMOS monolithic audio Codec. It contains six multi-bit sigma delta DAC and a stereo ADC, Ideal for DVD and audio processing application.

The DAC consists of 128-time interpolation filters, 3rd order multi-bit $\Sigma\Delta$ modulators, switch capacitors and analog reconstruction filters. The $\Sigma\Delta$ converter offers superior differential linearity, with minimum distortion due to component mis-match. high tolerance to clock jitter. Additionally it includes separated digital volume control for each channel.

The ADC utilizes cascaded $\Sigma\Delta$ architecture. The internal digital filter has a 20K bandwidth. It support sampling frequency up to 96K Hz.

FEATURES

- Six Channel Audio DAC.
  - 104 dB SNR (A Weighted).
  - -91 dB THD + N Ratio (A Weighted).
  - 32K - 192 KHz. Sampling Rates.
  - On -chip Reconstruction Filters.
  - Independent Digital Volume Control.
- Stereo Audio ADC.
  - Up to 96K sampling Rate.
- I^2S, Left and Right Justified Digital I/F Formats.
- 2-wire Serial Control Interface.
- 3.3 Volt Power Supply.

Applications

- Digital Surround Sound For Home Theatre
- DVD
- Car Audio.
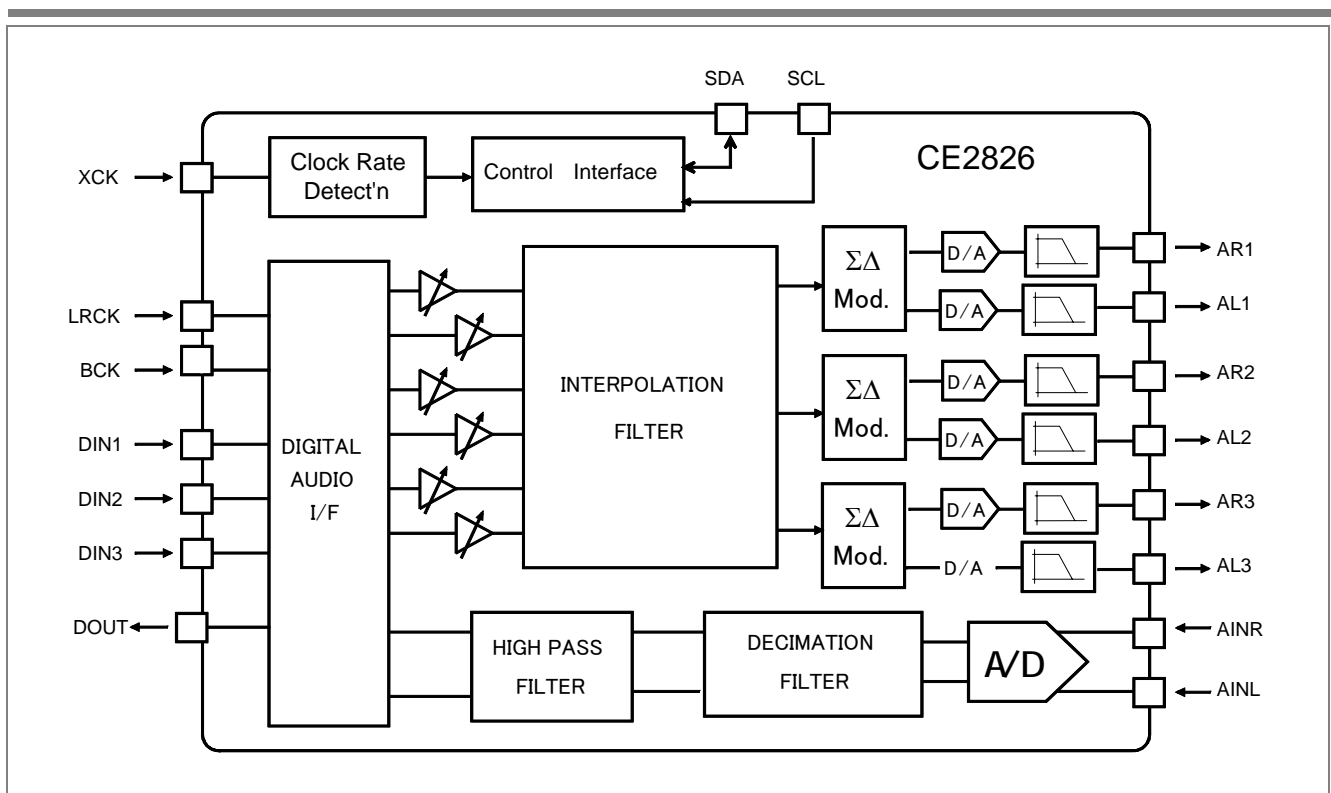
CE2826 Performance

Item	DAC PERFORMANCE SPECIFICATIONS	Spec.
1	Audio Output Level	1 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.1 dB
3	SNR (A-weight)	>104 dB
4	THD + NOISE (A-weight, 0 dB input)	< -91 dB
5	Dynamic Range	94 dB
6	Channel Separation	< -90 dB
7	Nonlinear Distortion	< 0.25 dB
8	Channel Gain Error	< 0.1 dB
	ADC PERFORMANCE SPECIFICATIONS	
1	Maximum Input Level	5 Vpp
2	0 dB Audio Input Level	1 Vrms
3	Audio Bandwidth 20Hz - 20 KHz	+/- 0.5 dB
4	SNR (A-weight)	>94 dB
5	THD + NOISE (A-weight, 0 dB input)	< -88 dB
6	Dynamic Range	91 dB
7	Channel Separation	< -90 dB
8	Nonlinear Distortion	< 0.5 dB
9	Channel Gain Error	< 0.5 dB

All Measurement were taken with only one channel active.

Description (continue)

The DAC support conversion rate from 32K to 192KHz while the ADC from 32K to 96K. The CE2826 support 32, 24, 20 and 16-bit input data. It also support multiple sampling frequency data. Each DAC has its own individual volume control.
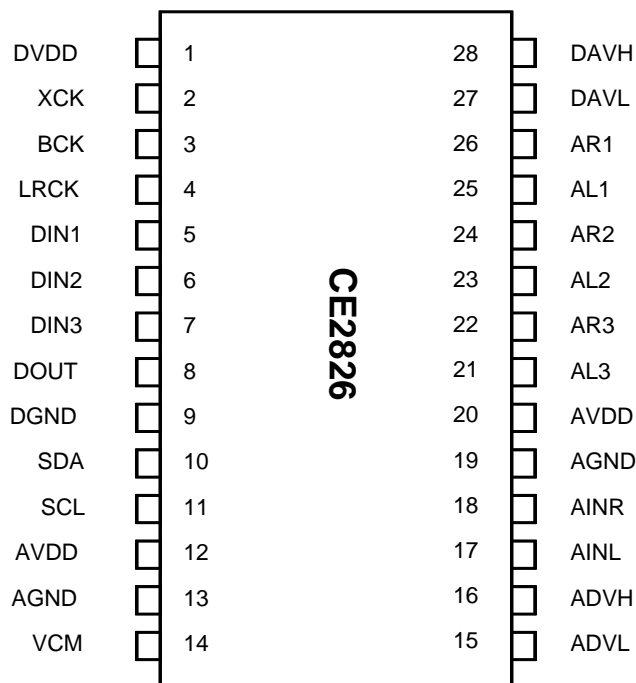
XCK REQUIREMENT

The CE2826 supports 384 and 256 times sampling clock for 32, 44.1, 48, 96 and 192K audio; 192 or 128 times for the 96 K audio.; and 96 and 64 times for the 192K audio. There is an clock frequency detection circuit to set up the system clock normally the user don't need to set the CREG[5:4] registers.

XCK Requirement

Sampling Rate	XCK Freq.					
	CREG1[5:4]=[0 0]		CREG1[5:4]=[0 1]		CREG1[5:4]=[1 0]	
	Normal XCK		2 times XCK		4 times XCK	
fs	384*fs	256*fs	2*384*fs	2*256*fs	4*384*fs	4*256*fs
32 K	12.288 MHz	8.192 MHz				
44.1	16.934 Mhz	11.29 Mhz.				
48 K	18.432 MHz	12.288 Mhz.				
96 K	18.432 MHz	12.288 Mhz.	36.864 MHz	24.576 Mhz.		
192 K	18.432 Mhz	12.288 Mhz.	36.864 Mhz	24.576 Mhz.	73.728 Mhz	49.152 Mhz.

Normal XCK is preferred for all sampling rates.

PIN ASSIGNMENT

```
              DVDD ⊏  1        28  ⊐ DAVH
               XCK ⊏  2        27  ⊐ DAVL
               BCK ⊏  3        26  ⊐ AR1
              LRCK ⊏  4        25  ⊐ AL1
              DIN1 ⊏  5        24  ⊐ AR2
              DIN2 ⊏  6   C    23  ⊐ AL2
              DIN3 ⊏  7   E    22  ⊐ AR3
              DOUT ⊏  8   2    21  ⊐ AL3
              DGND ⊏  9   8    20  ⊐ AVDD
               SDA ⊏ 10   2    19  ⊐ AGND
               SCL ⊏ 11   6    18  ⊐ AINR
              AVDD ⊏ 12        17  ⊐ AINL
              AGND ⊏ 13        16  ⊐ ADVH
               VCM ⊏ 14        15  ⊐ ADVL
```

PIN DESCRIPTION

Pin Name	Pin #	Type	Description
DIGITAL			
DVDD	1	+3.3V	Digital power supply, 3.3 Volt.
XCK	2	I	External Master Clock Input.
BCK	3	I	Audio Serial Data Clock Input.
LRCk	4	I	Left/Right channel clock pin. Please refer to Figure 1, Input data format for its definition
DIN1	5	I	Channel 1 or TDM serial audio data input.
DIN2	6	I	Channel 2 serial audio data input.
DIN3	7	I	Channel 3 serial audio data input.
DOUT	8	O	Serial ADC output
DGND	9	GND	Digital ground
SDA	10	I/O	Serial command port data line.
SCL	11	I	Serial command port clock line.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
Analog			
DAVH	28	+3.3V	DAC positive reference voltage. It should be connected to AVDD with a 22 uF capacitor in parallel with a 0.1 uF.
DAVL	27	GND	DAC negative reference voltage. It should be connected to AGND.
AR1	26	O	Analog right channel 1 output
AL1	25	O	Analog left channel 1 output
AR2	24	O	Analog right channel 2 output
AL2	23	O	Analog left channel 2 output
AR3	22	O	Analog right channel 3 output
AL3	21	O	Analog left channel 3 output
AVDD	20	+3.3V	DAC power supply.
AGND	19	GND	DAC ground pin.
AINR	18	I	ADC right channel input. Input resistance is 20K Ohm
AINL	17	I	ADC left channel input. Input resistance is 20K Ohm
ADVH	16	I	ADC buffered reference voltage output. It should be Connected to a 22 uF capacitor in parallel with a 0.1 uF. Signal level is AVDD/2.
ADVL	15	I/O	Analog negative reference voltage. It should be tied to AGND.
VCM	14	I/O	Analog circuit common mode voltage de-coupling pin.
AGND	13	GND	ADC ground pin.
AVDD	12	+3.3V	ADC power supply

DIGITAL AUDIO SERIAL INTERFACE

The digital serial interface consists of 3 serial input pins, DIN1, DIN2, DIN3, and one serial clock input pin, BCK, and one left/right indicator input pin, LRCK. The data are 2's complement MSB first numbers. The CE2826 supports four resolution, which are selected programming the control register CREG0[5:4] via the I^2C serial control port. Table 1 describes these four resolution.

Table (1): Audio Serial Data Input Resolution,

Format	CREG0[5:4]	DIN[3:1]
0	00	16-bit (default)
1	01	20-bit
2	10	24-bit
3	11	32-bit

The DIN3, DIN2 and DIN1 can be either 24-bit or 32-bit per frame as well as left justified, right justified or I2S. The CE2826 counts the number of BCK per frame to determine whether the input is 24 or 32 bits format.

Table (2): Audio Serial Data Input Modes

Mode	CREG0[7:6]	DIN[3:1]
0	00	Right Justified
1	01	Left Justified
2	10	I2S (default)
3	11	TDM

TDM Input Format

The CE2826 support Time Division Multiplex data input. In this format only one data input pin is required. The six channel data are sent in serial order, channel 1 first, followed by channel 2 and so forth. The number of bits per channel is defined by CREG0[5:4].

Figure 1. Audio Serial Input Data Format
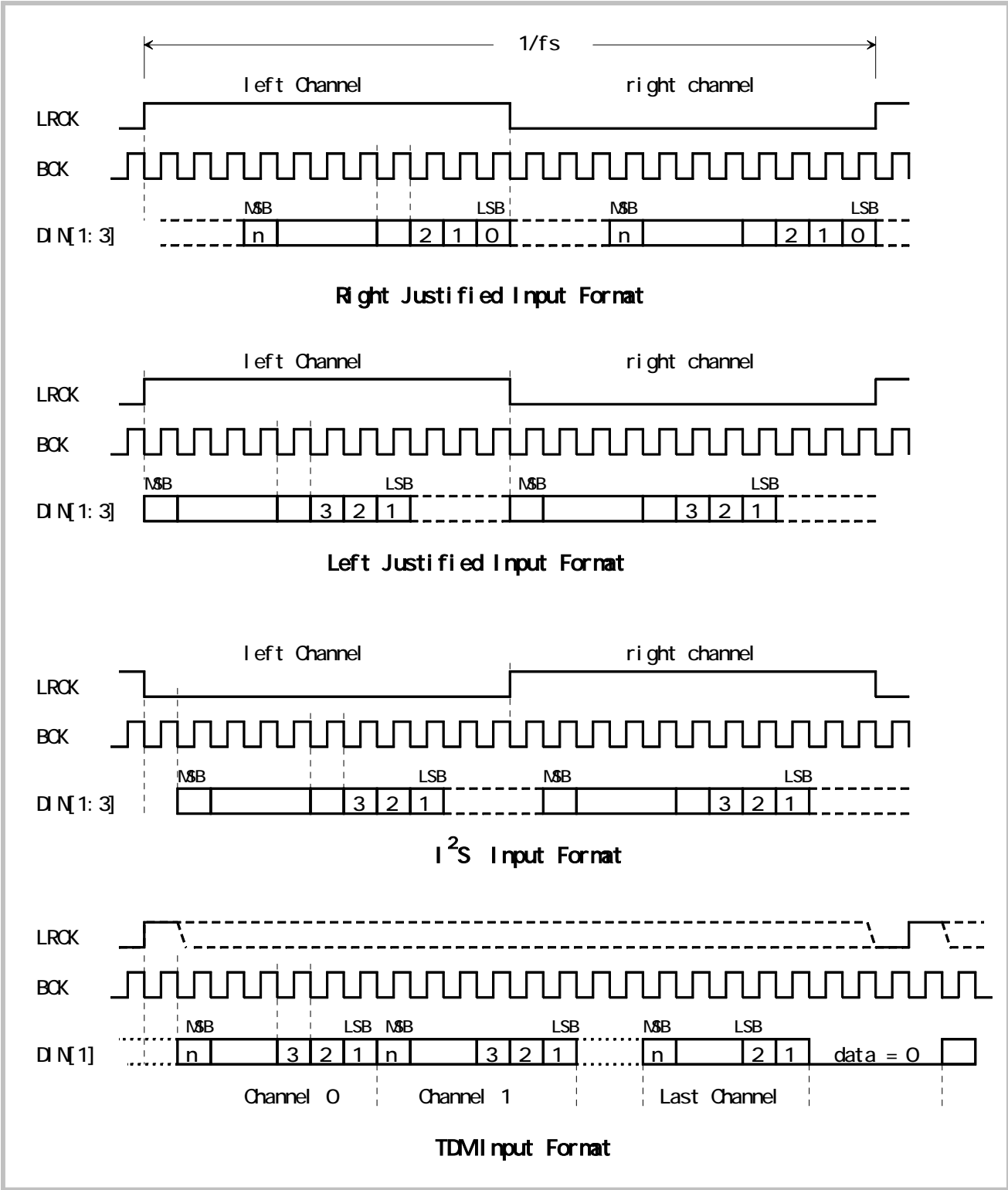
INFINITE ZERO DETECTION

The CE2826 has an Infinite Zero Detection circuit which detects zero in the Audio Serial Port that lasts for approximately 0.1 sec. By default, the zero detection circuit is on.

Serial Command Port

The user can select the chip operation mode by programming the internal control registers through serial I^2C port. The Chip Address for the CE2826 is 35H. The protocol for write operation consists of sending 3 byte data to CE2826, following each byte is the acknowledges generated by CE2826. The first byte is the 7-bit Chip Address followed by the read/write bit (read is high, write is low). The second byte is the control register address. The third byte is the control register data.

Upon power up, all programmable registers are set to default values. Figure 2 describes the serial command port timing relationship.

Figure 2. Serial Command Port Timing

I^2C Bus Control Register Write Example:
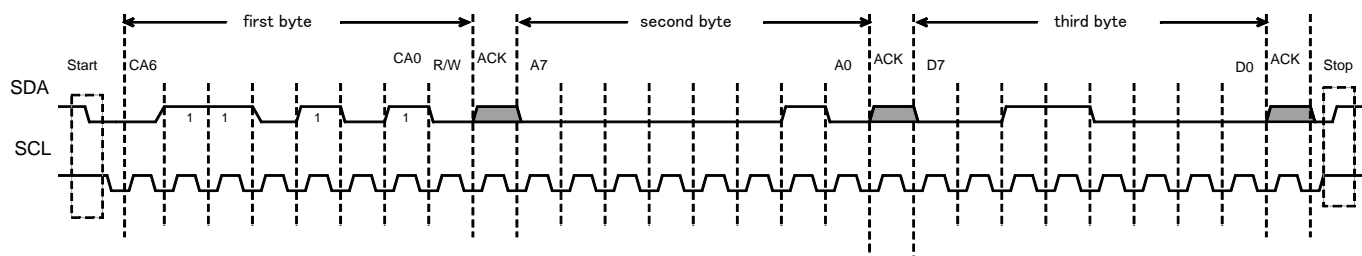
Example

Set channel 1L volume to 30H:

first byte: [CA R/W] = 6AH   (Note: Chip adrress: CA<6:0> = 35H, R/W =0.)

second byte: register address: A<7:0> = 02H

third byte: data D<7:0> = 30H

SERIAL PORT CONTROL REGISTER ASSIGNMENT

There are 8 registers dedicated to the CE2826 for chip functional programming, The register addresses assignments are

Address (decimal)	Register	Default Value	Register Function
0	CREG0[7:0]	80	Data input format, de-emphasis filter selection
1	CREG1[7:0]	80	Input format and PLL output frequency selection
2	VOLREG0[7:0]	80	Volume control for channel 1, left
3	VOLREG1[7:0]	80	Volume control for channel 1, right
4	VOLREG2[7:0]	80	Volume control for channel 2, left
5	VOLREG3[7:0]	80	Volume control for channel 2, right
6	VOLREG4[7:0]	80	Volume control for channel 3, left
7	VOLREG5[7:0]	80	Volume control for channel 3, right

CONTROL REGISTERS DESCRIPTION

Control Register 0(ADRS=hex00, default=hex80)

ADDR[3:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 00	FMT[1:0]		NBIT[1:0]		AMUTE	DEEMP	FSMPL[1:0]	
Default Value	1	0	0	0	0	0	0	0

FMT[1:0] Digital Serial Bus Format Select
    00: - Normal or Right Justified Format.
    01: -Left Justified Format.
    10: - I2S Format.(default)
    11: - TDM, Multi-channel Time Division Multiplex Format

NBIT[1:0]: - These two bits define the serial audio input resolution for right justified and TDM mode
    00: - 16-bit resolution. (default)
    01: - 20-bit resolution.
    10: - 24-bit resolution.
    11: - 32-bit resolution.

AMUTE: - Auto-mute detection enable.
    0: - Auto-mute enabled. (default)
    1: - No auto-mute.

DEEMP: - Enable de-emphasis
    0: - Normal. (default)
    1: - enable de-emphasis.

FSMPL: - Interpolation filter selection.
    These two bits are recognized only when "AUTODET" bit of the CREG1 is set to '0'.
    0X: - 44.1 or 48K sampling.(default)
    10: - 96K sampling.
    11: - 192K sampling.

Control Register 1 (ADRS=hex01, default=hex80)

ADDR[3:0]	CREG1[7:0]							
	BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Hex 01	AUTODET	FS384	CKDIV4	CKDIV2	ADCEN	MUTE56	MUTE34	MUTE12
Default Value	1	0	0	0	0	0	0	0

AUTODET Automatically detects the serial audio input data sampling rate clock frequency.
    0: - do not use auto-detect
    1: - automatically detects the serial audio input data sampling rate and clock frequency.

FS384: 384 fs or 256 fs control for the PLL clock output. This bit is recognized only when "AUTODET" bit is set to '0'
    otherwise the input format is automatically detected.
    0: the PLL takes the reference clock and multiplies it by 2 to generate a 512 bit clock
    1: the PLL takes the reference clock and multiplies it by 4/3 to generate a 512 bit clock

CKDIV4: Clock divider enable control.This bit is recognized only when "AUTODET" bit is set to '0' otherwise the input
    format is automatically detected.
    0: do not enable input clock divided by 4
    1: enable input clock divided by 4

CKDIV2: Clock divider enable control. This bit is recognized only when "AUTODET" bit is set to '0' otherwise the input
    format is automatically detected.
    0: do not enable input clock divided by 2
    1: enable input clock divided by 2

ADCEN: Enable the ADC.
    0: ADC is disabled.
    1: ADC is enabled.

MUTE56: Mute control for channels 5 and 6
    0: do not mute channels 5 and 6
    1: simultaneously mute channels 5 and 6

MUTE34: Mute control for channels 3 and 4
    0: do not mute channels 3 and 4
    1: simultaneously mute channels 3 and 4

MUTE12: Mute control for channels 1 and 2
    0: do not mute channels 1 and 2
    1: simultaneously mute channels1 and2

Volume Registers for channel 1 to channel 3, (ADRS=hex02 - hex07, default=hex80)

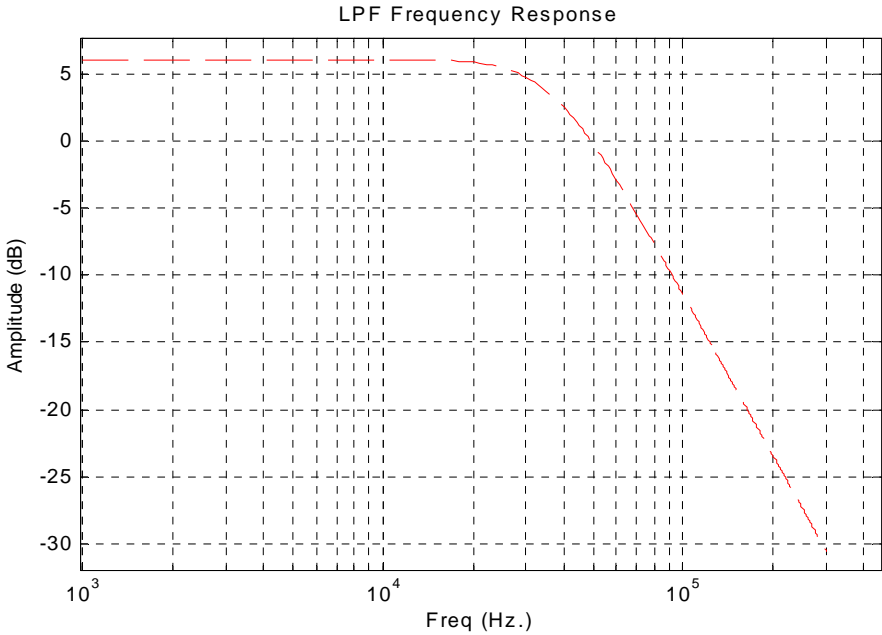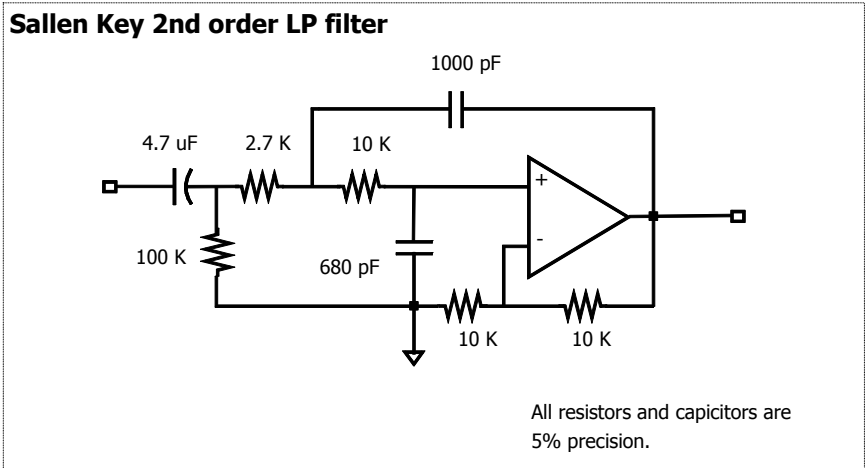| ADDR[3:0]	Volume Registers							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 02	Channel 1 left volume register, VOLREGL1[7:0]							
Hex 03	Channel 1 right volume register, VOLREGR1[7:0]							
Hex 04	Channel 2 left volume register, VOLREGL2[7:0]							
Hex 05	Channel 2 right volume register, VOLREGR2[7:0]							
Hex 06	Channel 3 left volume register, VOLREGL3[7:0]							
Hex 07	Channel 3 right volume register, VOLREGR3[7:0]							
Default Value	1	0	0	0	0	0	0	0

VOLREG:- Control the volume of the 6 DAC's

80h- corresponds to 0 dB setting. Value should not be programed greater than 80h.

SUGGESTED ANALOG RECONSTRUCTION FILTER

A second Sallen Key low pass reconstruction filter is recommend to remove the high frequency sigma delta modulator noise. The filter's component values and characteristic are shown in the following figures.

Sallen Key 2nd order LP filter

1000 pF

4.7 uF   2.7 K   10 K

100 K

680 pF

10 K   10 K

+

-

All resistors and capicitors are
5% precision.

LPF Frequency Response

Amplitude (dB)

Freq (Hz.)

ADC

The ADC converters have a input buffer. The buffers have a equivalent input resistance of 20K ohm. To ensure the performance it is recommended that the applications should have a simple low pass filter to remove the high frequency noise.

Recommended ADC
input circuits

4.7 uF 220 Ohm 20 K 20 K

20 K 0.01uf

VCM ADC
Internal Buffer
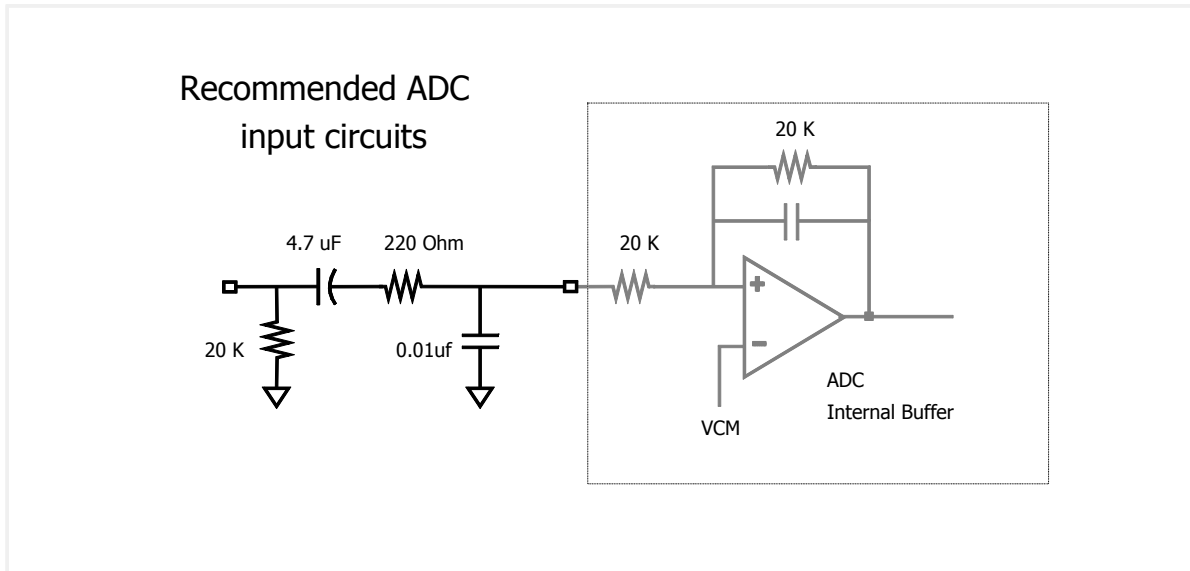
TIMING DIAGRAM

Figure 3. Audio Serial Interface Timing Requirement
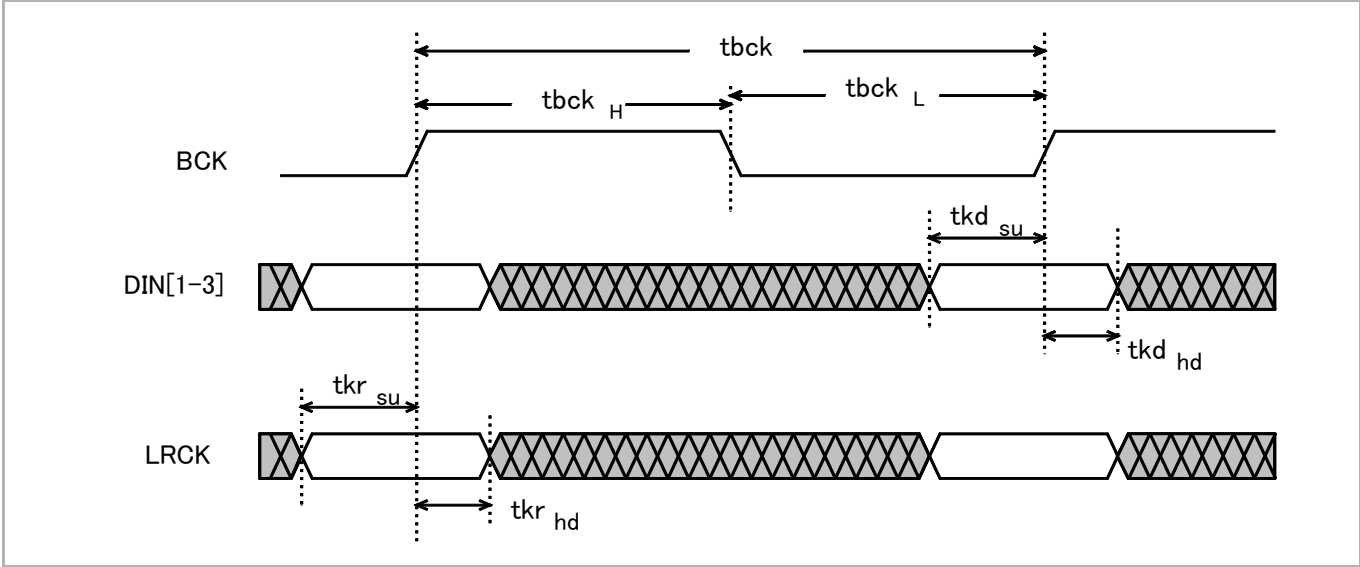
Figure 4. Serial Command Port Write Timing Requirement
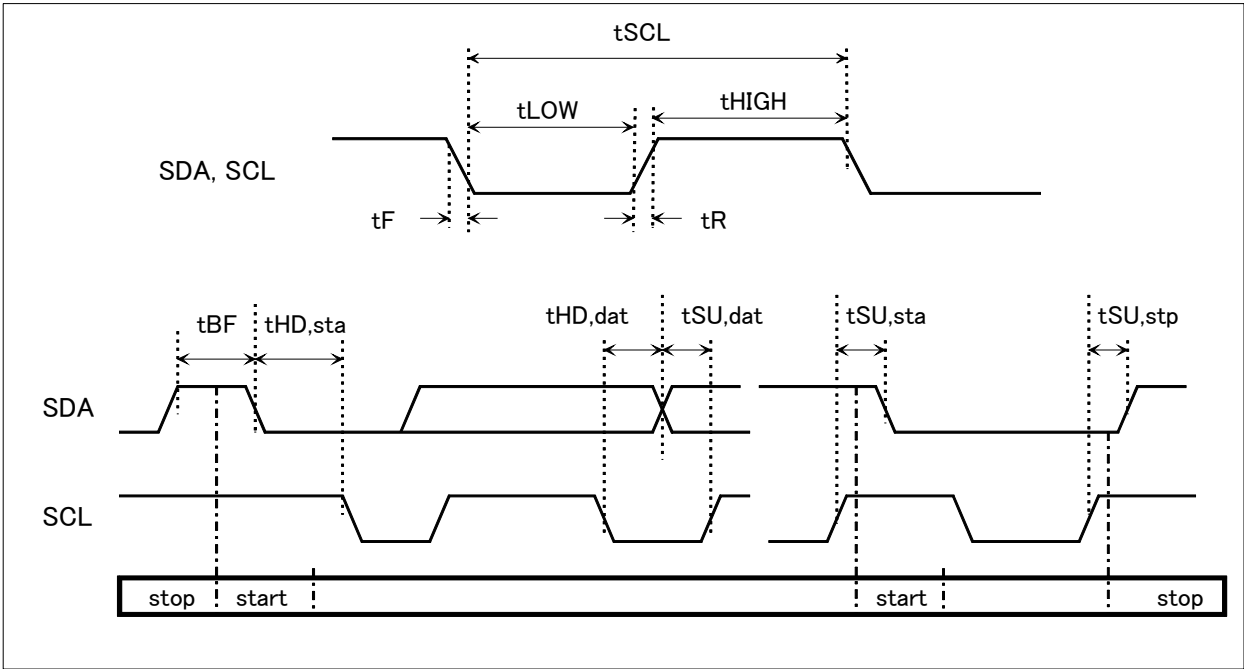
ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	º C
T_j	Junction Temperature (Plastic Package)	-65	+150	º C
Tsol	Lead Soldering Temperature (10 sec., 1/4" from pin)		280	º C
Tvsol	Vapor Phase Soldering (1 minute)		220	º C
Tstor	Storage Temperature	-65	+150	º C

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

ELECTRICAL CHARACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Power Supply					
AVDD	Analog power supply voltage	2.8	3.3	4.0	V
DVDD	Digital power supply voltage	2.8	3.3	4.0	V
I_{DA}	Analog Current		60		mA
I_{DD}	Digital Current		20	18	mA

Audio DAC Characteristics					
	Full Scale Output Voltage to a 10K load	.98	1	1.02	Vrms
V_{VCM}	Reference voltage		VDD/2		V

Digital Characteristics					
V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
I_{OZH}	Hi-Z Leakage Current, HIGH, V_{DD}=Max, V_{IN}=3.3 Volt			33	μ A
I_{OZL}	Hi-Z Leakage Current, LOW, V_{DD}=Max, V_{IN}=$V_{SS)}$			-10	μ A
C_I	Digital Input Capacitance (T^A=25°C, f=1Mhz)			8	pF
C_O	Digital Output Capacitance (T^A=25°C, f=1Mhz)			10	pF

Audio Serial Interface Timing					
tbck	BCK Cycle Time	80			ns
$tbck_H$	BCK Pulse Width, HIGH	30			ns
$tbck_L$	BCK Pulse Width, LOW	30			ns
tkd_{su}	Audio Data Setup Time With Respect To Rising Edge of BCK	10			ns
tkd_{hd}	Audio Data Hold Time With Respect to Rising Edge of BCK	15			ns
tkr_{su}	Audio LRCK Setup Time With Respect To Rising Edge of BCK	10			ns

Parameter	Characteristics	Min	Typ	Max	Units
tkr$_{hd}$	Audio LRCK Hold Time With Respect To Rising Edge of BCK	15			ns

Serial Command Port

fSCL	SCL Clock Frequency			100	kHz
tSU,sta	Start condition set up time	4.7			us
tHD,sta	Start condition hold time	4.0			us
tSU,stp	Stop condition set up time	4.0			us
tLOW	SCL Low time	4.7			us
tHIGH	SCL High time	4.0			us
tR	SCL & SDA rise time			1.0	us
tF	SCL & SDA fall time			0.3	us
tSU,DAT	Data set-up time	250			ns
tHD,DAT	Data hold time	0			ns
tBF	Bus Free time	4.7			us

PACKAGING INFORMATION

Dimensions

	mm.				mm.		
	min	norm	max		min	norm	max
A			2.13	E1	5.0	5.3	5.6
A1	0.05		0.25	E2	7.4	7.8	8.2
b	0.22	0.3	0.38	e		0.65	
C	0.09		0.20	L	0.63	0.9	1.03
D	9.90	10.20	10.50				

28-Pin (SSOP)