■ INTRODUCTION:

The CE3213 series are highly integrated Li-Ion and Li-Pol linear charger management devices, targeted at space limited portable applications.

Furthermore, the CE3213 is specifically designed to work within USB power specifications.

The CE3213 series offers a variety of safety features and functions, while still implementing a complete charging system in a small package.

The battery is charged in three phases: conditioning, constant or thermally regulated current, and constant voltage.

Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature.

Charge is terminated based on minimum current. The CE3213 automatically restarts the charge if the battery voltage falls below an internal threshold; low-power consumption sleep mode is automatically set when the external input supply (wall adapter or USB supply) is removed. Multiple versions of this device family enable easy design of the CE3213 in cradle chargers or in the end equipment, while using low cost or high-end AC adapters.

■ APPLICATIONS：

- Smartphones, PDAs
- Digital Still Cameras
- Portable Media Players
- Portable Navigation Devices
- Bluetooth Applications

■ FEATURES:

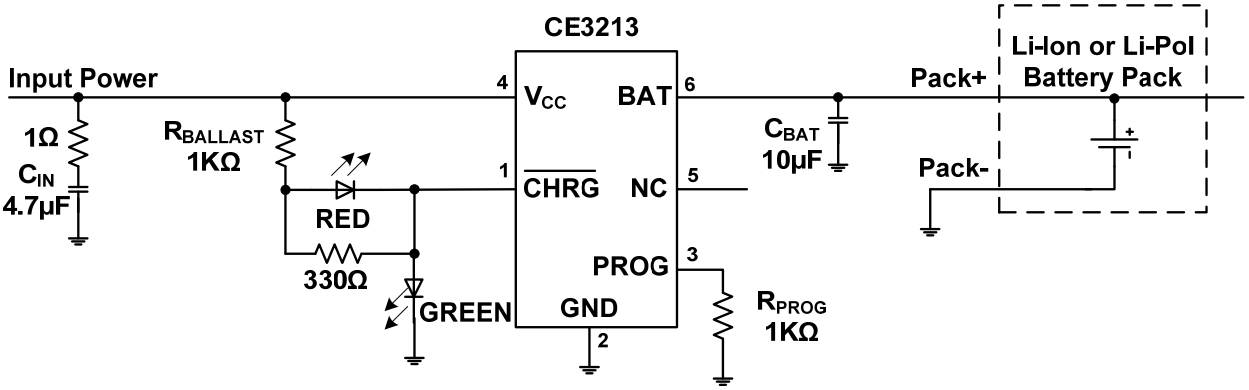
- Internet Appliances
- Low-Power Handheld Devices
- Small 3 mm × 3 mm DFN6 Package
- Ideal for Low-Dropout Designs for Single-Cell Li-Ion or Li-Pol Batteries Charge Directly from USB Port or AC Adapter in Space Limited Portable Applications
- Integrated Power FET and Current Sensor for Up to 1-A Charge Applications
- Reverse Leakage Protection Prevents Battery Drainage
- Integrated Current and Voltage Regulation
- ±1% Voltage Regulation Accuracy
- Charge Termination by Minimum Current
- Precharge Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage of Charge
- Thermal Regulation Maximizes Charge Rate Without Risk of Overheating
- Charge Current Monitor Output for Gas Gauging
- Status Output for LED or System Interface Indicates Charge and Fault Conditions
- Battery Insertion and Removal Detection
- Automatic Sleep Mode for Low-Power Consumption
- Short-Circuit Protection
- Soft-Start Limits Inrush Current
- Charge Voltage Options: 4.1V, 4.15V, 4.2V and 4.35

■ ORDER INFORMATION(1)

Device No.	Package	Operating free air temperature range
CE3213A410FC6	DFN3X3-6	-40~+85℃
CE3213A415FC6	DFN3X3-6	-40~+85℃
CE3213A420FC6	DFN3X3-6	-40~+85℃
CE3213A435FC6	DFN3X3-6	-40~+85℃

(1) Contact Chipower to check availability of other battery regulation voltage versions or charge termination current versions .

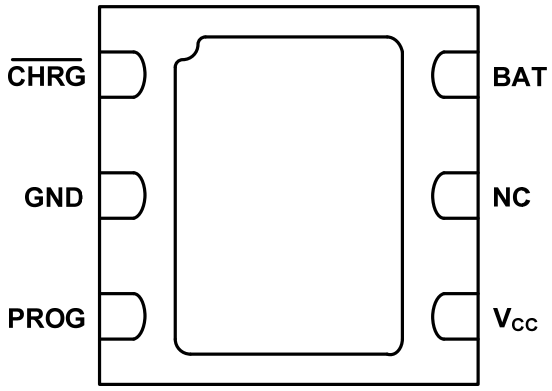
■ TYPICAL APPLICATION CIRCUIT



Typical Application for Charging Between 100mA and 1A

Figure 1. Standard Application Circuit

■ PIN CONFIGURATION



DFN3X3-6(Top View)

Table 1. DFN3X3-6 Pin Description

PIN		TYPE(1)	DESCRIPTION AND REQUIRED COMPONENTS
No.	NAME		
1	$\overline{CHRG}$	O	**Open Drain Charge Status Output**. When the battery is being charged, the $\overline{CHRG}$ pin is pulled low by an internal switch, otherwise $\overline{CHRG}$ pin is in high impedance state.
2	GND	I	**Ground Terminal**.
3	PROG	O	**Constant Charge Current Setting, Charge Current Monitor and Shutdown Pin**. The charge current is set by connecting a 1% accuracy metal film resistor R_{PROG} from this pin to GND. When in pre-conditioning mode, the PROG pin voltage is regulated to 0.1V. When in constant charge current mode, the PROG pin voltage is regulated to 1V.In all modes during charging, the voltage on PROG pin can be used to measure the charge current as the following formula: $I_{BAT}=1000V_{PROG}/R_{PROG}$ The PROG pin can also be used to shut down the charger. Disconnecting the program resistor from ground allows a 3μA current to pull the PROG pin high, the charger enters shutdown mode, charging stops and the input supply current drops to 50μA. Reconnecting R_{PROG} to ground will return the charger to normal operation. **The PROG pin must not be directly shorted to ground at any condition.**
4	V_{CC}	I	**Charge Input Voltage and Internal Supply**. V_{CC} is the power supply to the internal circuit. V_{CC} can range from 4.35V to 6.5V and should be bypassed with at least a 4.7μF capacitor. When V_{CC} drops to within 100mV of the BAT pin voltage, CE3213 enters low power sleep mode, dropping BAT pin's current to less than 2μA.
5	NC		**Not Connect**
6	BAT	I/O	**Charger Power Stage Output and Battery Voltage Sense Input**. BAT pin provides charge current to the battery and regulates the final float voltage. Connect the positive terminal of the battery to BAT pin. Bypass BAT to GND with 10μF to 47μF capacitor. BAT pin draws less than 2μA current in chip disable mode or in sleep mode.
7	Thermal PAD		**Exposed Thermal Paddle (bottom)**. There is an internal electrical connection between the exposed thermal pad and GND pin of the device. The exposed thermal pad must be connected to the same potential as the GND

			pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times. This pin should be connected to a continuous analog ground plane as close as to the device by 2x3 via matrix directly under the CE3213 for electrical contact and rated thermal performance. It dissipates the heat from the IC.

(1) I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS

(unless otherwise specified , T_A=25°C)(1)

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage(2)	V_{CC}	V_{SS}-0.3~V_{CC}+7	V
BAT, PROG Pin Voltage(2)		V_{SS}-0.3~V_{CC}+0.3	
$\overline{CHRG}$ Pin Voltage(2)		V_{SS}-0.3~V_{CC}+0.3	
BAT Short-Circuit Duration	-	Continuous	-
BAT Pin Output Current (Continuous)	I_{BAT}	1.2	A
Output sink current	$I_{\overline{CHRG}}$	10	mA
Junction Temperature	T_j	-40~150	°C
Storage Temperature	T_{stg}	-40~+125	°C
Lead Temperature (Soldering, 10s)	T_{solder}	260	°C
ESD rating(3)	HBM JESD22-A114A	4	kV
	MM JESD22-A115A	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input voltage range(1)	V_{CC}	4.35	6.5	V
BAT Pin Output Current (Continuous)	I_{BAT}		1(2)	A
Operating junction temperature range	T_j	0	125	°C
Fast-charge current programming resistor(3)	R_{PROG}	1	10	kΩ

(1) If V_{CC} is between UVLO and 4.35V, and above the battery voltage, then the IC is active (can deliver some charge to the battery), but the IC will have limited or degraded performance (some functions may not meet data sheet specifications). The

battery may be undercharged (V_{FLOAT} less than in the specification), but will not be overcharged (V_{FLOAT} will not exceed specification).

(2) The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.

(3) Use a 1% tolerance metal film resistor for R_{PROG} to avoid issues with the R_{PROG} short test when using the maximum charge current setting.

■ DISSIPATION RATINGS(1)

PACKAGE	θ_{JA}	T_A<40℃ POWER RATING	DERATING FACTOR ABOVE T_A=40℃
DFN3X3-6	55°C /W	1.5W	0.025W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

■ ELECTRICAL CHARACTERISTICS

Over recommended operating, T_j = 0~125°C range, typical values are tested at V_{CC}=5V and T_A=25°C, maximum and minimum values are guaranteed over 0°C to 85°C Ambient Temperature with a supply voltage in the range of 4.35V to 6.5V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER DOWN THRESHOLD – UNDERVOLTAGE LOCKOUT(UVLO)						
Undervoltage Lockout Threshold(1)	V_{UVL}	V_{CC} Rising : 0V→4V	3.5	3.7	3.9	V
Hysteresis on UVLO	ΔV_{UVL}	V_{CC} Falling: 4V→0V	150	200	300	mV
QUIESCENT CURRENT						
V_{CC} quiescent current, Charge on Mode	$I_{CC(CHGON)}$	R_{PROG}=1kΩ		150	500	μA
V_{CC} quiescent current, Charge Done Mode	$I_{CC(DONE)}$	Charge Terminated		50	100	μA
V_{CC} quiescent current, Shutdown Mode	$I_{CC(SHDN)}$	R_{PROG} Not Connected or V_{CC}<V_{UVL}		50	100	μA
V_{CC} quiescent current, Sleep Mode	$I_{CC(SLP)}$	V_{UVL} < V_{CC} < V_{BAT} + $V_{(SLP\_EXIT)}$		50	100	μA
Battery leakage current into BAT pin, Charge Done Mode	$I_{BAT(DONE)}$	Charge Terminated, V_{BAT}=V_{FLOAT}	0	-2.5	-6.0	μA
Battery leakage current into BAT pin, Shutdown Mode	$I_{BAT(SHDN)}$	R_{PROG} Not Connected		±1	±2	μA
Battery leakage current into BAT pin, Sleep Mode	$I_{BAT(SLP)}$	V_{UVL} < V_{CC} < V_{BAT} + $V_{(SLP\_EXIT)}$ or V_{CC} Floating		±1	±2	μA
VOLTAGE REGULATION, V_{CC}≥V_{FLOAT}+$V_{(DO-MAX)}$, I_{BAT}> I_{TERM}, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED						

Regulated Output (Float) Voltage	V_{FLOAT}	0°C ≦ T_A ≤ 85°C, I_{BAT} = 20mA, R_{PROG}=10kΩ	-1		+1	%
Dropout voltage, V_{CC} – V_{BAT}	$V_{(DO)}$	I_{BAT}=1A		400	750	mV
CURRENT REGULATION, V_{CC}≥V_{BAT}+$V_{(DO-MAX)}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED						
Fast Charge Current Range	I_{CHG}	V_{BAT} > V_{TRIKL}, I_{CHG}= K_{PROG} x V_{PROG} /R_{PROG}	0.1		1.0	A
Fast Charge Current Set Voltage	V_{PROG}	R_{PROG} = 1kΩ, Current Mode	0.9	1.0	1.1	V
Fast Charge Current set factor	K_{PROG}	100mA ≤I_{CHG}≤1000mA $\frac{mA * k\Omega}{Volts}$		1000		
External resistor range	R_{PROG}	Resistor connected to PROG pin	1		10	kΩ
Fast Charge Current in typical application		R_{PROG} = 1kΩ, V_{BAT}=4.0V Current Regulation Mode	950	1000	1050	mA
		R_{PROG} = 2kΩ, V_{BAT}=4.0V Current Regulation Mode	450	500	550	mA
PROG Pin Pull-Up Current	I_{PROG}			3		μA

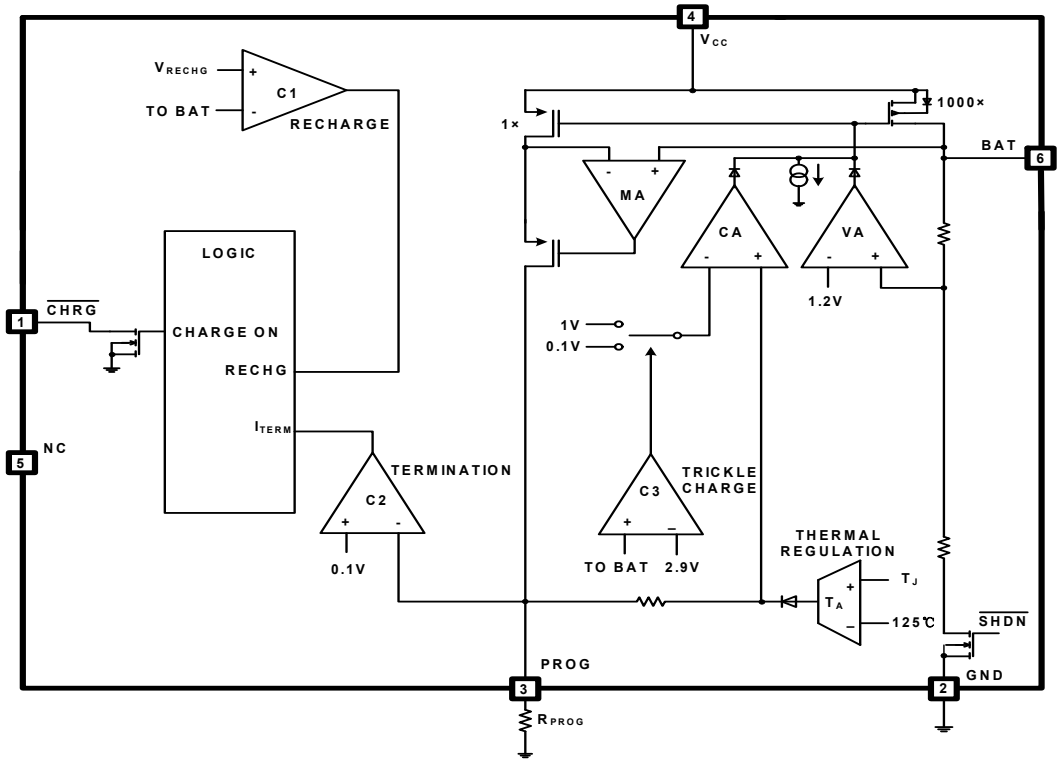
(1) Specified by design, not production tested.

PRECHARGE AND OUTPUT SHORT-CIRCUIT CURRENT REGULATION, V_{CC}–V_{BAT} > $V_{(DO-MAX)}$, V_{CC}≥4.35V, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED; Thermal regulation loop not active						
Precharge to fast-charge transition threshold	V_{TRIKL}	R_{PROG} =1kΩ, V_{BAT} Rising	2.8	2.9	3.0	V
Precharge Hysteresis	$V_{(TRIKL-HYS)}$	R_{PROG} = 1kΩ, V_{BAT} Falling	80	100	120	mV
Precharge Current range	$I_{(PRECHG)}$	V_{BAT} < V_{TRIKL}, $I_{(PRECHG)}$= K_{PROG} x V_{PRECHG} /R_{PROG}	8.5		115	mA
Precharge Current set voltage	V_{PRECHG}	Voltage on PROG pin, V_{BAT} < V_{TRIKL}	85	100	115	mV
Precharge Current in typical application		V_{BAT} < V_{TRIKL}, R_{PROG}=1kΩ	90	100	110	mA
Battery shorted regulation current	$I_{BAT(SHORT)}$	BAT=GND, R_{PROG}=1kΩ	90	100	110	mA
TEMPERATURE REGULATION (Thermal regulation), CHARGER ENABLED, NO FAULT CONDITIONS DETECTED						
Temperature regulation limit	$T_{J(REG)}$	V_{CC}= 5V, V_{BAT}=3.2 V, Fast charge current set to 1A		125		°C
CHARGE TERMINATION DETECTION, V_{BAT}= V_{FLOAT}, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, Thermal regulation LOOP NOT ACTIVE						
C/10 Charge termination detection	I_{TERM}	V_{BAT} > V_{RECHG},	8.5		115	mA

current range		I_{TERM}= K_{PROG} x V_{TERM} /R_{PROG}				
C/10 Charge termination detection set voltage(1)	V_{TERM}	V_{BAT} > V_{RECHG}	85	100	115	mV
Deglitch time, termination detected	$T_{DGL(TERM)}$	I_{BAT} Falling Below I_{CHG}/10	0.8	1.8	4.0	mS
BATTERY RECHARGE THRESHOLD						
Recharge Threshold Detection	$\triangle V_{RECHG}$	V_{FLOAT}－V_{BAT}< $\triangle V_{RECHG}$	60	100	150	mV
Deglitch time, recharge detection	$T_{DGL(RECHG)}$	V_{BAT} Falling	0.8	1.8	4.0	mS
SLEEP COMPARATOR						
Sleep mode entry threshold voltage	V_{SLP}	V_{CC} Falling, V_{UVL} < V_{BAT} ≤ V_{FLOAT}	60	80	100	mV
Sleep mode exit threshold voltage	$V_{(SLP\_EXIT)}$	V_{CC} Rising , V_{UVL} < V_{BAT} ≤ V_{FLOAT}	60	100	140	mV
$\overline{CHRG}$ STATUS OUTPUT						
$\overline{CHRG}$ Pin Low-level Output Voltage	$V_{\overline{CHRG}}$	$I_{\overline{CHRG}}$=5mA (sink current)		0.3	0.6	V
SOFT START						
Soft-Start Time	t_{SS}	I_{BAT}=0 to I_{BAT} =1000V/R_{PROG}		20		μS

(1) The voltage on the PROG pin is compared to the V_{TERM} voltage to determine when the termination should occur.

■ BLOCK DIAGRAM



Future 2. Functional Block Diagram

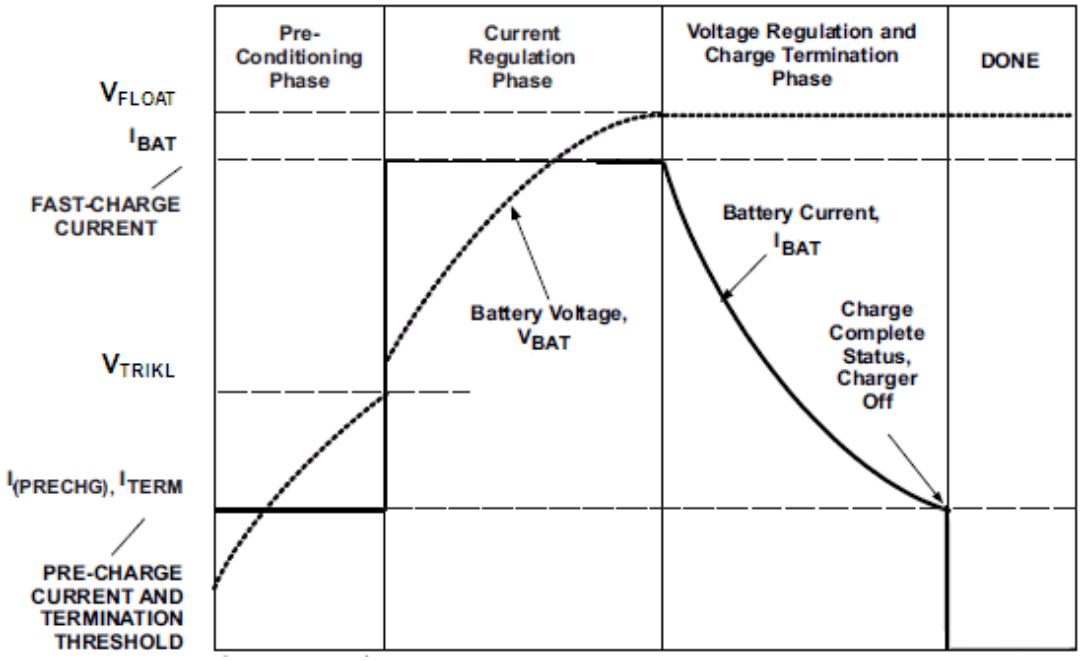
■ FUNCTIONAL DESCRIPTION

The CE3213 series are highly integrated Li-Ion or Li-Pol linear battery chargers, targeted at space-limited portable applications. It operates from either a USB port or Wall Adapter and charges a single-cell Li-Ion or Li-Pol battery with up to 1A of charge current.

The charge current is programmable using external components (R_{PROG} resistor). The charge process starts when an external input power is connected to the system, $V_{CC} > V_{UVL}$, $V_{CC} > V_{BAT} + V_{(SLP\_EXIT)}$, and the BAT pin voltage is below the recharge threshold, $V_{BAT} < V_{RECHG}$.

When the charger is enabled two control loops modulate the battery switch drain to source impedance to limit the BAT pin current to the programmed charge current value (charge current loop) or to regulate the battery voltage to the programmed charge voltage value (charge voltage loop). If $V_{BAT} < V_{TRIKL}$ (2.9 V typical), the BAT pin current is internally set to 1/10th of the programmed fast charge current value in current regulation mode.

A typical charge profile is shown below, for an operation condition that does not cause the IC junction temperature to exceed $T_{J(REG)}$ (125°C typical).



Future 3. Charging Profile With $T_{J(REG)}$

If the operating conditions cause the IC junction temperature to exceed $T_{J(REG)}$, the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop is activated when an internal voltage reference, which is inversely proportional to the IC junction temperature, is lower than a fixed, temperature stable internal voltage. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to $T_{J(REG)}$, effectively regulating the IC junction temperature.

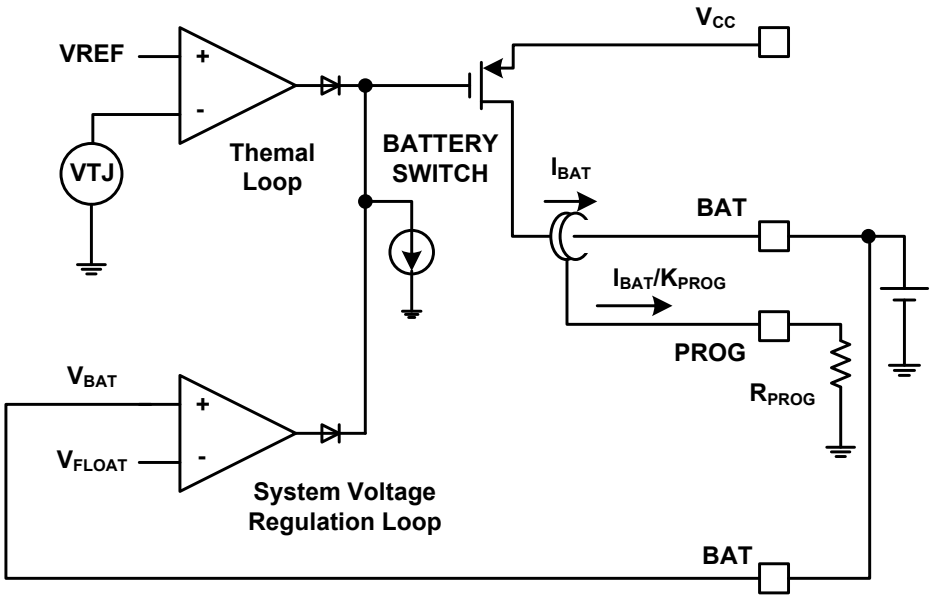


Figure 4. Thermal Regulation Circuit

A modified charge cycle, with the thermal loop active, is shown in Figure 5.

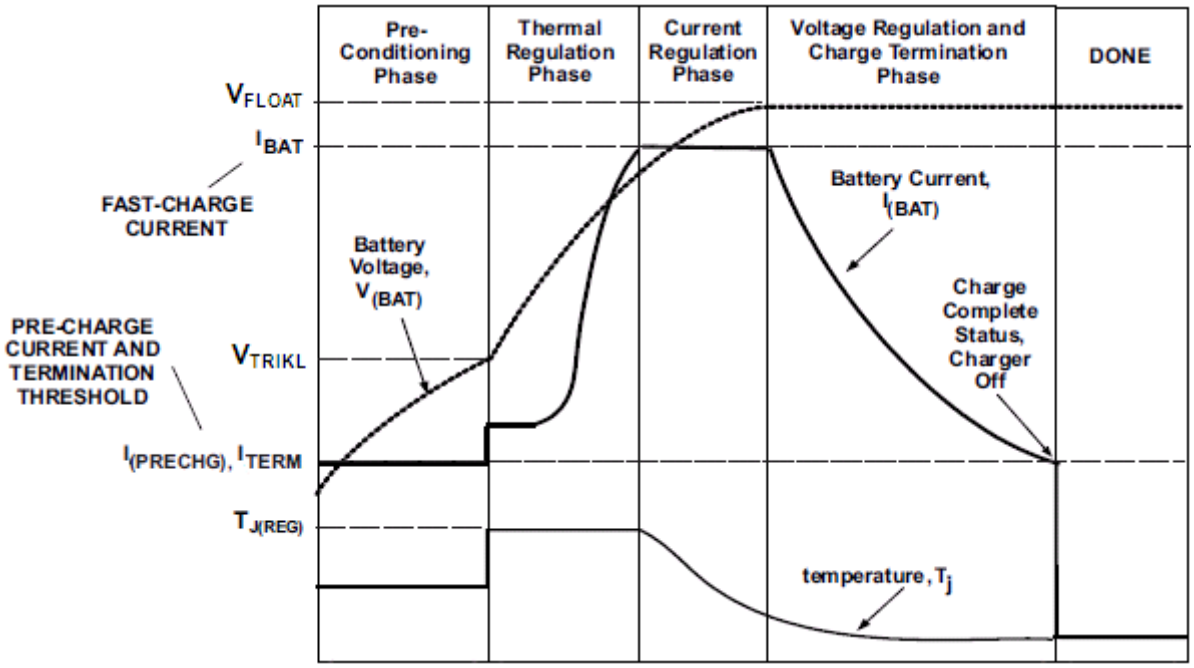


Figure 5. Charge Profile, Thermal Loop Active

■ OPERATING MODES

Power Down (Undervoltage Lockout, UVLO)

An internal undervoltage lockout circuit monitors the input voltage, the CE3213 is in a power-down mode when the input power voltage (V_{CC}) is below the power-down threshold (Undervoltage Lockout threshold) V_{UVL}. The UVLO circuit has a built-in hysteresis of 200mV.

During the power down mode, all IC functions are off, and the host commands at the control pins are not interpreted. The integrated power MOSFET connected between V_{CC} and BAT pins is off, the status output pin $\overline{CHRG}$ is set to the high impedance state.

Sleep Mode

The CE3213 enters the low-power sleep mode when the input power voltage (V_{CC}) is above the power down threshold (Undervoltage Lockout threshold) V_{UVL} but still lower than the sleep mode exit threshold, $V_{CC} < V_{BAT} + V_{(SLP\_EXIT)}$. During the sleep mode, the charger is off, and the host commands at the control pins are not interpreted. The integrated power MOSFET connected between V_{CC} and BAT pins is off, the status output pin $\overline{CHRG}$ is to the high impedance state.

The sleep mode is entered from any other state, if the input power (V_{CC}) is not detected. This feature prevents draining the battery during the absence of V_{CC}.

The backgate control circuit prevents any reverse current flowing from the battery to the adapter terminal during the charger off delay time.

Note that the $\overline{CHRG}$ pin is not deglitched, and it indicates input power loss immediately after the input voltage falls below the battery voltage. If the input source frequently drops below the battery voltage and recovers, a small capacitor can be used from $\overline{CHRG}$ to GND to prevent $\overline{CHRG}$ flashing events.

Shutdown Mode

An external host can enable or disable the charging process using a dedicated control N-CH MOSFET. At any point in the charge cycle, the CE3213 can be put into shutdown mode by removing R_{PROG} thus floating the PROG pin. A new charge cycle can be initiated by reconnecting the program resistor.

The quiescent current required in shutdown mode is 50μA typical.

Begin Charge Mode

All blocks in the IC are powered up, and the CE3213 is ready to start charging the battery. A new charge cycle is started when the control logic decides that all conditions required to enable a new charge cycle are met.

Charging Mode

When the charging mode is active, the CE3213 executes the charging algorithm, as described in the operational flow chart, Figure 6.

Battery's absence Mode Operation

This mode is different than a typical LDO since it has different modes of operation, and delivers less current at lower output voltages.

Note that a load on the output prior to powering the device may keep the part in short-circuit mode. Also,

during normal operation, exceeding the programmed fast charge level causes the output to drop, further restricting the output power, and soon ends up in short-circuit mode. Operation with a battery or keeping the average load current below the programmed current level prevents this type of latch up.

STATE MACHINE DIAGRAM

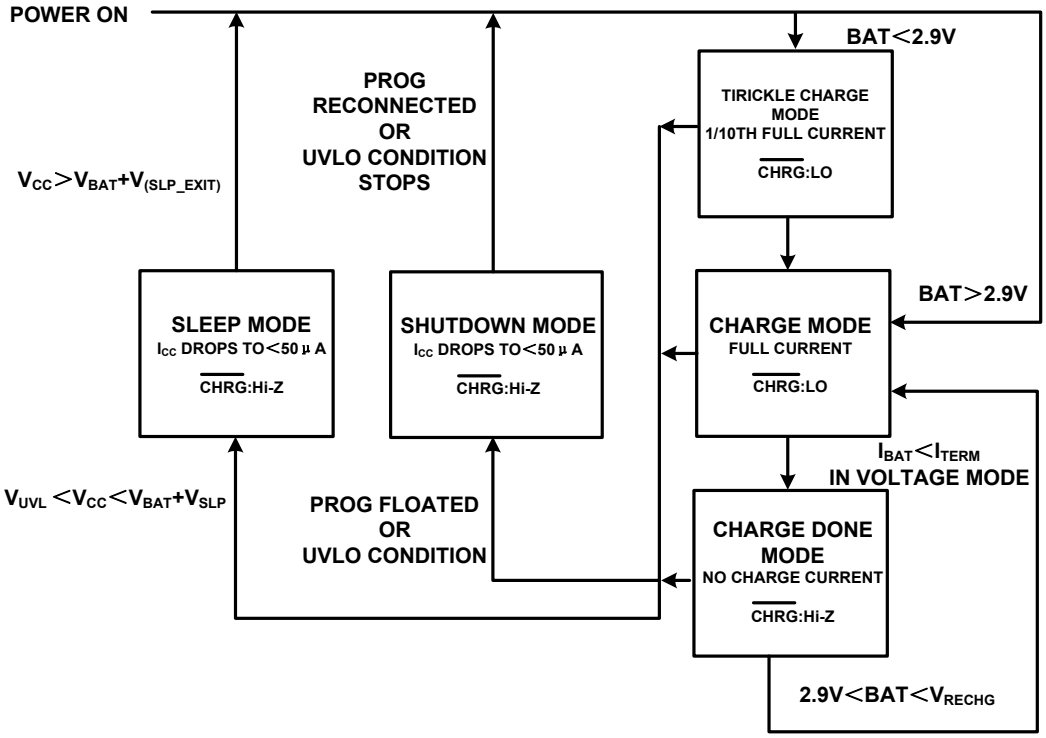


Figure 6. Operational Flow Chart

CONTROL LOGIC OVERVIEW

An external host can enable or disable the charging process using a dedicated control N-CH MOSFET. At any point in the charge cycle, the CE3213 can be put into shutdown mode by removing R_{PROG} thus floating the PROG pin. A high-level signal on the gate of N-CH MOSFET enables the charge, and a low-level signal disables the charge. The CE3213 is in shutdown mode with floating the PROG pin. A new charge cycle can be initiated by reconnecting the program resistor. **Details refer to Manual Shutdown sections.**

Table 1 describes the charger control logic operation.

Table 1. Control Logic Functionality

CE3213 FAMMILY OPERATION MODE	PROG PIN FLOATING	INPUT POWER	OUTPUT SHORT CIRCUIT	TERMINATION (latched)	POWER DOWN	CHARGER POWER STAGE
POWER DOWN	No	Low	X	X	Yes	OFF

SLEEP	X	Not Detected	X	X	No	OFF
SHUTDOWN	Yes	Detected	X	X	X	OFF
SEE STATE DIAGRAM	No	Detected	Yes	X	No	ON
	No	Detected	No	Yes	No	OFF
CHARGING	No	Detected	No	No	No	ON

In both SHUTDOWN and SLEEP modes the charge process is disabled.

NORMAL CHARGE CYCLE

A charge cycle begins when the voltage at the V_{CC} pin rises above the UVLO threshold level and a 1% program resistor is connected from the PROG pin to ground or when a battery is connected to the charger BAT pin. If the BAT pin voltage is less than the V_{TRIKL} threshold (2.9V typical), the charger enters pre-conditioning (trickle charge) mode. In this mode, the CE3213 applies approximately 1/10th of the programmed fast charge current value in current regulation mode to bring the battery voltage up to a safe level for full current charging.

When the BAT pin voltage rises above the V_{TRIKL} threshold (2.9V typical), the charger enters current regulation mode, where the programmed fast charge current I_{CHG} is applied to the battery. When the BAT pin approaches the final float voltage (V_{FLOAT}), the CE3213 enters voltage regulation mode and the charge current begins to decrease. When the charge current drops to 1/10th of the programmed fast charge current value in current regulation mode, the charge cycle ends.

PROGRAMMING CHARGE CURRENT

The charge current delivered to the battery from USB bus or wall adapter supply is programmed using a single resistor from the PROG pin to ground. The battery charge current is 1000 times the current out of the PROG pin. The program resistor and the charge current (I_{CHG}) are calculated using the equations:

$I_{CHG} = K_{PROG} \times V_{PROG} / R_{PORG} = 1000V/R_{PORG}$

$R_{PORG} = K_{PROG} \times V_{PROG} / I_{CHG} = 1000V/I_{CHG}$

POWER ON RESET (POR)

The CE3213 resets itself as the input voltage rises above the POR rising threshold. The CE3213 has a typical rising POR threshold of 3.7V and a falling POR threshold of 3.5V. Then the charger begins to charge the battery.

LOW BATTERY CHARGE CONDITIONING (TRICKLE CHARGE)

During a charge cycle, if the BAT pin voltage is below the V_{TRIKL} threshold (2.9V typical), the CE3213 applies a precharge current, $I_{(PRECHG)}$, 1/10th of the programmed fast charge current value in current regulation mode to the battery until the BAT pin voltage rises back above the V_{TRIKL} threshold (2.9V typical). This feature ensures that deeply discharged batteries are gradually charged before reapplying full charge current, to revive deeply discharged cells and decrease the power dissipation. The resistor connected between the PROG and GND, R_{PROG}, determines the precharge rate. The V_{PRECHG} and K_{PROG}

parameters are specified in the specifications table.

$I_{(PRECHG)}= K_{PROG} \times V_{PRECHG} / R_{PROG}= 100V/R_{PROG}$

For example, if the charger is programmed to charge at 1000mA from the wall adapter input and 500mA from the USB input, the charge current during pre-conditioning mode would be 100mA and 50mA, respectively.

BATTERY CURRENT REGULATION (FAST CHARGE)

The CE3213 offers on-chip current regulation. The current regulation is defined by the value of the resistor connected to PROG pin.

During a charge cycle, the fast charge current I_{CHG} is applied to the battery if the BAT pin voltage is above the V_{TRIKL} threshold (2.9V typical): $I_{CHG}= K_{PROG} \times V_{PROG} / R_{PROG} = 1000V/R_{PROG}$

Where K_{PROG} is the BAT pin output current set factor and V_{PROG} is the fast charge current set voltage.

BATTERY VOLTAGE REGULATION

Voltage regulation feedback is accomplished through the BAT pin. The battery pack voltage is sensed through the BAT pin, which is tied directly to the positive side of the battery pack. The CE3213 monitors the battery pack voltage between the BAT and GND pins. When the battery voltage rises to V_{FLOAT} threshold, the voltage regulation phase begins and the charging current begins to taper down. The voltage regulation threshold V_{FLOAT} is fixed by an internal IC voltage reference.

MONITORING CHARGE CURRENT

When the charge function is enabled, internal circuits generate a current proportional to the charge current at the PROG pin. This current, when applied to the external charge current programming resistor R_{PROG} generates an analog voltage that can be monitored by an external host to calculate the current sourced from the BAT pin. Charge current out of the BAT pin can be determined at any time by monitoring the PROG pin voltage and using the following equations:

$V_{PROG} = I_{BAT} \times R_{PROG} / K_{PROG} = I_{BAT} \times R_{PROG} /1000$

THERMAL REGULATION LOOP

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 125°C. This feature protects the CE3213 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the CE3213. The charge current can be set according to typical (not worst-case) ambient temperatures with the assurance that the charger will automatically reduce the current in worst-case conditions.

CHARGE TERMINATION DETECTION

The charging current is monitored during the voltage regulation phase. Charge termination is indicated at the $\overline{CHRG}$ pin ($\overline{CHRG}$=Hi-Z) once the charge current falls below the termination current threshold I_{TERM} after the final float voltage is reached:

$I_{TERM}= K_{PROG} \times V_{TERM} / R_{PROG}= 100V/R_{PROG}$

which is 1/10th of the programmed fast charge current value in current regulation mode.

This condition is detected by using an internal, filtered comparator to monitor the PROG pin. When the

PROG pin voltage falls below 100mV (Note: Any external sources that hold the PROG pin above 100mV will prevent the CE3213 from terminating a charge cycle.) for longer than $T_{DGL(TERM)}$ (1.8ms typical), charging is terminated. The charge current is latched off and the CE3213 enters charge done mode, where the input supply current drops to 50μA. **(Note: C/10 charge termination is disabled in trickle charging and thermal regulation modes.)**

When charging, transient loads on the BAT pin can cause the PROG pin to fall below 100mV for short periods of time before the DC charge current has dropped to 1/10th of the programmed fast charge current value in current regulation mode. The 1.8ms deglitch period ($T_{DGL(TERM)}$) on the termination comparator ensures that transient loads of this nature do not result in premature charge cycle termination and false termination indication. Once the average charge current drops below 1/10th the programmed fast charge current value in current regulation mode, the CE3213 terminates the charge cycle and ceases to provide any current through the BAT pin. In this state, all loads on the BAT pin must be supplied by the battery.

The CE3213 constantly monitors the BAT pin voltage in charge done mode. If this voltage drops below the recharge threshold (V_{RECHG}), another charge cycle begins and current is once again supplied to the battery. Figure 6 shows the state diagram of a typical charge cycle

Table 2 describes the termination latch functionality.

Table 2. Termination Latch Functionality

TERMINATION DETECTED LATCHED WHEN	TERMINATION LATCH RESET AT
$I_{BAT} < I_{TERM}$ **AND** $t > T_{DGL(TERM)}$ **AND** $V_{BAT} > V_{(RECHRG)}$	Floating the PROG pin
	New charging cycle started; see state machine diagram

RECHARGE

Once the charge cycle is terminated, the charger sits idle and continuously monitors the voltage on the BAT pin using a comparator with a 1.8ms filter time, $T_{DGL(RECHG)}$. A charge cycle automatically restarts when the battery voltage falls below V_{RECHG} threshold (which corresponds to approximately 80%-90% battery capacity). This ensures that the battery is kept at, or near, a fully charged condition and eliminates the need for periodic charge cycle initiations. $\overline{CHRG}$ output enters a strong pull-down state during recharge cycles.

If the battery is removed from the charger, a sawtooth waveform of approximately 100mV appears at the battery output. This is caused by the repeated cycling between termination and recharge events. This cycling results in pulsing at the $\overline{CHRG}$ output; an LED connected to this pin will exhibit a blinking pattern, indicating to the user that a battery is not present. The frequency of the sawtooth is dependent on the amount of output capacitance. See the Battery Absent Detection section for additional details.

MANUAL SHUTDOWN

At any point in the charge cycle, the CE3213 can be put into shutdown mode by removing RPROG thus floating the PROG pin. This reduces the battery drain current to less than 2μA and the supply current to

less than 50μA. A new charge cycle can be initiated by reconnecting the program resistor.

In manual shutdown, the $\overline{CHRG}$ pin is set to the high impedance state.

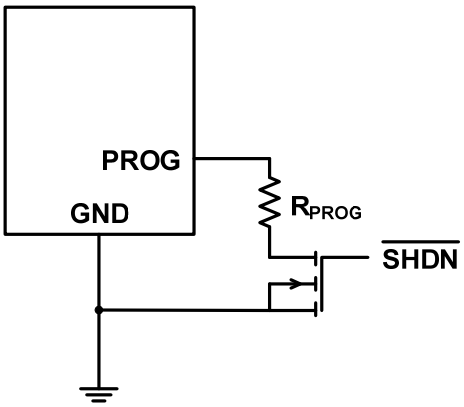


Figure 7. Shutdown Operation

SIGNALS IN A CHARGE CYCLE

Signals in a charge cycle are illustrated in Figure 8.

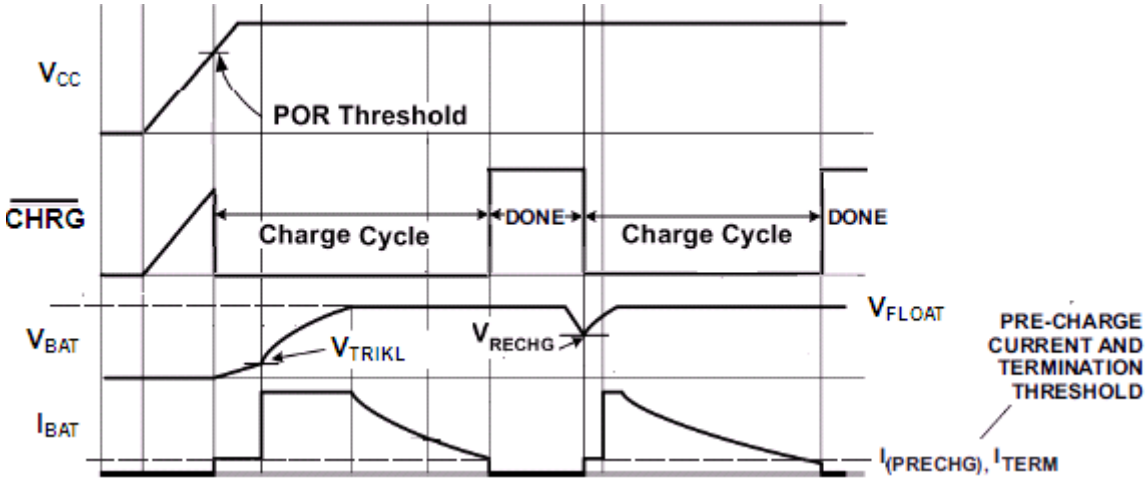


Figure 8. Operation Waveforms

BATTERY ABSENT DETECTION

The CE3213 provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

If the battery is not present, the charger will charge the output capacitor to the regulation voltage quickly, then the BAT pin's voltage decays slowly to recharge threshold because of low leakage current at BAT pin, which results in a 100mV ripple waveform at BAT pin, in the meantime, $\overline{CHRG}$ pin outputs a pulse to indicate that the battery's absence. The pulse's frequency is around 1Hz when a 10μF output capacitor is used.

CHARGE STATUS INDICATOR ($\overline{CHRG}$)

The CE3213 family provides battery charge status via $\overline{CHRG}$ status pin. $\overline{CHRG}$ pin is internally connected to an N-channel open drain MOSFET. $\overline{CHRG}$ is pulled low when the charger is in charging status, otherwise $\overline{CHRG}$ becomes high impedance.

The following table lists the indicator status and its corresponding charging state.

Table 3. Charge Status Indicator(1)

Charge State Description	$\overline{CHRG}$
Preconditioning-Current Mode (Trickle) Charge	ON
Constant-Current Mode (Fast) Charge	ON
Constant-Voltage Mode (Taper) Charge, $I_{BAT}>I_{TERM}$	ON
Charge Temination (Charge Done)	HI-Z
Power Down (Undervoltage Lockout) Mode	HI-Z
Sleep Mode ($V_{CC}< V_{SLP}$, or the V_{CC} is removed)	HI-Z
Floating the PROG pin	HI-Z
No battery with Charge Enabled	FLASH Rate depends on C_{BAT}
Fault Condition (Battery Short Circuit)	ON
Fault Condition (Battery Overvoltage)	HI-Z

(1) Pulse loading on the BAT pin may cause the IC to cycle between Done and charging states (LEDs Flashing).

The $\overline{CHRG}$ status pin can be used to communicate to the host processor or drive LEDs.

It is supposed that red LED and green LED are connected to $\overline{CHRG}$ pin

The LEDs should be biased with as little current as necessary to create reasonable illumination, therefore, a ballast resistor should be placed between the LED cathode and the status pin. LED current consumption will add to the overall thermal power budget for the device package, hence it is good to keep the LED drive current to a minimum 2mA should be sufficient to drive most low cost red or green LEDs. It is not recommended to exceed 10mA for driving an individual status LED. The required ballast resistor values can be estimated using following formula:

$R_{BALLAST} = [V_{CC} - V_{F(LED)}] / I_{LED}$

Example:

$R_{BALLAST} = [5.0V - 2.0V] / 2mA = 1.5k\Omega$

Note: Red LED forward voltage (V_F) is typically 2.0V@ 2mA.

STARTUP WITH DEEPLY DEPLETED BATTERY CONNECTED

The CE3213 charger furnishes the programmed charge current if a battery is detected. If no battery is connected the CE3213 operates as follows:

- The output current is regulated to the programmed pre-charge current if $V_{BAT} < V_{TRIKL}$.
- The output current is regulated to the programmed fast charge current If $V_{BAT} > V_{TRIKL}$ **AND** voltage regulation is not reached.

SELECTING INPUT BYPASS CAPACITOR

In most applications, all that is needed is a bypass capacitor, typically a 4.7μF capacitor placed in close

proximity to V_{CC} and GND pins, works well. The CE3213 is designed to work with both regulated and unregulated external dc supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance has to be added to the input of the charger.

Protecting the V_{CC} Pin from Overvoltage Transients

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors to bypass the V_{CC} pin, which powered by USB bus or Wall Adapter Input. High voltage transients can be generated under some start-up conditions, depending on the power supply characteristics and cable length, such as when the USB or wall adapter is hot plugged. When power is supplied via the USB bus or wall adapter, the cable inductance along with the self resonant and high Q characteristics of some types of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage pin ratings and damage the CE3213. The long cable lengths of most wall adapters and USB cables makes them especially susceptible to this problem. To bypass the V_{CC} pin, add a 1Ω resistor in series with an X5R ceramic capacitor to lower the effective Q of the network and greatly reduce the ringing. A tantalum, OS-CON, or electrolytic capacitor can be used in place of the ceramic and resistor, as their higher ESR reduces the Q, thus reducing the voltage ringing.

The oscilloscope photograph in Figure 9 shows how serious the overvoltage transient can be for the USB and wall adapter inputs. For both traces, a 5V supply is hot-plugged using a three foot long cable. For the top trace, only a 4.7μF capacitor (without the recommended 1Ω series resistor) is used to locally bypass the input. This trace shows excessive ringing when the 5V cable is inserted, with the overvoltage spike reaching 10V. For the bottom trace, a 1Ω resistor is added in series with the 4.7μF capacitor to locally bypass the 5V input. This trace shows the clean response resulting from the addition of the 1Ω resistor.

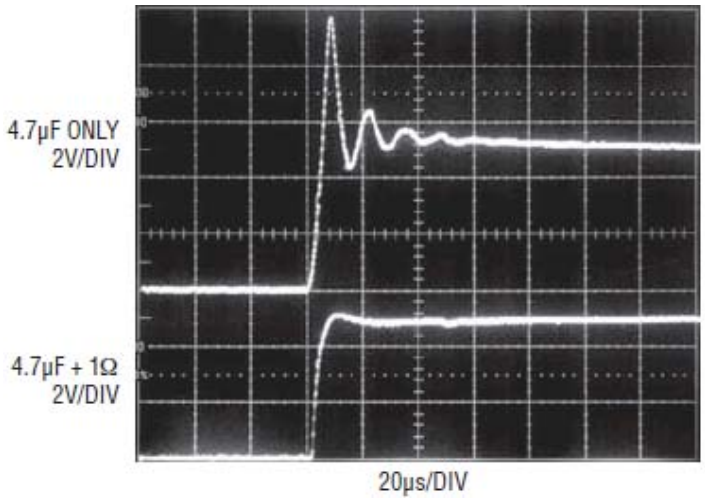


Figure 9. Waveforms Resulting from Hot-Plugging a 5V Input Supply

Even with the additional 1Ω resistor, bad design techniques and poor board layout can often make the overvoltage problem even worse. System designers often add extra inductance in series with input lines in an attempt to minimize the noise fed back to those inputs by the application. In reality, adding these

extra inductances only makes the overvoltage transients worse. Since cable inductance is one of the fundamental causes of the excessive ringing, adding a series ferrite bead or inductor increases the effective cable inductance, making the problem even worse. For this reason, **do not** add additional inductance (ferrite beads or inductors) in series with the USB or wall adapter inputs. For the most robust solution, 6V transorbs or zener diodes may also be added to further protect the USB and wall adapter inputs. Two possible protection devices are the SM2T from ST Microelectronics and the EDZ series devices from ROHM.

Always use an oscilloscope to check the voltage waveforms at the V_{CC} pin during USB and wall adapter hot-plug events to ensure that overvoltage transients have been adequately removed.

SELECTING OUTPUT CAPACITOR

The CE3213 family requires only a small output capacitor for loop stability. A 10μF ceramic capacitor placed between the BAT and GND pins is typically sufficient for embedded applications (i.e., non-removable battery packs). This capacitance helps with termination, and cycling frequency between charge done and refresh charge when no battery is present. It also helps cancel out any battery lead inductance for long leaded battery packs. It is recommended to put as much ceramic capacitance on the input as the output so as not to cause a drop out of the input when charging is initiated.

STABILITY CONSIDERATIONS

The constant-voltage mode feedback loop is stable without an output capacitor provided a battery is connected to the charger output. With no battery present, an output capacitor is recommended to reduce ripple voltage. When using high value, low ESR ceramic capacitors, it is recommended to add a 1Ω resistor in series with the capacitor. No series resistor is needed if tantalum capacitors are used.

In constant-current mode, the PROG pin is in the feedback loop, not the battery. The constant-current mode stability is affected by the impedance at the PROG pin. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 20k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin is loaded with a capacitance, C_{PROG}, the following equation can be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 10^5 \bullet C_{PROG}}$$

Average, rather than instantaneous, charge current may be of interest to the user. For example, if a switching power supply operating in low current mode is connected in parallel with the battery, the average current being pulled out of the BAT pin is typically of more interest than the instantaneous current pulses.

In such a case, a simple RC filter can be used on the PROG pin to measure the average battery current as shown in Figure 10. A 10k resistor has been added between the PROG pin and the filter capacitor to ensure stability

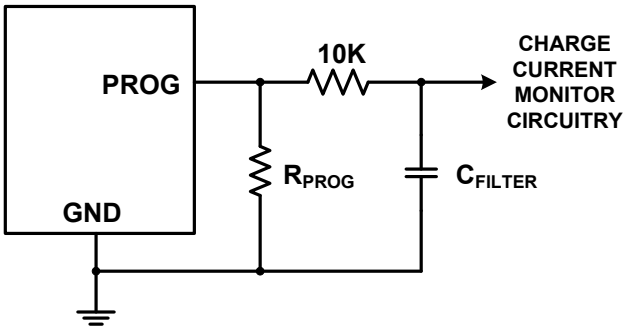


Figure 10. Isolating Capacitive Load on PROG Pin and Filtering

POWER DISSIPATION

The conditions that cause the CE3213 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Nearly all of this power dissipation is generated by the internal MOSFET—this is calculated to be approximately:

$P_D = (V_{CC} – V_{BAT}) • I_{BAT}$

where P_D is the power dissipated, V_{CC} is the input supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$T_A = 125°C – P_D \theta_{JA}$

$T_A = 125°C – (V_{CC} – V_{BAT}) • I_{BAT} • \theta_{JA}$

Example: An CE3213 operating from a 5V USB supply is programmed to supply 1A full-scale current to a discharged Li-Ion battery with a voltage of 3.7V. Assuming θ_{JA} is 55°C/W (see Board Layout Considerations), the ambient temperature at which the CE3213 will begin to reduce the charge current is approximately:

$T_A = 125°C – (5V – 3.7V) • 1A • 55°C/W$

$T_A = 125°C – 1.3W • 55°C/W = 125°C –71.5°C$

$T_A = 53.5°C$

The CE3213 can be used above 53.5°C ambient, but the charge current will be reduced from 1A. The approximate current at a given ambient temperature can be approximated by:

$$I_{BAT} = \frac{125°C - T_A}{(V_{CC} - V_{BAT}) \bullet \theta_{JA}}$$

Using the previous example with an ambient temperature of 64.5°C, the charge current will be reduced to approximately:

$$I_{BAT} = \frac{125°C - 64.5°C}{(5V - 3.7V) \bullet 55°C/W} = \frac{1.1W}{1.3V},$$

$I_{BAT} = 846mA$

Moreover, when thermal feedback reduces the charge current, the voltage at the PROG pin is also

reduced proportionally as discussed in the Operation section.

It is important to remember that CE3213 applications do not need to be designed for worst-case thermal conditions since the IC will automatically reduce power dissipation when the junction temperature reaches approximately 125°C.

THERMAL CONSIDERATIONS

The thermal path for the heat generated by the IC is from the die to the copper lead frame, through the package leads (especially the ground lead) and the Exposed Thermal Die Pad to the PC board copper. The PC board copper is the heat sink.

The CE3213 is housed in a thermally-enhanced Exposed Thermal Die Pad package that has an exposed metal pad on the backside of the package.

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = (T_J - T_A) / P_D$$

Where:

T_J = chip junction temperature

T_A = ambient temperature

P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D, is a function of the charge rate and the voltage drop across the internal Power FET. It can be calculated from the following equation when a battery pack is being charged :

$$P_D = (V_{CC} - V_{BAT}) \bullet I_{BAT}$$

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, Figure 3.

If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active effectively reducing the charge current to avoid excessive IC junction temperature.

For improved overall thermal performance of the charger, to deliver maximum charge current under all conditions, it is critical that the exposed metal pad on the backside of the CE3213 package is properly soldered to the PC board ground via thermal land on the PCB. This ground trace acts as a both a heat sink and heat spreader. The typical thermal resistance, θ_{JA}, 55°C/W, is achieved based on a land

pattern of 3 mm x1.8 mm with six vias (0.33-mm via diameter, the standard thermal via size) without air flow (see Figure 11).

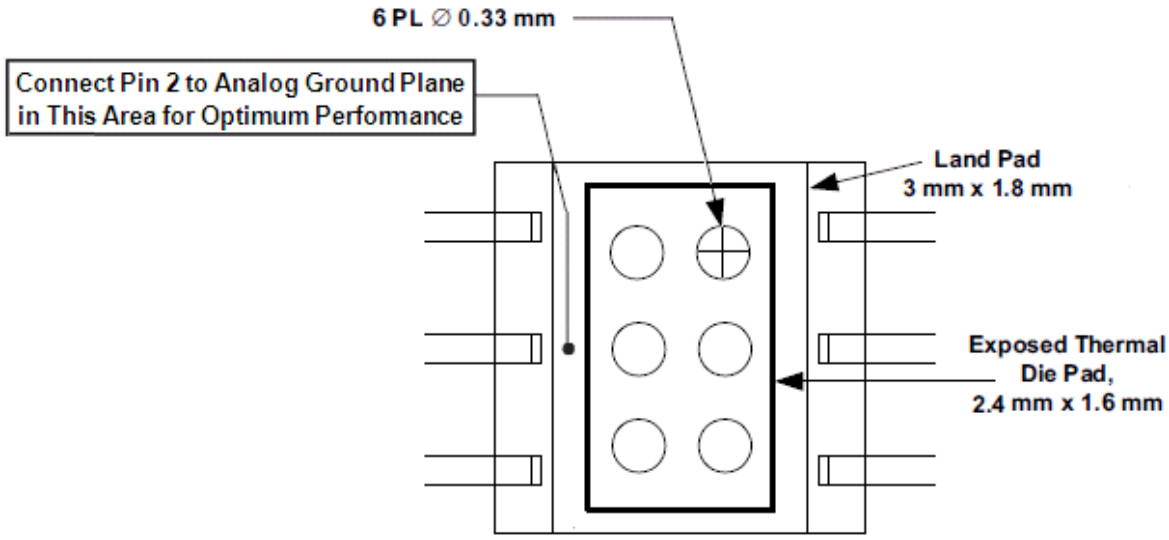


Figure 11. Recommended Land Pattern for 6-Pin DFN3x3 Exposed Thermal Die Pad

Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistances far greater than 55°C/W. As an example, a correctly soldered CE3213 can deliver 1000mA to a battery from a 5V supply at room temperature. Without a good backside thermal connection, this number could drop to less than 700mA.

For operation at full-scale rated charge current, the analog ground plane must provide adequate heat dissipating area. A 3 mm by 1.8 mm plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and air flow. Most applications have larger areas of internal ground plane available, and the Exposed Thermal Die Pad should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 1A or greater operation is desired. Connection from the exposed area of the Exposed Thermal Die Pad to the analog ground plane layer should be made using 0.33 mm diameter vias to avoid solder wicking through the vias. Six vias should be in the Exposed Thermal Die Pad area. Additional vias beyond the six recommended that enhance thermal performance should be included in areas not under the device package.

The footprint copper pads should be as wide as possible and expand out to larger copper areas to spread and dissipate the heat to the surrounding ambient.

Other heat sources on the board, not related to the charger, must also be considered when designing a PC board layout because they will affect overall temperature rise and the maximum charge current

INCREASING THERMAL REGULATON CURRENT

Reducing the voltage drop across the internal MOSFET can significantly decrease the power dissipation in the IC. This has the effect of increasing the current delivered to the battery during thermal regulation. **One method is by dissipating some of the power through an external component, such as a resistor or diode.**

Example: An CE3213 operating from a 5V wall adapter is programmed to supply 1000mA full-scale current to a discharged Li-Ion battery with a voltage of 3.7V. Assuming θ_{JA} is 55°C/W, the approximate charge current at an ambient temperature of 64.5°C is:

$$I_{BAT} = \frac{125°C - 64.5°C}{(5V - 3.7V) \bullet 55°C/W} = \frac{1.1W}{1.3V} = 846mA$$

By dropping voltage across a resistor in series with a 5V wall adapter (shown in Figure 12), the on-chip power dissipation can be decreased, thus increasing the thermally regulated charge current

$$I_{BAT} = \frac{125°C - 64.5°C}{(V_S - I_{BAT}R_{CC} - V_{BAT}) \bullet \theta_{JA}}$$

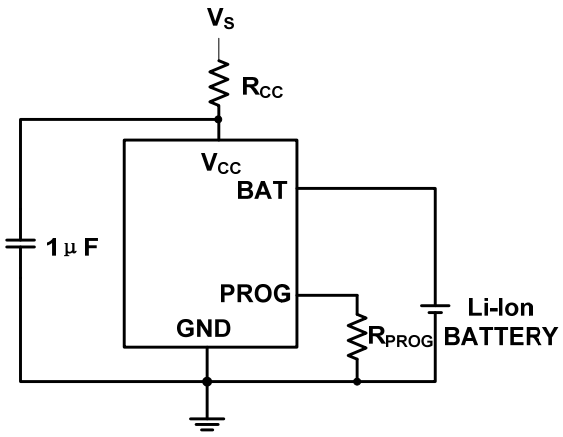


Figure 12. A Circuit to Maximize Thermal Mode Charge Current

Solving for I_{BAT} using the quadratic formula[2]

$$I_{BAT} = \frac{(V_S - V_{BAT}) - \sqrt{(V_S - V_{BAT})^2 - \frac{4R_{CC}(125°C - T_A)}{\theta_{JA}}}}{2R_{CC}}$$

Using R_{CC}=0.25Ω, V_S=5V, V_{BAT}=3.7V, T_A=64.5°C and θ_{JA}=55°C/W we can calculate the thermally regulated charge current to be: I_{BAT}=1063.77mA

The result shows that this configuration can deliver 1000mA full-scale rated charge current at higher ambient temperature.

While this application delivers more energy to the battery and reduces charge time in thermal mode, it may actually lengthen charge time in voltage mode if V_{CC} becomes low enough to put the CE3213 into dropout.

This technique works best when R_{CC} values are minimized to keep component size small and avoid dropout. Remember to choose a resistor with adequate power handling capability.

CHARGE CURRENT SOFT-START and SOFT-STOP

The CE3213 includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When

a charge cycle is initiated, the charge current ramps from zero to the full-scale current over a period of approximately 20μs. Likewise, internal circuitry slowly ramps the charge current from full-scale to zero when the charger is shut off or self terminates. This has the effect of minimizing the transient current load on the power supply during start-up and charge termination.

REVERSE POLARITY INPUT VOLTAGE PROTECTION

In some applications, protection from reverse polarity voltage on V_{CC} is desired. If the supply voltage is high enough, a series blocking diode can be used. In other cases, where the voltage drop must be kept low a P-channel MOSFET can be used (as shown in Figure 13).

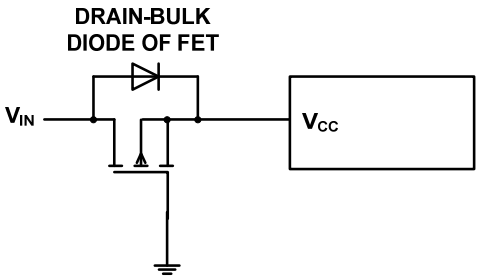


Figure 13. Low Loss Input Reverse Polarity Protection

USB and WALL ADAPTER POWER

The CE3213 family allows charging from both a wall adapter and a USB port. Figure 14 shows an example of how to combine wall adapter and USB power inputs. A P-channel MOSFET, MP1, is used to prevent back conducting into the USB port when a wall adapter is present and a Schottky diode, D1, is used to prevent USB power loss through the 1k pull-down resistor.

Typically a wall adapter can supply more current than the 500mA-limited USB port. Therefore, an N-channel MOSFET, MN1, and an extra 2k program resistor are used to increase the charge current to 1A when the wall adapter is present.

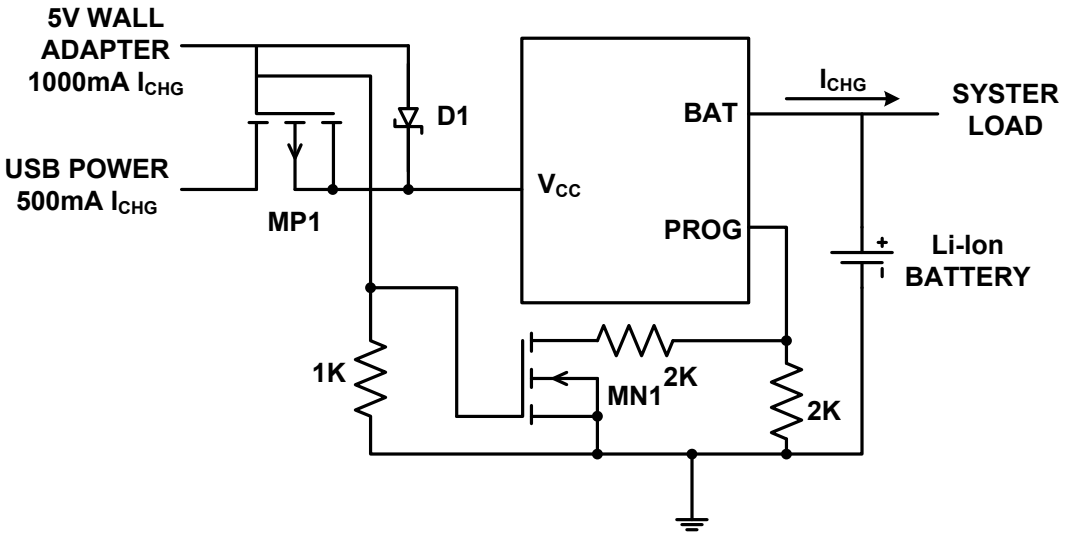
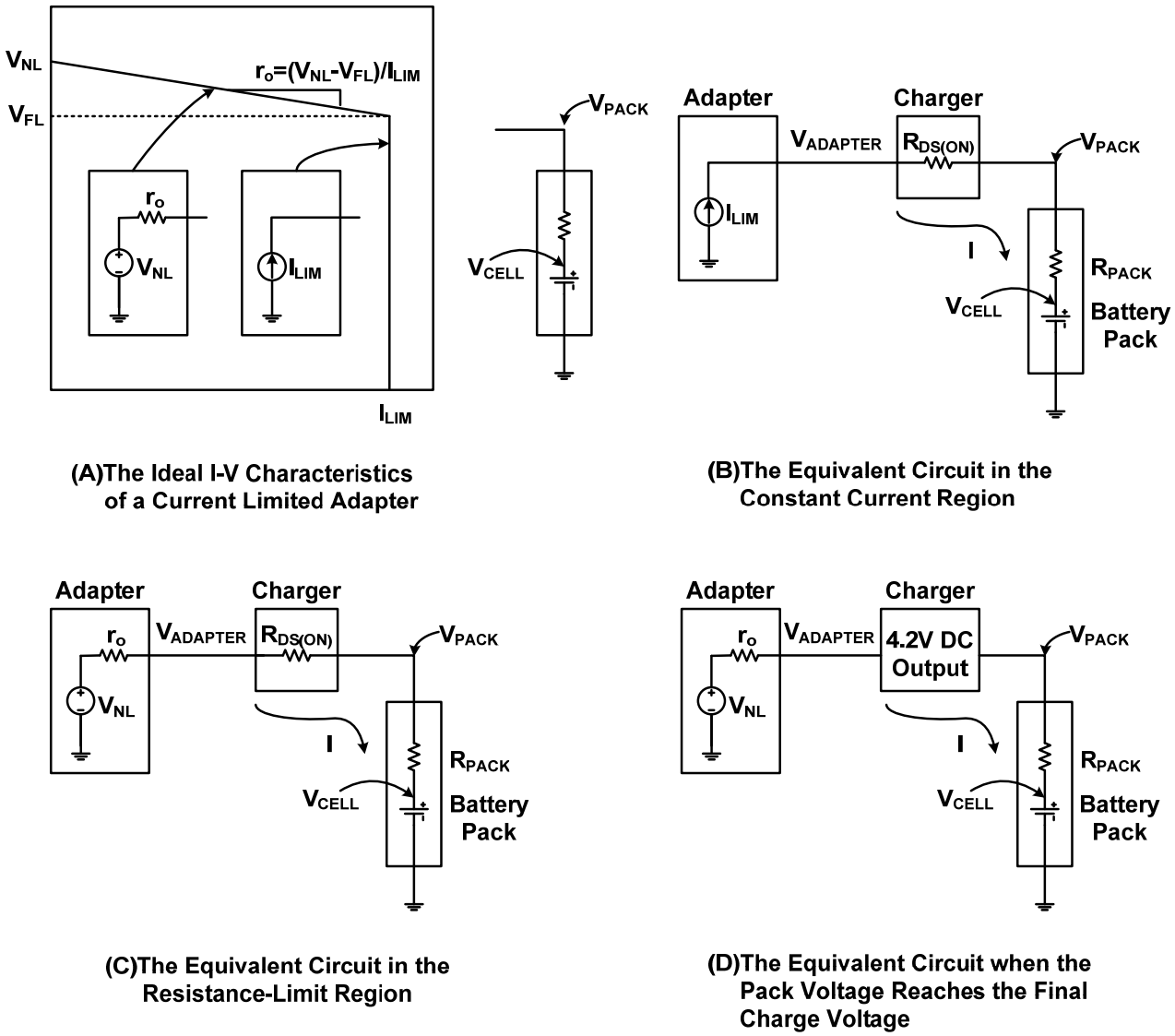


Figure 14. Combining Wall Adapter and USB Power

CURRENT-LIMITED ADAPTER

Figure 15 shows the ideal current-voltage characteristics of a current-limited adapter. V_{NL} is the no-load adapter output voltage and V_{FL} is the full load voltage at the current limit I_{LIM}. Before its output current reaches the limit I_{LIM}, the adapter presents the characteristics of a voltage source. The slope r_O represents the output resistance of the voltage supply. For a well regulated supply, the output resistance can be very small, but some adapters naturally have a certain amount of output resistance.

The adapter is equivalent to a current source when running in the constant-current region. Being a current source, its output voltage is dependent on the load, which, in this case, is the charger and the battery.



(A)The Ideal I-V Characteristics of a Current Limited Adapter

(B)The Equivalent Circuit in the Constant Current Region

(C)The Equivalent Circuit in the Resistance-Limit Region

(D)The Equivalent Circuit when the Pack Voltage Reaches the Final Charge Voltage

Figure 15. The Equivalent Circuit of the Charging System Working with Current Limited Adapter

PCB LAYOUT CONSIDERATIONS

The CE3213 series are fully integrated single-chip low cost single-cell Li-Ion or Li-Pol battery chargers ideal for portable applications. Careful PCB layout is necessary. For optimal performance, place all peripheral components as close to the IC as possible. A short connection is highly recommended.

Several layout tips are listed below for the best electric and thermal performance. Figure 16 below illustrates the PCB layout example as reference.

- Input bypass capacitor from V_{CC} to GND (thermal pad) should be placed as close as possible to CE3213, with short trace runs to both V_{CC} and GND (thermal pad), and connected to ground plane. The trace of input in the PCB should be placed far away the sensitive devices or shielded by the ground.
- The GND should be connected to a strong ground plane for heat sinking and noise protection.
- Output filter capacitors from BAT to GND (thermal pad) should be placed as close as possible to CE3213, with short trace runs to both BAT and GND (thermal pad), and connected to ground plane to reduce noise coupling.
- The connection of R_{PROG} should be isolated from other noisy traces. The short wire is recommended to prevent EMI and noise coupling.
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The BAT pin is the voltage feedback to the device and should be connected with its trace as close to the battery pack as possible.
- The high current charge paths into V_{CC} pin and from the BAT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The CE3213 family are packaged in a thermally enhanced Exposed Thermal Die Pad package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection.
- There is an internal electrical connection between the exposed thermal pad and GND pin of the device. The exposed thermal pad must be connected to the same potential as the GND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. GND pin must be connected to ground at all times.

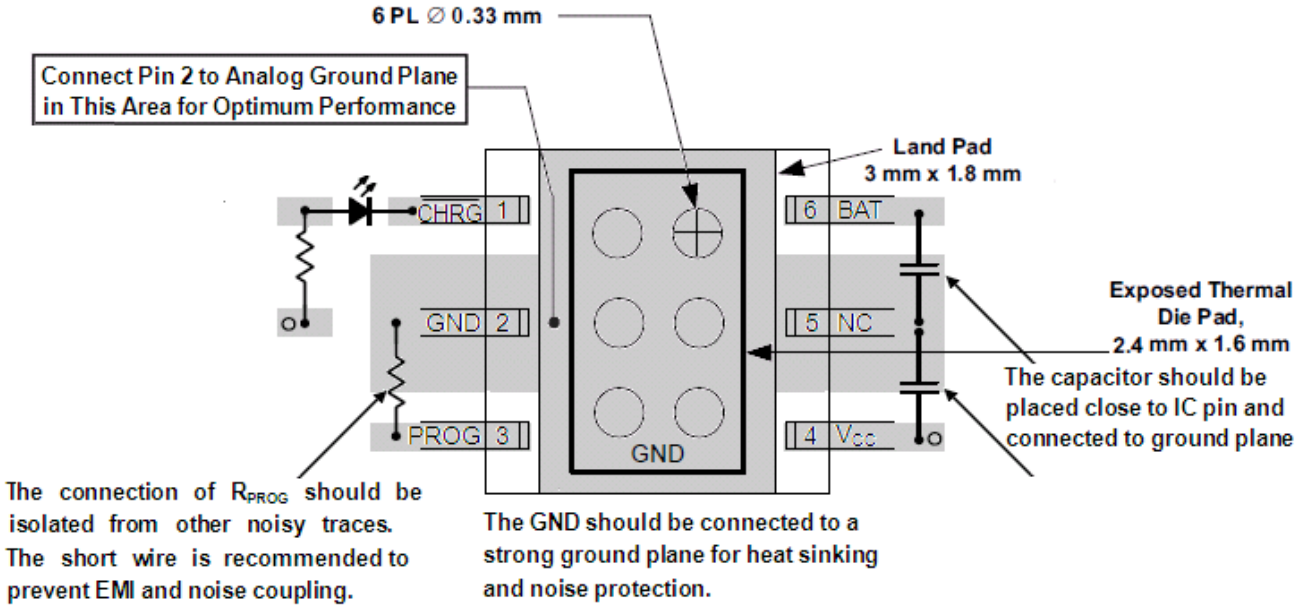
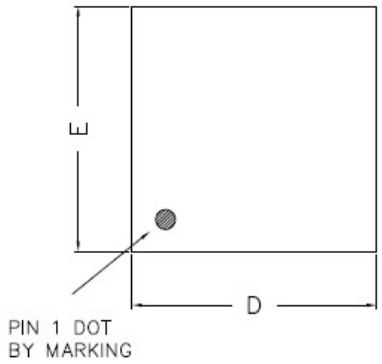


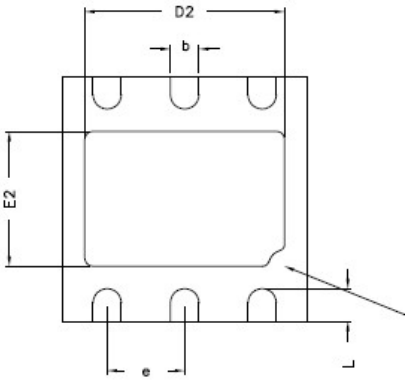
Figure 16. CE3213AXXXFC6 PCB Layout

■ PACKAGING INFORMATION

● DFN3x3-6 Package Outline Dimensions

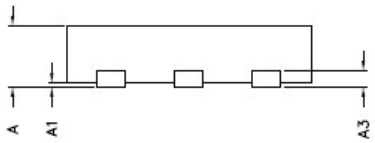


TOP VIEW



BOTTOM VIEW

PIN #1 IDENTIFICATION
CHAMFER



SIDE VIEW

Symbol	Dimensions In Millimeters		
	Min	NOM	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.2 REF		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
b	0.28	0.35	0.40
L	0.30	0.40	0.50
D2	2.30	2.45	2.55
E2	0.15	1.65	1.75
e	0.95 BSC		