■ INTRODUCTION:

The CE3320 is a highly integrated standalone switch mode single-cell Li-Ion battery charger. It utilizes a 1.5MHz synchronous buck converter topology to reduce power dissipation during charging. Low power dissipation, an internal integrated MOSFET and current sense resistor allow a physically small charger that can be embedded in a wide range of space-limited portable applications with high capacity batteries. The single cell charger has a single input that operates from either a USB port or AC wall adapter for a versatile solution.

The battery is charged in three phases: trickle-charge, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and shutdown the charge if the internal temperature threshold is exceeded.

The CE3320 includes complete charge termination circuitry, automatic recharge and a ±1% float voltage. Battery charge current, charge timeout and end-of-charge indication parameters are set with external components.

Additional features include defective battery detection, battery overvoltage protection and a voltage-based battery pack thermistor monitoring input (NTC) that monitors battery temperature for safe charging.

■ APPLICATIONS:

- Battery Back-Up Systems
- Tablets and Portable Mobile Internet Devices
- Netbook, Smartbook
- Portable Media Players
- IPod, iPhone, iPad Docking
- Bluetooth speaker & 2.4G Wireless speaker
- Smart Phones
- Portable Data Capture Terminals
- Personal Medical Products
- Portable Instruments
- 3G/4G Wireless Routers

■ FEATURES:

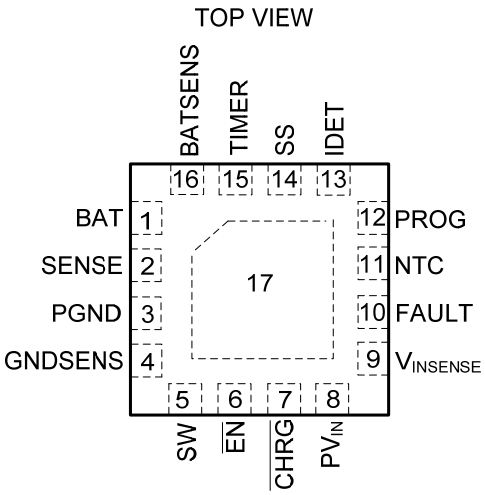
- 1.5MHz High-Efficiency Switch Mode Charger
- Single Input Mini-USB/Adapter Charger
  - 7V Maximum Input Voltage Rating
  - 5.5 V Maximum Operating Input Voltage
  - Compatible with Current Limited Adapters
- High Integration for Reduced BOM Count and Board Space Savings
  - Low $R_{DS(ON)}$ Integrated Power FETs for Up to 2A Charge Rate
  - Integrated Charge Current Sense Resistor
  - Integrated Reverse Current Blocking Element
- Low Power Dissipation
- Accurate Battery Management Functions
  - 1% Battery Regulation Accuracy
  - 10% Charge Current Accuracy
- Remote Sensing at Battery Terminals
- IDET Blanking
- Programmable Charge Current Detection/Termination
- Automatic Recharge
- Complete System Level Protection
  - Input UVLO, Sleep Mode, V_{IN_DPM}, Battery Over-voltage Protection(Battery OVP)
  - Reverse Leakage Protection Prevents Battery Drainage
  - Hard Short On The Battery Terminals Protection
  - High Rate Charge Current Limit
  - Cycle By Cycle Current Limit
  - Thermal Shutdown
  - Voltage Based, NTC Monitoring Input For Temperature Qualified Charging
  - Programmable Charge Safety Timer
  - Defective Battery Detection
  - Soft-Start Feature to Reduce Inrush Current
- Status Output for Charging and Faults

■ ORDER INFORMATION(1)

Operating free air temperature range	Battery Float Voltage	Package	Device No.
-40~+85℃	4.20V	QFN4X4-16	CE3320A420QD16
-40~+85℃	**4.20V**	**QFN4X4-16B**	**CE3320A420QD16B**
-40~+85℃	4.35V	QFN4X4-16B	CE3320A435QD16B

(1)Contact Chipower to check availability of other battery float voltage versions.

■ PIN CONFIGURATION:



PIN FUNCTIONS

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	BAT	I/O	**Battery Charger Output Terminal**. Connect to the positive terminal of the battery. Connect a 10μF ceramic chip capacitor between BAT and PGND to keep the ripple voltage small.
2	SENSE	I	**Internal Sense Resistor**. Connect to external inductor.
3	PGND	P	**Power Ground**. Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the internal n-channel low-side FET. On PCB layout, connected directly to ground connection of input and output capacitors of the charger and should be connected to the ground plane to return current through the internal low-side FET.
4	GNDSENS	I	**Ground Sense**. Connect this pin to the negative battery terminal. GNDSENS provides a Kelvin connection for PGND and must be connected to PGND schematically.
5	SW	O	**Switch Node Connection**. This pin connects to the drains of the internal main and synchronous power MOSFET switches. Connect to external inductor. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

(1)I = input; O = output; P = power

PIN FUNCTIONS (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
6	$\overline{EN}$	I	**Chip Enable Input Pin**. Pulling the $\overline{EN}$ pin high places the CE3320 into a low power state where the BAT drain current drops to less than 3μA and the supply current is reduced to less than 50μA. For normal free running operation, pull the $\overline{EN}$ pin low.
7	$\overline{CHRG}$	I	**Open-Drain Charge Status Output**. When the battery is being charged, $\overline{CHRG}$ is pulled low by an internal N-channel MOSFET. When the charge current drops below the IDET threshold (set by the R_{IDET} programming resistor) for more than 5 milliseconds, the N-channel MOSFET turns off and a 30μA weak current source is connected from $\overline{CHRG}$ to ground. (This signal is latched and is reset by initiating a new charge cycle.) When the timer runs out or the input supply is removed, the current source will be disconnected and the $\overline{CHRG}$ pin is forced to a high impedance state. A battery pack temperature fault causes this pin to blink.
8	PV_{IN}	I	**Positive Supply Voltage Input**. This pin connects to the power devices inside the chip. V_{IN} ranges from 4.5V to 5.5V for normal operation. Operation down to the V_{IN_DPM} is allowed with current limited wall adapters. Decouple with a 10μF or larger surface mounted ceramic capacitor.
9	$V_{INSENSE}$	I	**Positive Supply Sense Input**. This pin connects to the inputs of all input comparators (UVL, $V_{INSENSE}$ to $V_{BATSENS}$, V_{IN_DPM}). It also supplies power to the controller portion of this chip. When the BATSENS pin rises to within 130mV of $V_{INSENSE}$, the CE3320 enters sleep mode, dropping I_{IN} to 50μA. Tie this pin to the terminal of the PV_{IN} by a R&C decoupling circuit.
10	FAULT	I	**Battery Fault**. This pin is a logic high if a shorted battery is detected or if a battery pack temperature fault is detected. A battery pack temperature fault occurs with the NTC temperature monitor circuit enabled and the thermistor temperature is either below 0°C or above 50°C (typical).

(1) I = input; O = output; P = power

PIN FUNCTIONS (continued)

11	NTC	I	**Input to the NTC (Negative Temperature Coefficient) Thermistor Temperature Monitoring Circuit**. Under normal operation, tie a thermistor from the NTC pin to the GNDSENS pin and a resistor of equal value from NTC to $V_{INSENSE}$. When the voltage on this pin is above $0.74V_{INSENSE}$ (Cold, 0°C) or below $0.29V_{INSENSE}$ (Hot, 50°C), charging is disabled and the $\overline{CHRG}$ pin blinks. When the voltage on NTC comes back between $0.74V_{INSENSE}$ and $0.29V_{INSENSE}$, the timer continues where it left off and charging resumes. There is approximately 3°C of temperature hysteresis associated with each of the input comparators. If the NTC function is not used, connects the NTC pin to GNDSENS. This will disable all of the NTC functions. NTC should never be pulled above $V_{INSENSE}$.
12	PROG	O	**Charge Current Program**. The R_{PROG} resistor connects from this pin to GNDSENS, setting the current: $$R_{PROG} = \frac{1.130K}{I_{BAT}(AMPS)}$$ where I_{BAT} is the high rate battery charging current.
13	IDET	O	**Charge Rate Detection Threshold**. Connecting a resistor, R_{IDET} to GNDSENS programs the charge rate detection threshold. If R_{IDET} = R_{PROG}, $\overline{CHRG}$ provides an $I_{BAT}/10$ indication. For other thresholds see the Applications Information section.
14	SS	O	**Soft-Start/Compensation**. Provides soft-start function and compensation for the float voltage control loop and compensation for the charge current control loop. Tie a soft-start/compensation capacitor between this pin and GNDSENS.
15	TIMER	O	**Timer Capacitor**. The timer period is set by placing a capacitor, C_{TIMER}, to GNDSENS. Set C_{TIMER} to: C_{TIMER} = Time (Hrs) • 0.09(μF) where time is the desired taper timer charging time. Connect this pin to IDET to disable the timer. Connect this pin to GNDSENS to end battery charging when I_{BAT} drops below the IDET charge rate threshold.
16	BATSENS	I	**Battery Sense Input**. An internal resistor divider sets the final float voltage at this pin. The resistor divider is disconnected in sleep mode or when $\overline{EN}$ = H to reduce the battery drain current. Connect this pin to the positive battery terminal.
17	Exposed Pad(bottom)	P	**Ground**. This pin must be soldered to the PCB ground for electrical contact and rated thermal performance. There is an internal electrical connection between the exposed pad and the PGND pin of the device. Do not use the Exposed Pad as the primary ground input for the device. PGND pin must be connected to ground at all times.

(1)I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS(1)

(unless otherwise specified, T_A=25°C)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage(2)	t<1ms，DC<1%	PV_{IN},$V_{INSENSE}$	-0.3~7	V
	Steady State		-0.3~ 6	
SW, SENSE, BAT, BATSENS, SS, FAULT, $\overline{CHRG}$, $\overline{EN}$, NTC, PROG, IDET, TIMER Voltage(2)			-0.3~6	V
Output sink current		$I_{\overline{CHRG}}$	10	mA
Power Dissipation	QFN4x4-16	P_D	2.5	W
	QFN4x4-16B		2.7	
Operating free air temperature range(3)		T_A	-40~85	°C
Operating Junction Temperature(4)		T_j	-40~125	°C
Storage Temperature Range		T_{stg}	-65~+125	°C
Lead Temperature (Soldering, 10s)		T_{solder}	260	°C
ESD rating(5)		Human Body Model - (HBM)	2	kV
		Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) The CE3320 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

(4) This IC includes overtemperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

(5) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNITS
Supply voltage at PV_{IN}, $V_{INSENSE}$	4.5(1)		5.5 (2)	V
Charge current, I_{BAT}			2	A
Operating free air temperature range, T_A	0		85	°C
Operating junction temperature range, T_j	0		125	°C

(1) If PV_{IN} and $V_{INSENSE}$ is between UVLO and 4.5V, and above the battery voltage, then the IC is active (can deliver some charge to the battery), but the IC will have limited or degraded performance (some functions may not meet data sheet specifications). The battery may be undercharged (V_{FLOAT} less than in the specification), but will not be overcharged (V_{FLOAT} will not exceed specification).

(2) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on the SW pin. A tight layout minimizes switching noise.

■ ELECTRICAL CHARACTERISTICS

V_{IN}=5V, $V_{\overline{EN}}$=0V, R_{PROG}=560Ω, R_{IDET}=560Ω, T_A=25℃, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Supply Voltage	V_{IN}	**Note1**	4.5		5.5	V
Supply Current	I_{IN}	PV_{IN} Connected to $V_{INSENSE}$, PROG and IDET Pins Open, Charger On			2	mA
		Shutdown, $\overline{EN}$= V_{IN}			50	μA
ENABLE						
$\overline{EN}$ Low-level Voltage	$V_{\overline{ENL}}$	$V_{\overline{EN}}$ Falling, Device ON			0.3	V
$\overline{EN}$ High-level Voltage	$V_{\overline{ENH}}$	$V_{\overline{EN}}$ Rising, Device Off	1.5		V_{IN}	V
$\overline{EN}$ Input Bias Current	$I_{(\overline{EN})}$	$\overline{EN}$=GNDSENS or $\overline{EN}$=V_{IN}		±0.01	±1	μA
BATTERY CHARGER						
Trickle Charge Threshold	V_{TRIKL}	V_{BAT} Rising Measured from BATSENS to GNDSENS	2.8	2.9	3.0	V
		V_{BAT} Falling Measured from BATSENS to GNDSENS	2.55	2.65	2.75	V
Trickle Charge Current	I_{TRIKL}	V_{BAT} = 2V	35	50	65	mA
Deglitch Time For Trickle Charge To Current Mode Charge Transition	$t_{DGL(TRIKL)}$			5		mS
Current Mode Charge Current	I_{BAT}	R_{PROG} = 560Ω, V_{BAT} =3.5V	1.8	2	2.2	A
		R_{PROG} = 1.13k, V_{BAT} =3.5V	0.9	1	1.1	A
		Shutdown, $\overline{EN}$= V_{IN}			±5	μA
PROG Pin Voltage	V_{PROG}	R_{PROG} = 560Ω,Current Mode		1.200		V
V_{BAT} Regulated Float Voltage	V_{FLOAT}	Measured from BATSENS to GNDSENS	-1		1	%
IDET Pin Voltage	V_{IDET}	R_{IDET} = 560Ω		1.200		V
IDET Threshold	I_{IDET}	R_{IDET} = 560Ω	150	200	250	mA
Deglitch Time For IDET	$t_{DGL(IDET)}$	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL}=100ns		5		mS
Recharge Battery Threshold Voltage	V_{RECHRG}	V_{FLOAT} – V_{RECHRG}.V_{BAT} Falling Measured from BATSENS to GNDSENS	50	100	150	mV
Deglitch Time For Recharge	$t_{DGL(RECHRG)}$	V_{BAT} Falling Below V_{RECHRG}, Measured from BATSENS to GNDSENS	4			mS
Recharge Time	t_{RECHRG}	Percent of Desired Taper Timer Charge Time		50		%

■ ELECTRICAL CHARACTERISTICS(continued)

V_{IN}=5V, $V_{\overline{EN}}$=0V, R_{PROG}=560Ω, R_{IDET}=560Ω, T_A=25℃, unless otherwise specified

STATUS OUTPUT						
$\overline{CHRG}$ Pin Weak Pull-Down Current	$I_{WPD-\overline{CHRG}}$	$V_{\overline{CHRG}}$=1V	15	30	50	μA
$\overline{CHRG}$ Pin Low-level Output Voltage	$V_{OL-\overline{CHRG}}$	$I_{\overline{CHRG}}$=5mA(sink current)		0.1	0.4	V
$\overline{CHRG}$ Pin Leakage Current	$I_{\overline{CHRG}-LEAK}$	When output FET is off, $V_{\overline{CHRG}}$=5V			1	μA
$\overline{CHRG}$ Pin Pulse Frequency	$f_{\overline{CHRG}-FLASH}$	Battery Temperature Fault, C_{TIMER}=0.1μF		1.5		Hz
$\overline{CHRG}$ Pin Pulse Width	$t_{\overline{CHRG}-PULSE}$	Battery Temperature Fault, C_{TIMER}=0.1μF		333		mS
FAULT Pin Low-level Output Voltage	$V_{OL-FAULT}$	1mA Load			0.4	V
FAULT Pin High-level Output Voltage	$V_{OH-FAULT}$	1mA Load	4.6			V
INPUT PROTECTION						
V_{IN} Undervoltage Lockout Voltage	V_{UVL}	V_{IN} Rising, Measured from $V_{INSENSE}$ to GNDSENS	2.9		3.1	V
V_{IN} Undervoltage Lockout Hysteresis	ΔV_{UVL}	Measured from $V_{INSENSE}$ to GNDSENS		200		mV
Sleep-mode Entry Threshold	V_{SLP}	$V_{INSENSE}$ – $V_{BATSENS}$ Falling (Turn-Off), $V_{BATSENS}$=4V	250	300	350	mV
Sleep-mode Exit Hysteresis	$V_{(SLP\_EXIT)}$	$V_{INSENSE}$ – $V_{BATSENS}$ Rising (Turn-On), $V_{BATSENS}$=4V	300	350	400	mV
Deglitch time for $V_{INSENSE}$ rising above $V_{BATSENS}$ + $V_{(SLP\_EXIT)}$		Rising voltage, 2-mV over drive, t_{RISE}=100nS		5		mS
Input DPM Threshold	V_{IN_DPM}	**Note2**	4.3	4.5	4.7	V
Battery OVP Threshold Voltage	$V_{(BOVP)}$	$V_{BATSENS}$ threshold over V_{FLOAT} to turn off charger during charge	102	105	108	%V of V_{FLOAT}
VB_{OVP} Hysteresis	$V_{(BOVP-HYS)}$	Lower limit for $V_{BATSENS}$ falling from above $V_{(BOVP)}$		5		%V of V_{FLOAT}
Battery Short Circuit Threshold Voltage	$V_{(BATSHRT)}$	$V_{BATSENS}$ rising, 100 mV hysteresis		1.8		V
Battery Short Circuit Current	$I_{(BATSHRT)}$		35	50	65	mA
Safety Timer Accuracy	t_{TIMER}	C_{TIMER} = 0.1μF		±10		%
Low-Battery Trickle Charge Time	t_{TRIKL}	Percent of Desired Taper Timer Charge Time, V_{BAT}< 3.1V, Measured Using BATSENS and GNDSENS Pins		25		%

■ ELECTRICAL CHARACTERISTICS(continued)

V_{IN}=5V, $V_{\overline{EN}}$=0V, R_{PROG}=560Ω, R_{IDET}=560Ω, T_A=25℃, unless otherwise specified

Soft-Start Ramp Current	I_{SS}	V_{BAT}< V_{FLOAT} – 100mV, V_{BAT} Across BATSENS and GNDSENS Pins	6	12.8	16	μA
THERMAL SHUTDOWN PROTECTION						
Thermal Shutdown	T_{TSD}			160		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C
OSCILLATOR						
Oscillator Frequency	f_{osc}		1.2	1.5	1.8	MHz
Maximum Duty Cycle	D_{MAX}				100	%
Minimum Duty Cycle	D_{MIN}		0			%
POWER SWITCH						
P-CH MOSFET On Resistance	R_{PFET}	Measured from PV_{IN} to SW		115		mΩ
N-CH MOSFET On Resistance	R_{NFET}	Measured from SW to PGND		110		mΩ
P- CHMOSFET Leakage Current	I_{LKG}	$V_{\overline{EN}}$=V_{IN}=5V, V_{SW}=0V		±0.01	±1	μA
N- CHMOSFET Leakage Current		$V_{\overline{EN}}$=V_{IN}=V_{SW}=5V		±3	±10	μA
Cycle by Cycle Current Limit	I_{CL}			3.5		A
Reverse Leakage Current (Measured from SW to PV_{IN})	$I_{REV-LEAK}$	$\overline{EN}$=H or L, PV_{IN}=0V, V_{SW}=5V			1	μA
BATTERY-PACK NTC MONITOR						
NTC Pin Hot Temperature Fault Threshold	V_{HOT}	From NTC to GNDSENS Pin Falling Threshold		0.29 $V_{INSENSE}$		%
		From NTC to GNDSENS Pin Rising Threshold		0.30 $V_{INSENSE}$		%
NTC Pin Cold Temperature Fault Threshold	V_{COLD}	From NTC to GNDSENS Pin Rising Threshold		0.74 $V_{INSENSE}$		%
		From NTC to GNDSENS Pin Falling Threshold		0.72 $V_{INSENSE}$		%
NTC Disable Threshold	$V_{(NTCDIS)}$	From NTC to GNDSENS Pin Falling Threshold	0.015 $V_{INSENSE}$	0.020 $V_{INSENSE}$	0.025 $V_{INSENSE}$	%
NTC Disable Hysteresis	$\Delta V_{(NTCDIS-HYS)}$	From NTC to GNDSENS Pin		0.010 $V_{INSENSE}$		%
Deglitch time for NTC change				5		mS

Note 1: Operation with current limited wall adapters is allowed down to the V_{IN_DPM} threshold.
Note 2: In order to prevent the input power supply from drooping too low and either crash the rest of the system and/or disable the charger, the charger's V_{IN_DPM} feature may reduce the charge current to prevent the input from dropping below the V_{IN_DPM} threshold.

■ TYPICAL APPLICATION CIRCUITS

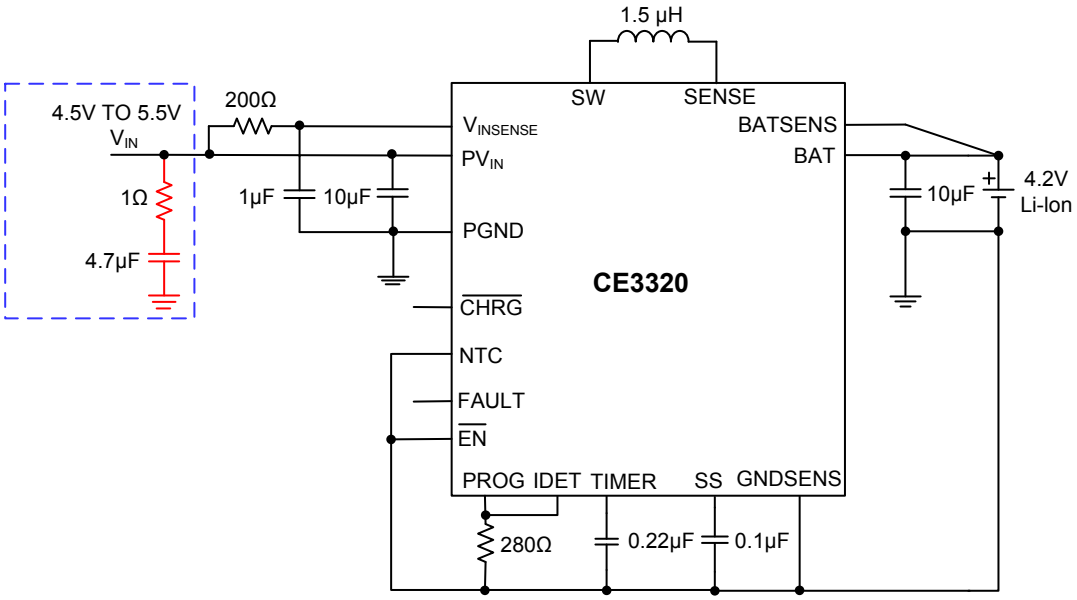


Figure1 Typical Application Circuit

■ BLOCK DIAGRAM

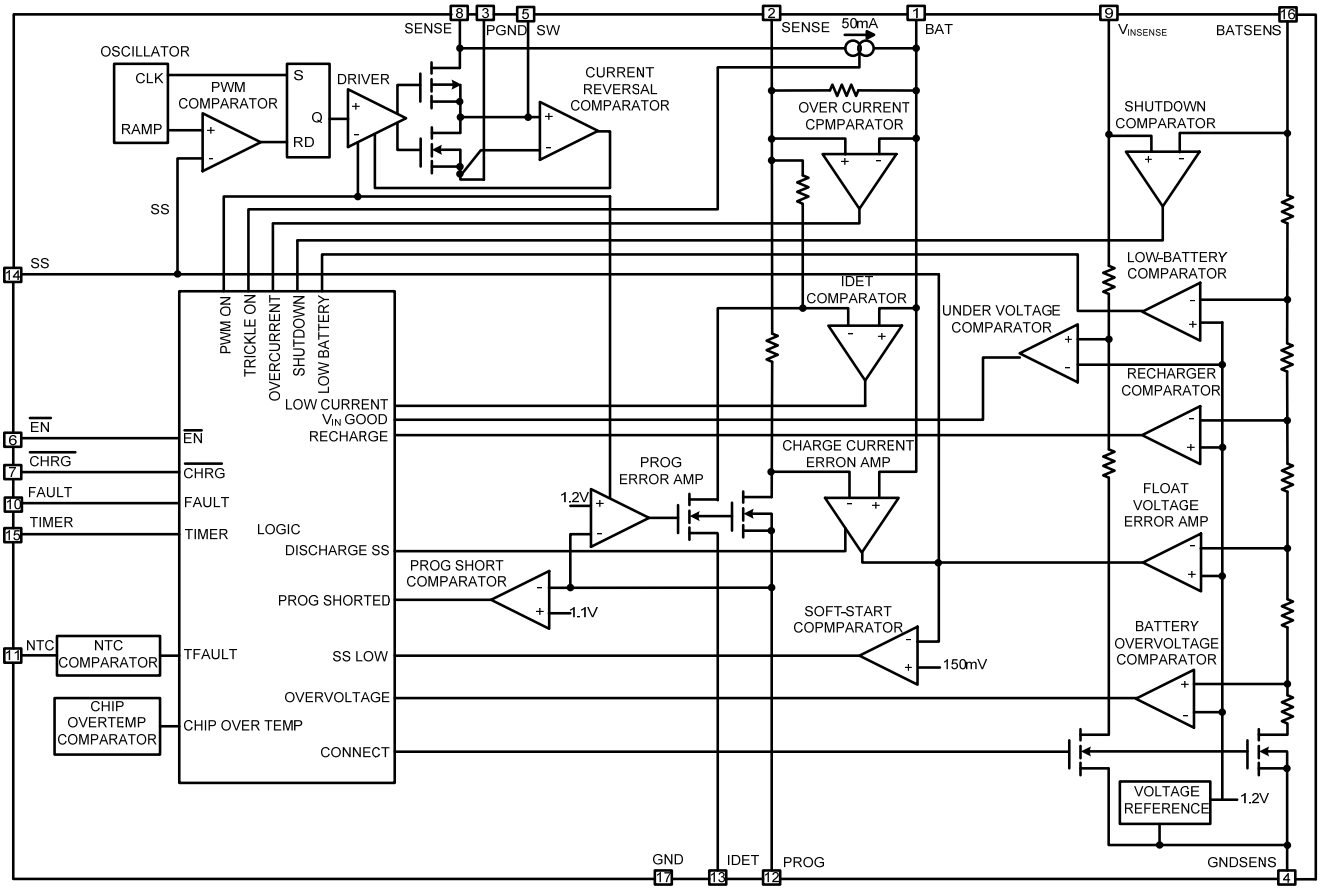


Figure 2 Functional Block Diagram

■ OPERATION

The CE3320 is a constant current, constant voltage Li-Ion battery charger based on a synchronous buck architecture. Low power dissipation makes continuous high rate (2A) battery charging practical. The battery DC charge current is programmed by a resistor R_{PROG} (or a DAC output current) at the PROG pin.

Linear vs. Switching Battery Charging

The CE3320 performs battery charging using the benefits of the step-down or "buck" architecture to multiply the input current when stepping down the output voltage. This property is expressed mathematically in the comparison below, and provides the ability to maximize battery charging from current limited devices, as well as greatly decrease power and heat related dissipation.

Linear Charging

Linear charge current relationship(1):

$$I_{BATL} \approx I_{IN}$$

Note(1): Equation does not take into account thermal foldback.

Efficiency of linear charger:

$$\eta_L = \frac{V_{BAT}}{V_{IN}}$$

Switch-Mode Charging

Switch-mode current relationship:

$$I_{BATS} = \frac{\eta_S \bullet V_{IN} \bullet I_{IN}}{V_{BAT}}$$

Where η_S is estimated with 90%.

Example: Power Savings

Conventional Linear Charger IC: $P_{DL} = (V_{IN}-V_{BAT}) \bullet I_{BAT} = (5V-3.5V) \bullet 1A = 1.5W$

Switch-Mode Charger IC:

$$P_{DS} = \frac{V_{BAT} \bullet I_{BAT}}{\eta_S} - V_{BAT} \bullet I_{BAT} = \frac{3.5V \bullet 1A}{0.9} - 3.5V \bullet 1A = 3.89W - 3.5W = 0.39W$$

Battery Charging

Charging begins when the V_{IN} voltage rises above the UVLO level (approximately 3.0V), V_{IN} is 250mV greater than the battery voltage and $\overline{EN}$ is low. At the beginning of the charge cycle, if the battery voltage is less than the trickle charge threshold, 2.65V, the charger goes into trickle charge mode and delivers approximately 50mA to the battery using a linear charger. If the battery voltage stays low for more than one quarter of the taper timer time, the battery is considered faulty, the charge cycle is terminated and the FAULT pin produces a logic high output.

When the battery voltage exceeds the trickle charge threshold, the low rate linear charger is turned off and the high rate PWM charger ramps up (based on the SS pin capacitance) reaching its full-scale constant current (set via the PROG pin). When the battery approaches the float voltage, the charge current will start to decrease. When the charge current drops below the charge rate detection threshold (set via the IDET pin) for more than 5ms, an internal comparator turns off the internal pull-down N-channel MOSFET at the $\overline{CHRG}$ pin, and connects a weak current source (30μA typical) to ground to indicate a near end-of-charge condition.

Taper timer charging time is set by an external capacitor connected to the timer pin. After time out occurs, the charge cycle is terminated and the $\overline{CHRG}$ pin is forced to a high impedance state. To restart the charge cycle, remove and reapply the input voltage, or momentarily shut the charger down via the $\overline{EN}$ pin. Also, a new charge cycle will begin if the battery voltage drops below the recharge threshold voltage(100mV below the float voltage). The taper timer charging time of a recharge cycle lasts only one-half of the normal taper timer charging time.

A negative temperature coefficient (NTC) thermistor located close to the battery pack can be used to monitor battery temperature and suspend charging when battery temperature is out of the 0°C to 50°C window. A temperature fault drives the FAULT pin high and makes the $\overline{CHRG}$ pin blink. When the input voltage (V_{IN}) is present, the charger can be shut down by pulling the $\overline{EN}$ pin up.

IDET Blanking

The IDET comparator provides an end-of-charge indication by sensing when battery charge current is less than the IDET threshold. To prevent a false end-of-charge indication from occurring during soft-start, this comparator is blanked until the battery voltage approaches the float voltage.

Automatic Battery Recharge

After the charge cycle is completed and if both the battery and the input power supply (wall adapter) are still connected, a new charge cycle will begin if the battery voltage drops below V_{RECHRG} due to self-discharge or external loading. This will keep the battery near maximum capacity at all times without manually restarting the charge cycle.

In some applications such as battery charging in GPRS cell phones, large load current transients may cause battery voltage to momentarily drop below the recharge threshold. To prevent these transients from initiating are charge cycle when it is not needed, the output of the recharge comparator is digitally qualified. Only if the battery voltage stays below the recharge threshold for at least 4ms will battery recharging occur. (GPRS qualification is available even if time out is disabled.)

Battery Charging Profile

There are four loops that influence the charge current:

- Constant current loop (CC)
- Constant voltage loop (CV)
- Input-voltage dynamic power management loop (V_{IN-DPM})
- Cycle by Cycle current limit

During the charging process, all the four loops are enabled and the one that is dominant takes control.

The CE3320 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications.

Figure 3 illustrates the entire battery charging profile, which consists of three phases:

1. Preconditioning-Current Mode (Trickle) Charge - Linear Mode.
2. Constant-Current Mode(Fast) Charge - Switching Mode.
3. Constant-Voltage Mode (Taper) Charge - Switching Mode.

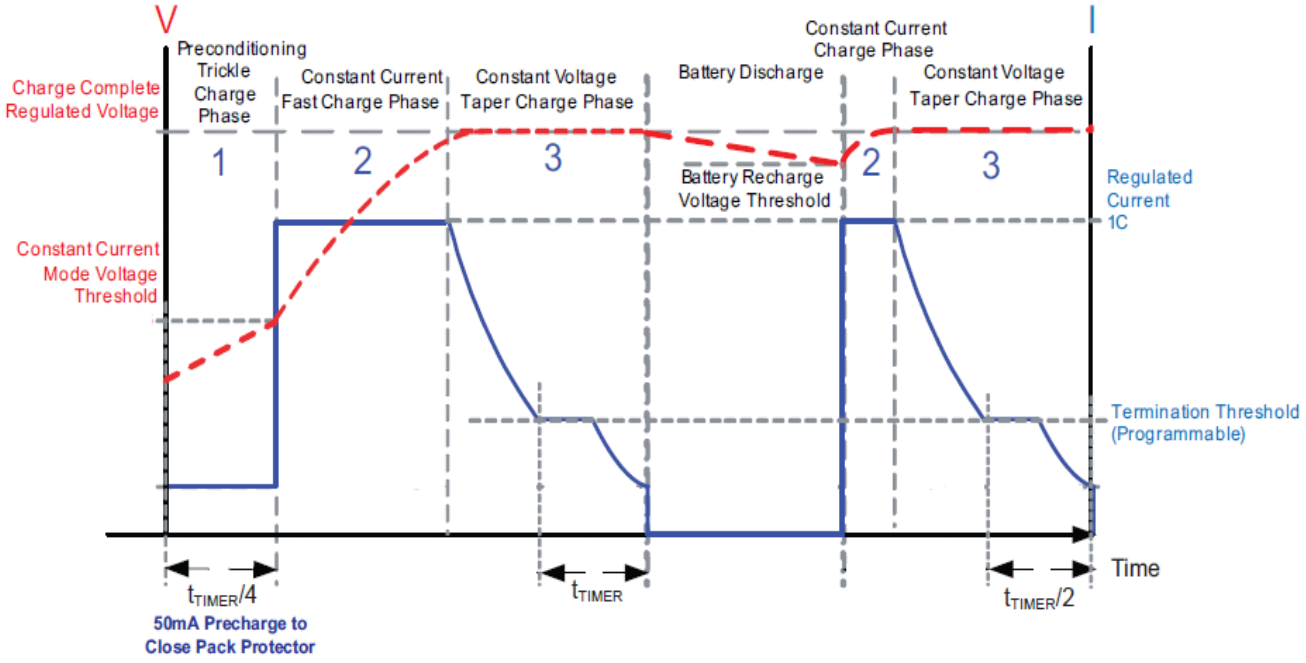


Figure 3: Charging Current and Battery Voltage vs Time

■ TYPICAL PERFORMANCE CHARACTERISTICS

(T_A=25℃, unless otherwise specified, Test Figure1 above)

Oscillator Frequency vs V_{IN}

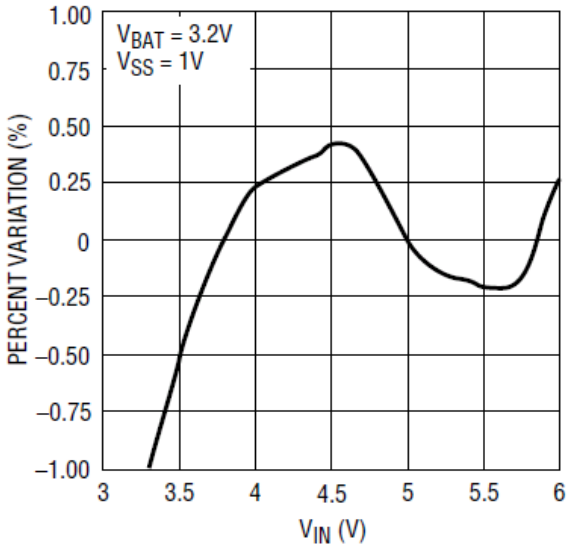


Figure 4

Oscillator Frequency vs Temperature

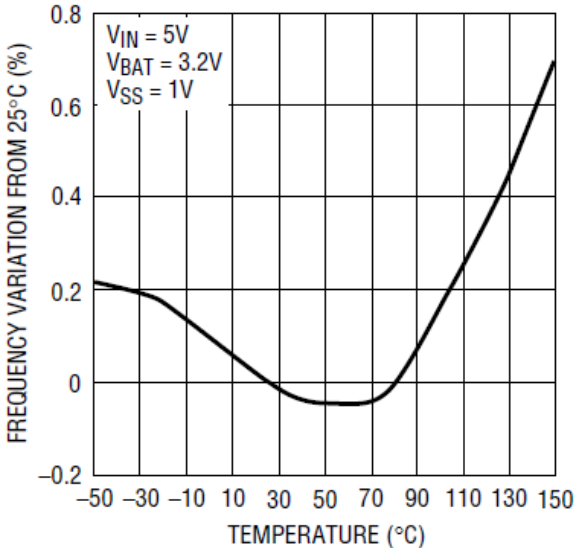


Figure5

Power Loss vs V_{BAT} Charging (PWM Mode)

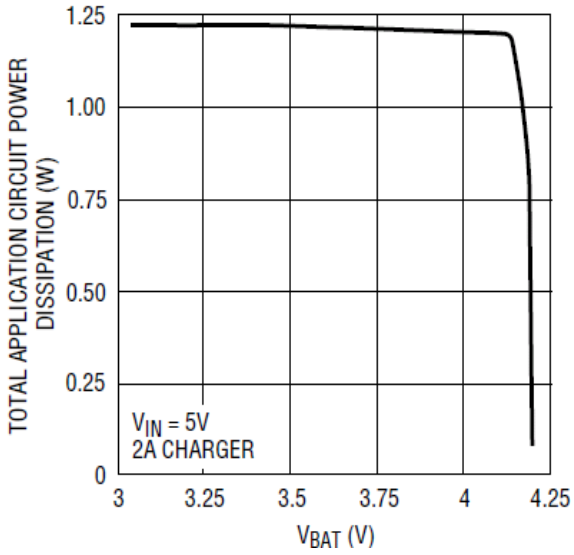


Figure 6

Dissipation of Figure 36 Circuit vs I_{BAT}

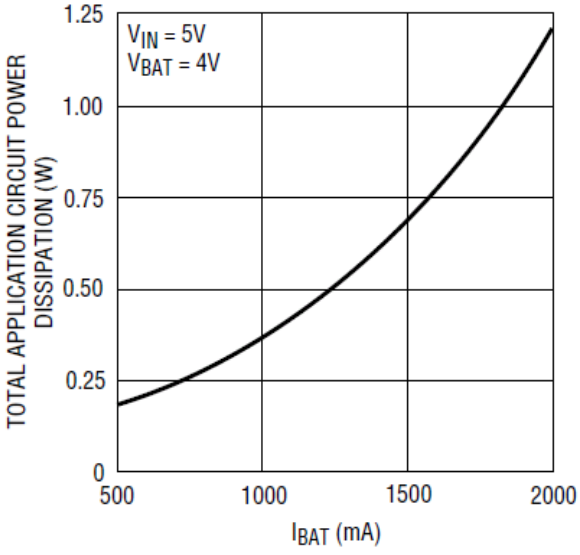


Figure7

■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A =25℃, unless otherwise specified, Test Figure1 above)

Dissipation of Figure 36 Circuit vs V_{IN}

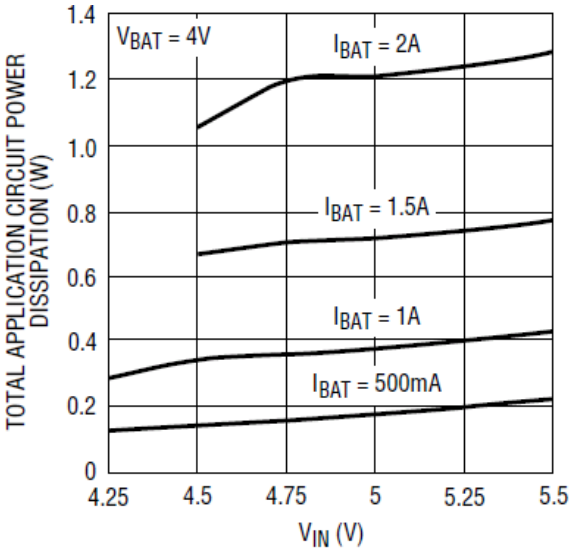


Figure 8

Trickle Charge Current vs V_{BAT}

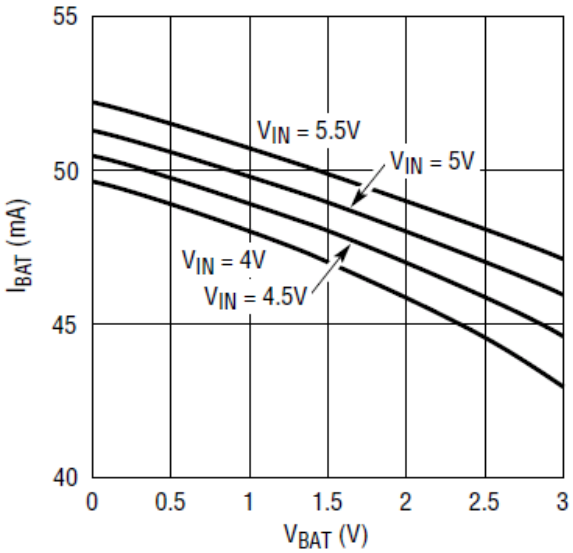


Figure9

PROG Pin Characteristic(V_{PROG} vs I_{PROG})

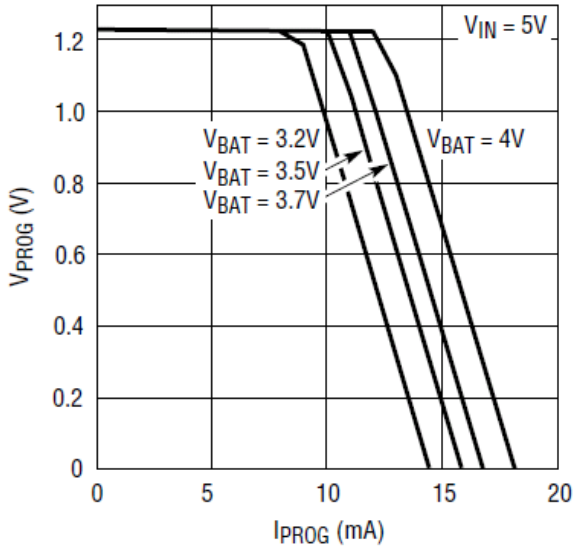


Figure 10

IDET Threshold vs R_{IDET} for R_{PROG}=560Ω

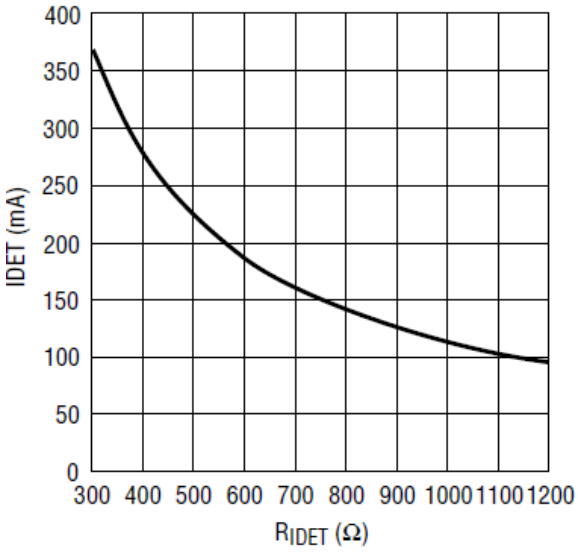


Figure 11

■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A =25℃, unless otherwise specified, Test Figure1 above)

Output Charging Characteristic Showing Constant Current and Constant Voltage

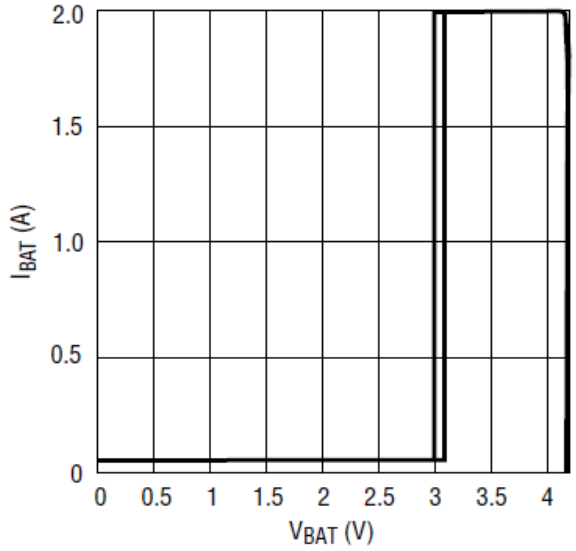


Figure 12

V_{FLOAT} and Recharge Battery Operation Threshold Voltage vs Temperature

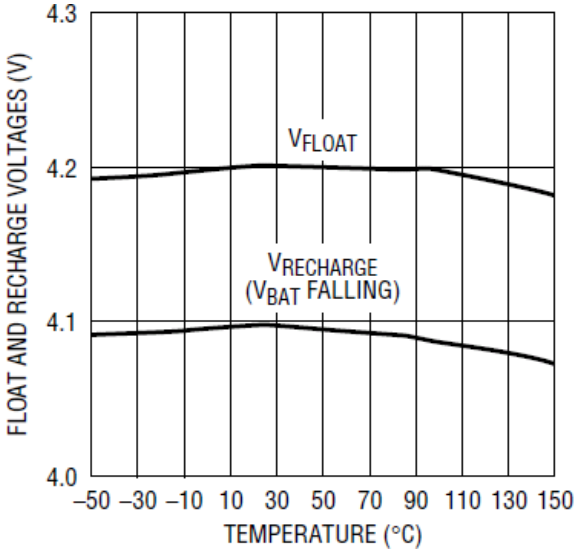


Figure 13

$\overline{CHRG}$ Pin Temperature Fault Behavior (Detail)

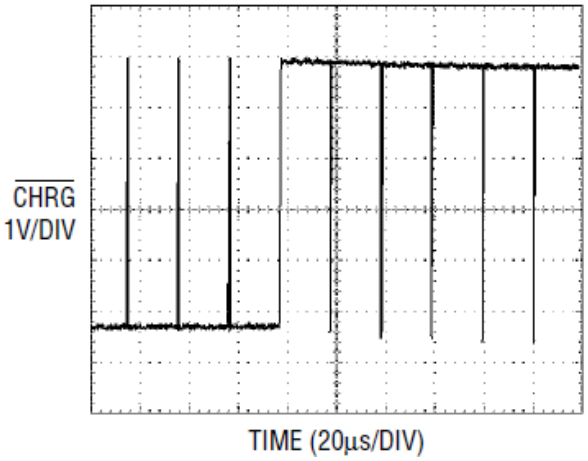


Figure 14

Soft-Start (PWM Mode)

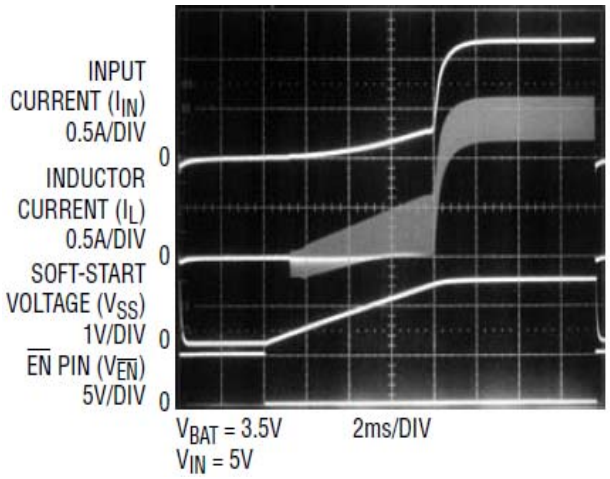


Figure 15

■ APPLICATION INFORMATION

Because of the high integration in the CE3320 IC, the application circuit based on this Synchronous Buck Li-Ion Charger IC is rather simple. Only low profile external components need to be selected for the targeted application specifications.

Soft-Start and Compensation Capacitor Selection

The CE3320 has a low current trickle charger and a PWM-based high current charger. Soft-start is used whenever the high rate charger is initially turned on, preventing high start-up current. Soft-start ramp rate is set by the internal 12.8μA pull-up current and an external capacitor from SS to GNDSENS. The control range on the SS pin is approximately 0.3V to1.6V. With a 0.1μF capacitor, the time to ramp up to maximum duty cycle is approximately 10ms.

The external capacitor on the SS pin also sets the compensation for the current control loop and the float voltage control loop. A minimum capacitance of 10nF is required.

Trickle Charge And Defective Battery Detection

While monitoring the charge cycle, the CE3320 utilizes a charge safety timer to help identify defective cells and to ensure that the battery is charged safely. Operation is as follows:

At the beginning of a charge cycle, if the battery voltage is low (below 2.65V), the charger goes into trickle charge reducing the charge current to 50mA. If the low battery voltage persists for one quarter of the taper timer charging time, the battery is assumed to be defective, the charge cycle is terminated, the $\overline{CHRG}$ pin output assumes a high impedance state, and the FAULT pin pulls high. The fault can be cleared by toggling V_{CC}, temporarily forcing the $\overline{EN}$ pin to high, or temporarily forcing the BAT pin voltage above 2.9V.

If the battery voltage exceeds the trickle charge threshold of 2.9V(typ.) prior to the expiration of the timer, the charge cycle proceeds into fast charge. Two time out periods of 37.5 minutes for Trickle Charge mode and 2.5 hours for Constant Voltage Taper mode.

Mode	Time
Trickle Charge (TC) Time Out	37.5 minutes
Constant Voltage (CV) Mode Taper Time Out, $I_{BAT}<I_{IDET}$	2.5 hours

Table 1. Summary for a 0.22μF Ceramic Capacitor Used for the Timer Capacitor

Charge Current and IDET Programming

The CE3320 has two different charge modes. If the battery is severely depleted (battery voltage less than 2.65V) a 50mA trickle current is initially used. If the battery voltage is greater than the trickle charge threshold, high rate charging is used. This higher charge current is programmable and is approximately 935 times the current delivered by the PROG pin. This current is usually set with an external resistor from PROG to GNDSENS, but it may also be set with a current output DAC connected to the PROG pin. The voltage on the PROG pin is nominally 1.2V.

For 2A charge current:

$$R_{PROG} = \frac{935 \bullet 1.2V}{2A} \cong 560\Omega$$

Using a 1% tolerance metal film resistor for R_{PROG} will improve the charge current accuracy and to avoid issues with the R_{PROG} short test when using the maximum charge current setting.

The IDET threshold (a charge current threshold used to determine when the battery is nearly fully charged) is programmed in much the same way as the PROG pin, except that the IDET threshold is 93.5 times the current delivered by the IDET pin. This current is usually set with an external resistor from IDET

to GNDSENS, but it may also be set with a current output DAC. The voltage on the IDET pin is nominally 1.2V.

For 200mA IDET current (corresponding to C/10 for a 2AHr battery):

$$R_{IDET} = \frac{93.5 \bullet 1.2V}{0.2A} \cong 560\Omega$$

1.13kΩ programs approximately 100mA and 280Ω approximately 400mA.

Using a 1% tolerance metal film resistor for R_{IDET} will improve the end-of-charge (IEDT) current threshold accuracy.

For applications where IDET is set to one tenth of the high rate charge current, and slightly poorer charger current and IDET threshold accuracy is acceptable, the PROG and IDET pins may be tied together and a single resistor, R1,can program both (Figure 16).

$$R1 = \frac{467.5 \bullet 1.2}{I_{CHARGE}}$$

and

$$IDET = \frac{I_{CHARGE}}{10}$$

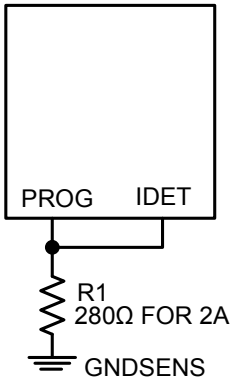


Figure 16. Programming Charge Current and IDET Threshold with a Single Resistor

The equations for calculating R1 (used in single resistor programming) differ from the equations for calculating R_{PROG} and R_{IDET} (2-resistor programming) and reflect the fact that the current from both the IDET and PROG pins must flow through a single resistor R1 when a single programming resistor is used.

Programming The Timer

The programmable timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER pin, C_{TIMER}, to GNDSENS.. The taper timer charging time is:

Time(Hours)=C_{TIMER}/0.09μF or C_{TIMER}=Time(Hours)•0.09μF

where time is the desired taper timer charging time.

The TIMER pin is driven by a constant current source and will provide a linear response to increases in the timer capacitor value. Thus, if the timer capacitor were to be doubled from the nominal 0.1μF value, the time-out periods would be doubled.

The TIMER pin should not be left floating or unterminated, as this will cause errors in the internal timer control circuit. The constant current provided to charge the timer capacitor is very small, and this pin is susceptible to noise and changes in capacitance value. Therefore, the timer capacitor should be physically located on the printed circuit board layout as close as possible to the TIMER pin. Since the accuracy of the internal timer is dominated by the capacitance value, a 10% tolerance or better ceramic capacitor is recommended. Ceramic capacitor materials, such as X7R and X5R types, are a good choice for this application.

The timer starts when an input voltage greater than the undervoltage lockout threshold level is applied and the $\overline{EN}$ pin is lower than the chip enable threshold voltage level. After a time-out occurs, the charge current stops, and the $\overline{CHRG}$ output assumes a high impedance state to indicate that the charging has stopped. Connecting the TIMER pin to IDET disables the timer function. Connect this pin to GNDSENS to end battery charging when I_{BAT} drops below the I_{DET} charge rate threshold.

Hardware Chip Enable Input ($\overline{EN}$)

The CE3320 contains a $\overline{EN}$ input. Drive $\overline{EN}$ low to enable charge and enter normal operation.

At any point in the charge cycle, the CE3320 can be put into shutdown mode by driving the $\overline{EN}$ pin high. This reduces the battery drain current to less than 3μA and the supply current to less than 50μA. When in shutdown mode, the $\overline{CHRG}$ pin is in the high impedance state. Driving $\overline{EN}$ high during DEFAULT mode resets the safety timer.

A new charge cycle can be initiated by driving the $\overline{EN}$ pin low. A resistor pull-down on this pin forces the CE3320 to be enabled if the pin is allowed to float.

Input Voltage Protection in Charge Mode

Undervoltage Lockout

Internal undervoltage lockout circuits monitor V_{IN} and keep the charger circuits shut down until V_{IN} rises above the undervoltage lockout threshold. The UVLO has a built-in hysteresis of 200mV.

Sleep Mode

The CE3320 enters the low-power sleep mode if the voltage on $V_{INSENSE}$ falls below sleep-mode entry threshold, $V_{BATSENS}+V_{SLP}$, and $V_{INSENSE}$ is higher than the undervoltage lockout threshold, V_{UVL}. This feature prevents reverse current draining from the battery during the absence of $V_{INSENSE}$. When $V_{INSENSE}< V_{BATSENS}+V_{SLP}$, the CE3320 turns off the PWM converter. Once $V_{INSENSE} > V_{BATSENS} + V_{(SLP\_EXIT)}$, the device initiates a new charge cycle.

Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage will decease. Once the supply drops to V_{IN_DPM} (typically 4.5V), the input current limit is reduced down to prevent further supply droop. When the IC enters this mode, the charge current is lower than the set value . This feature ensures IC compatibility with adapters with different current capabilities without a hardware change.

Battery Protection in Charge Mode

Output Overvoltage Protection

The CE3320 provides a built-in overvoltage protection to protect the device and other components against damage if the battery voltage goes too high. A comparator turns off both chargers (high rate and trickle) if battery voltage exceeds the float voltage V_{FLOAT} by approximately 5%. This may occur in situations where the battery is accidentally disconnected while battery charging is underway. Once $V_{BATSENSE}$ drops to the battery overvoltage exit threshold, the fault is cleared and charge process back to normal.

Battery Short Protection

During the normal charging process, if the battery voltage is lower than the short-circuit threshold, $V_{(BATSHRT)}$, the charger operates in linear charge mode with a lower charge rate of $I_{(BATSHRT)}= I_{TRIKL}$ as shown in Figure 2.

Short-Circuit Current Protection

Short-circuit protection is provided in several different ways. First, a hard short on the battery terminals will cause the charge to enter trickle charge mode, limiting charge current to the trickle charge current (typically 50mA). Second, PWM charging is prevented if the high rate charge current is programmed far above the 2A maximum recommended charge current (via the PROG pin). Third, an overcurrent comparator monitors the peak inductor current.

Thermal Shutdown and Protection

During the charging process, to prevent chip overheating, A comparator continuously monitors the junction temperature, T_J, of the die. This may cause a thermal shutdown of the CE3320 if the die temperature rises too high. At any state, if T_J exceeds T_{TSD} (approximately 160°C), CE3320 suspends charging and disables the buck converter. During thermal shutdown mode, the PWM is turned off, the timer is suspended. When T_J falls below T_{TSD} by approximately 20°C, the timer continues where it left off and a new charging cycle resumes.

Charge Cycle Status Output

The CE3320 provides battery charge cycle status via two status pins ($\overline{CHRG}$ and FAULT). $\overline{CHRG}$ pin is internally connected to an N-channel open drain MOSFET. FAULT pin is CMOS output, which can source or sink current. Table 2 describes the status of the charge cycle based on the $\overline{CHRG}$ and FAULT outputs.

FAULT	$\overline{CHRG}$	Description
Low	Low	Charge cycle has started, IDET has not been reached and charging is proceeding normally.
High	FLASH 1.5Hz, 50% Duty Cycle	Charge cycle has started, IDET has not been reached, but the charge current have been paused due to an NTC out-of-temperature condition.
Low	30μA pull down	IDET has been reached and charging is proceeding normally.
High	30μA pull down	IDET has been reached but the charge current have paused due to an NTC out-of-temperature condition.
Low	High	Normal time out (charging has stopped).
High	High	If FAULT goes high and $\overline{CHRG}$ goes high impedance simultaneously, then the CE3320 has timed out due to a bad cell ($V_{BATSENS}$ <3.1V after one-quarter the programmed taper timer charging time). If $\overline{CHRG}$ goes high impedance first, then the CE3220 has timed out normally (charging has stopped), but NTC is indicating an out-of-temperature condition.
Low	High	V_{IN} Undervoltage Lockout Mode
Low	High	Sleep Mode ($V_{INSENSE}$ < $V_{BATSENS}$+V_{SLP})
Low	FLASH Rate depends on output capacitance	①No battery with Charge Enabled ②No battery with Charge Enabled and safety timer disabled
High	Low	Fault Condition (Battery Short Circuit)
Low	30μA pull down	Fault Condition (Battery Overvoltage)

Table 2. $\overline{CHRG}$ and FAULT Status Indicator

These status pins can be used to communicate to the host processor or drive LEDs.
The LEDs should be biased with as little current as necessary to create reasonable illumination, therefore, a ballast resistor should be placed between the LED cathode and the $\overline{CHRG}$ pin. LED current consumption will add to the overall thermal power budget for the device package, hence it is good to keep the LED drive current to a minimum 2mA should be sufficient to drive most low cost red or green LEDs. It is not recommended to exceed 10mA for driving an individual status LED. The required ballast resistor values can be estimated using the following formula:

$$R_{BALLAST} = \frac{V_{IN} - V_{F(LED)}}{I_{LED}}$$

Example:

$$R_{BALLAST} = \frac{5.0V - 2.0V}{2mA} = 1.5K\Omega$$

Note: Red LED forward voltage (V_F) is typically 2.0V@ 2mA.

$\overline{\text{CHRG}}$ Status Output Pin

When a charge cycle starts, the $\overline{\text{CHRG}}$ pin is pulled to ground by an internal N-channel MOSFET which is capable of driving an LED. When the charge current drops below the end-of-charge (IDET) threshold for at least 4ms, and the battery voltage is close to the float voltage, the N-channel MOSFET turns off and a 30μA current source to ground is connected to the $\overline{\text{CHRG}}$ pin. This weak pull down remains until the charge cycle ends. After charging ends, the pin will become high impedance. By using two different value resistors, a microprocessor can detect three states from this pin (charging, end-of-charge and charging stopped). See Figure 17.

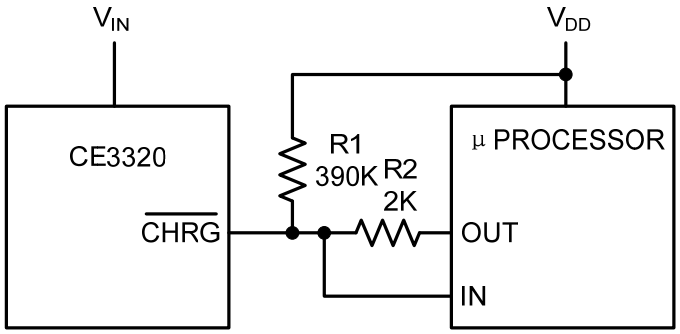


Figure 17. Microprocessor Interface

To detect the charge mode, force the digital output pin, OUT, high and measure the voltage on the $\overline{\text{CHRG}}$ pin. The N-channel MOSFET will pull the pin low even with a 2k pull-up resistor. Once the charge current drops below the end-of-charge threshold, the N-channel MOSFET is turned off and a 30μA current source is connected to the $\overline{\text{CHRG}}$ pin. The IN pin will then be pulled high by the 2k resistor connected to OUT. Now force the OUT pin into a high impedance state, the current source will pull the pin low through the 390k resistor. When charging stops, the $\overline{\text{CHRG}}$ pin changes to a high impedance state and the 390k resistor will then pull the pin high to indicate charging has stopped.

Charge Termination

Battery charging may be terminated several different ways, depending on the connections made to the TIMER pin. For time-based termination, connect a capacitor between the TIMER and GNDSENS pins (C_{TIMER}=Time(Hrs)•0.09μF). Charging may be terminated when charge current drops below the IDET threshold by tying TIMER to GNDSENS. Finally, charge termination may be defeated by tying TIMER to IDET. In this case, an external device can terminate charging by pulling the $\overline{\text{EN}}$ pin high.

Battery Temperature Detection

When battery temperature is out of range (either too hot or too cold)， charging is temporarily halted and the FAULT pin is driven high. In addition, if the battery is still charging at a high rate (greater than the IDET current) when a temperature fault occurs, the $\overline{\text{CHRG}}$ pin NMOS turns on and off at approximately 50kHz, alternating between a high and low duty factor at an approximate rate of 1.5Hz (Figure 18).

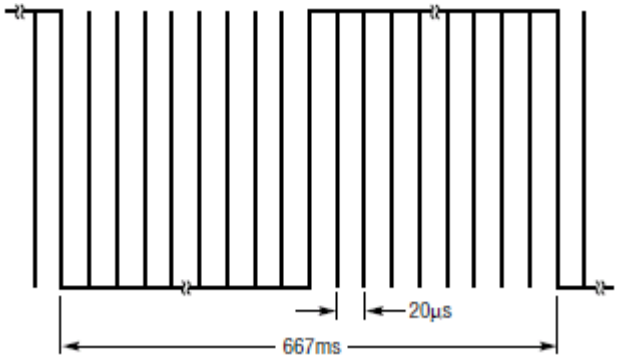


Figure 18. $\overline{\text{CHRG}}$ Temperature Fault Waveform

This provides a low rate visual indication (1.5Hz) when driving an LED from the $\overline{\text{CHRG}}$ pin while providing a fast temperature fault indication (20µseconds typical) to a microprocessor by tying the $\overline{\text{CHRG}}$ pin to an interrupt line. Serrations within this pulse are typically 500ns wide.

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and GNDSENS and the resistor, R_{NOM}, from the NTC pin to $V_{INSENSE}$. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C. The CE3320 goes into hold mode when the resistance, R_{HOT}, of the NTC thermistor drops to 0.41 times the value of R_{NOM}. For instance for R_{NTC} = 10k. (The value for a Vishay NTHS0603N02N1002J thermistor at 25°C) hold occurs at approximately 4.1k, which occurs at 50°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The CE3320 is designed to go into hold mode when the value of the NTC thermistor increases to 2.82 times the value of R_{NOM}. This resistance is R_{COLD}. For the Vishay 10k thermistor, this value is 28.2k, which corresponds toapproximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables the NTC function.

Thermistors

The CE3320 NTC trip points were designed to work with thermistors whose resistance temperature characteristics follow Vishay Dale's "R-T Curve 2." The Vishay NTHS0603N02N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the "R-T Curve 2" characteristic in a variety of sizes. Futhermore, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 7 will also work (Vishay Dale R-T Curve 2 shows a ratio of R_{COLD} to R_{HOT} of 2.815/0.4086 = 6.89).

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 1." Using these as indicated in the NTC Thermistor section will give temperature trip points of approximately 3°C and 47°C, a delta of 44°C.This delta in temperature can be moved in either direction by changing the value of R_{NOM} with respect to R_{NTC}.

Increasing R_{NOM} will move the trip points to higher temperatures. To calculate R_{NOM} for a shift to lower temperature for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \bullet R_{NTC} \text{ at } 25℃$$

where R_{COLD} is the resistance ratio of R_{NTC} at the desired cold temperature trip point. If you want to shift the trip points to higher temperatures, use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.4086} \bullet R_{NTC} \text{ at } 25℃$$

where R_{HOT} is the resistance ratio of R_{NTC} at the desired hot temperature trip point.

Here is an example using a 100k R-T Curve 1 thermistor from Vishay Dale. The difference between trip points is 44°C, from before, and we want the cold trip point to be 0°C, which would put the hot trip point at 44°C. The R_{NOM} needed is calculated as follows:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \bullet R_{NTC} \text{ at } 25℃$$

$$= \frac{3.266}{2.815} \bullet 100\text{K} = 116\text{K}$$

The nearest 1% value for R_{NOM} is 115k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 44°C respectively. To extend the delta between the cold and hot trip points a resistor, R1, can be added in series with R_{NTC} (see Figure 19).

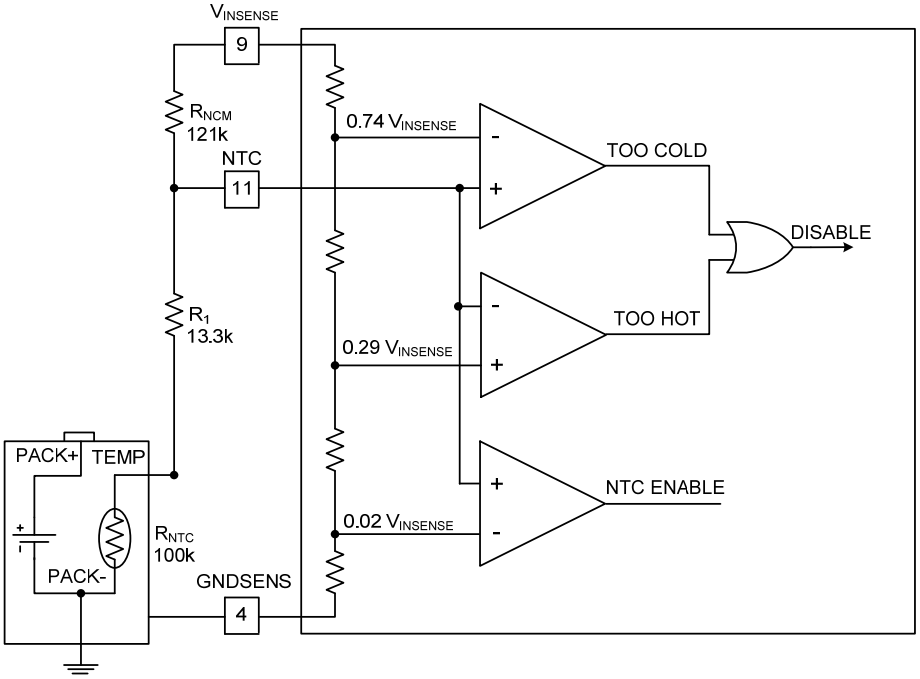


Figure 19. Extending the Delta Temperature

The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086}$$

$$R1 = \frac{0.4086}{2.815 - 0.4086} \bullet (R_{COLD} - R_{HOT}) - R_{HOT}$$

where R_{NOM} is the value of the bias resistor, R_{HOT} and R_{COLD} are the values of R_{NTC} at the desired temperature trip points. Continuing the example from before with a desired hot trip point of 50°C:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086} = \frac{100\text{K} \bullet (3.2636 - 0.3602)}{2.815 - 0.4086}$$

=120.8K, 121K is nearest 1%

$$R1 = 100\text{K} \bullet \left(\frac{0.4086}{2.815 - 0.4086} \bullet (3.266 - 0.3602) - 0.3602\right)$$

=13.3k, 13.3k is nearest 1%

The final solution is as shown if Figure 19 where R_{NOM} =121k, R1 = 13.3k and R_{NTC} = 100k at 25°C.

NTC Layout Considerations

It is important that the NTC thermistor not be in close thermal contact with the CE3320. Because the CE3320 package can reach temperatures in excess of the 50°C trip point, the NTC function can cause a hysteretic oscillation which turns the charge current on and off according to the package temperature rather than the battery temperature. This problem can be eliminated by thermally coupling the NTC thermistor to the battery and not to the CE3320.

NTC Trip Point Errors

When a 1% resistor is used for R_{NOM}, the major error in the 50°C trip point is determined by the tolerance of the NTC thermistor. A typical 10k NTC thermistor has a ±10% tolerance. By looking up the temperature coefficient of the thermistor at 50°C, the tolerance error can be calculated in degrees centigrade.Consider the Vishay NTHS0603N02N1002J thermistor which has a temperature coefficient of –3.3%/°C at 50°C. Dividing the tolerance by the temperature coefficient, ±10%/(3.3%/°C) = ±3°C, gives the temperature error of the hot trip point.

The cold trip point is a little more complicated because its error depends on the tolerance of the NTC thermistor and the degree to which the ratio of its value at 0°C and its value at 50°C varies from 7 to 1. Therefore, the cold trip point error can be calculated using the tolerance, TOL, the temperature coefficient of the thermistor at 0°C, TC (in %/°C), the value of the thermistor at 0°C, R_{COLD}, and the value of the thermistor at 50°C, R_{HOT}. The formula is:

$$\text{Temperature Error}(℃) = \frac{\left(\frac{1+\text{TOL}}{7} \bullet \frac{R_{COLD}}{R_{HOT}} - 1\right) \bullet 100}{\text{TC}}$$

For example, the Vishay NTHS0603N02N1002J thermistor with a tolerance of ±10%, TC of –4.5%/°C, and R_{COLD}/R_{HOT} of 6.89, has a cold trip point error of:

$$\text{Temperature Error}(℃) = \frac{\left(\frac{1\pm0.10}{7} \bullet 6.89 - 1\right) \bullet 100}{-4.5} = -1.8℃, +2.5℃$$

If a thermistor with a tolerance less than ±10% is used, the trip point errors begin to depend on errors other than thermistor tolerance including the input offset voltage of the internal comparators of the CE3320 and the effects of internal voltage drops due to high charging currents.

Selecting Input Bypass Capacitor

The CE3320 uses a synchronous buck regulator to provide high battery charging current. In most applications, all that is needed is a bypass capacitor, typically a 10μF capacitor placed in close proximity to PV_{IN} and PGND pins, works well. The CE3320 is designed to work with both regulated and unregulated external dc supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance has to be added to the input of the charger.

A 10μF chip ceramic capacitor is recommended for the input bypass capacitor, because it provides low ESR and ESL and can handle the high RMS ripple currents. However, some high Q capacitors may produce high transients due to self-resonance under some start-up conditions, such as connecting the charger input to a hot power source. Adding a 1.5Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

Protecting the PV_{IN} Pin from Overvoltage Transients

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors to bypass the PV_{IN} pin, which powered by USB bus or Wall Adapter Input. High voltage transients can be generated under some start-up conditions, depending on the power supply characteristics and cable length, such as when the USB or wall adapter is hot plugged. When power is supplied via the USB bus or wall adapter, the cable inductance along with the self resonant and high Q characteristics of some types of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage pin ratings and damage the CE3320. The long cable lengths of most wall adapters and USB cables makes them especially susceptible to this problem. To bypass the PV_{IN} pin, add a 1Ω resistor in series with an X5R ceramic capacitor to lower the effective Q of the network and greatly reduce the ringing. A tantalum, OS-CON, or electrolytic capacitor can be used in place of the ceramic and resistor, as their higher ESR reduces the Q, thus reducing the voltage ringing.

The oscilloscope photograph in Figure 20 shows how serious the overvoltage transient can be for the USB and wall adapter inputs. For both traces, a 5V supply is hot-plugged using a three foot long cable. For the top trace, only a 4.7μF capacitor (without the recommended 1Ω series resistor) is used to locally

bypass the input. This trace shows excessive ringing when the 5V cable is inserted, with the overvoltage spike reaching 10V. For the bottom trace, a 1Ω resistor is added in series with the 4.7µF capacitor to locally bypass the 5V input. This trace shows the clean response resulting from the addition of the 1Ω resistor.

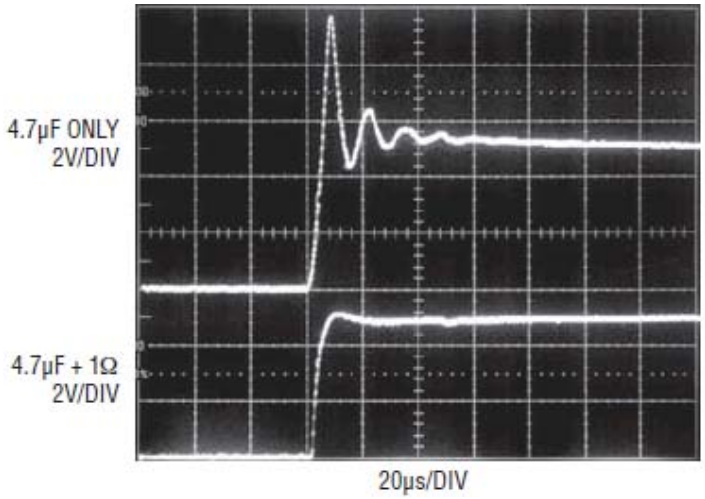


Figure 20. Waveforms Resulting from Hot-Plugging a 5V Input Supply

Even with the additional 1Ω resistor, bad design techniques and poor board layout can often make the overvoltage problem even worse. System designers often add extra inductance in series with input lines in an attempt to minimize the noise fed back to those inputs by the application. In reality, adding these extra inductances only makes the overvoltage transients worse. Since cable inductance is one of the fundamental causes of the excessive ringing, adding a series ferrite bead or inductor increases the effective cable inductance, making the problem even worse. For this reason, **do not** add additional inductance (ferrite beads or inductors) in series with the USB or wall adapter inputs. For the most robust solution, 6V transorbs or zener diodes may also be added to further protect the USB and wall adapter inputs. Two possible protection devices are the SM2T from ST Microelectronics and the EDZ series devices from ROHM.

Always use an oscilloscope to check the voltage waveforms at the PV_{IN} pin during USB and wall adapter hot-plug events to ensure that overvoltage transients have been adequately removed.

Selecting Output Bypass Capacitor

The CE3320 provides internal loop compensation. Using this scheme, the CE3320 is stable with 10µF to 200µFof local capacitance. The capacitance on the BAT rail can be higher if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor which provides low ESR and ESL and can handle the high RMS ripple currents, with the capacitance between 10µF and 47µF is recommended for local bypass to BAT. A 47µF bypass capacitor is recommended for optimal transient response.
EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 1.5MHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of the output capacitor is 0.1Ω and the battery impedance is raised to 2Ω with a bead or inductor, only 5% of the ripple current will flow in the battery. Similar techniques may also be applied to minimize EMI from the input leads.

Inductor Selection

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. A high (1.5MHz) operating frequency was chosen for the buck switcher in order to minimize the size of the inductor. However, take care to use inductors with low core losses at this frequency. The CE3320 is designed to work with 1.5µH to 2.2µH inductors. The

chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.
A good choice is the IHLP-2525AH-01from Vishay Dale.
To calculate the inductor ripple current:

$$\Delta I_L = \frac{V_{BAT}}{L \bullet f_{OSC}} \bullet \left(1 - \frac{V_{BAT}}{V_{IN}}\right) = \frac{V_{BAT} - \frac{{V_{BAT}}^2}{V_{IN}}}{L \bullet f_{OSC}}$$

where V_{BAT} is the battery voltage, V_{IN} is the input voltage, L is the inductance and f is the PWM oscillator frequency (typically 1.5MHz). Maximum inductor ripple current occurs at maximum V_{IN} and $V_{BAT} = V_{IN}/2$. Peak inductor current will be:

$$I_{PK} = I_{BAT} + 0.5 \bullet \Delta I_L$$

where I_{BAT} is the maximum battery charging current.
When sizing the inductor make sure that the peak current will not exceed the saturation current of the inductors.
Also, ΔI_L should never exceed 0.4(I_{BAT}) as this may interfere with proper operation of the output short-circuit protection comparator. 1.5µH provides reasonable inductor ripple current in a typical application. With 1.5µH and 2A charge current:

$$\Delta I_L = \frac{2.85V - \frac{(2.85V)^2}{V_{IN}}}{1.5\mu H \bullet 1.5MHz} = 0.61A_{P-P}$$

and

$$I_{PK} = 2.31A$$

Due to the high currents possible with the CE3320, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 2A DC load with peaks at 2.31A 20% of the time, a Δ40°C temperature rise current must be greater than 2.62A:

$$I_{TEMPRISE} = I_{BAT} + D \bullet (I_{PK} - I_{BAT}) = 2A + 0.2 \bullet (2.31 - 2A) = 2.62A$$

Remote Sensing-Kelvin Sensing the Battery

The internal P-channel MOSFET drain is connected to the BAT pin, while the BATSENS pin connects through an internal precision resistor divider to the input of the constant-voltage amplifier. This architecture allows the BATSENS pin to Kelvin sense the positive battery terminal. This is especially useful when the copper trace from the BAT pin to the Li-Ion battery is long and has a high resistance. High charge currents can cause a significant voltage drop between the positive battery terminal and the BAT pin. In this situation, a separate trace from the BATSENS pin to the battery terminals will eliminate this voltage error and result in more accurate battery voltage sensing. **The BATSENS pin MUST be electrically connected to the BAT pin.**
For highest float voltage accuracy, tie GNDSENS and BATSENS directly to the battery terminals. In a similar fashion, tie BAT and PGND directly to the battery terminals. This eliminates IR drops in the GNDSENS and BATSENS lines by preventing charge current from flowing in them.

USB Charge Reduction

In many instances, product system designers do not know the real properties of a potential port to be used to supply power to the battery charger. Typical powered USB ports commonly found on desktop and notebook PCs should supply up to 500mA(USB2.0) or 900mA(USB3.0). In the event a port being used to supply the charger is unable to provide the programmed fast charge current, or if the system under charge must also share supply current with other functions, the CE3320 will automatically reduce USB fast charge current to maintain port integrity and protect the host system.
The i**nput voltage based DPM** system becomes active when the voltage on the input falls below the i**nput voltage DPM** regulation threshold (**V_{IN_DPM}**), which is typically 4.5V. The i**nput voltage based DPM** system will reduce the fast charge current level in a linear fashion until the voltage sensed on the input recovers above the charge reduction threshold voltage.

Single Path Charging from a Line Adapter or USB Source

Most USB charging applications limit charging current to 500mA(USB2.0) or 900mA(USB3.0) due to the limitations of a USB port as a power source. The CE3320 is capable of, and may be programmed for, constant current charge levels up to 2A. Thus, charging operation is not just restricted to use with

USB port supplies. Any power source may be use within the operating voltage limits as specified in the Electrical Characteristics section of this datasheet. This makes the CE3320 perfect for applications that only have one input path, but may access either a line adapter source or a USB port supply.
In order to fully utilize the power capacity from a line adapter or USB port supply, program the fast charge rate according to the highest charging current capacity of the two possible sources. If the programmed fast charge rate is greater than the current source capacity, there is little danger of system failure because the CE3320 i**nput voltage based DPM** regulation loop will activate to automatically reduce the charging current and maintain a supply voltage set by the V_{IN_DPM} regulation threshold. The system is controlled by the voltage seen on the charger input pin and will not allow the charge current to force a voltage drop below the preset V_{IN_DPM} threshold. This "intelligent" approach to charging avoids a shutdown of the USB port and ensures that the battery will be charged at the maximum rate possible at all times throughout the charging cycle. This, in turn, maximizes charge cycle efficiency and reduces it to the shortest charging time period possible under limited Adapter/USB condition compared with traditional Charger
Figure 21 shows the basic operation of the **Input Voltage Based DPM** system.

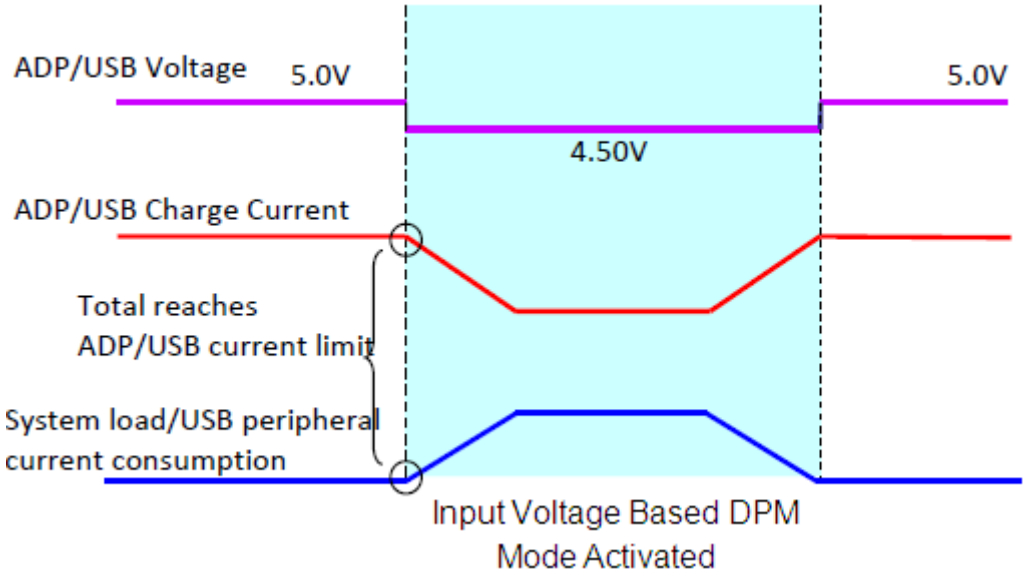


Figure 21. Input Voltage Based DPM Mode Operation

In case of an over-temperature condition with a high charge current, the device will cycle from charging to thermal shutdown and re-charge after temperature drops sufficiently, until the battery is charged to V_{FLOAT}.

Operation with a Current Limited Wall Adapter

Wall adapters with or without current limiting may be used with the CE3320, however, lowest power dissipation battery charging occurs with a current limited wall adapter. To use this feature, the wall adapter must limit at a current smaller than the high rate charge current programmed into the CE3320. For example, if the CE3320 is programmed to charge at 2A, the wall adapter current limit must be less than 2A.

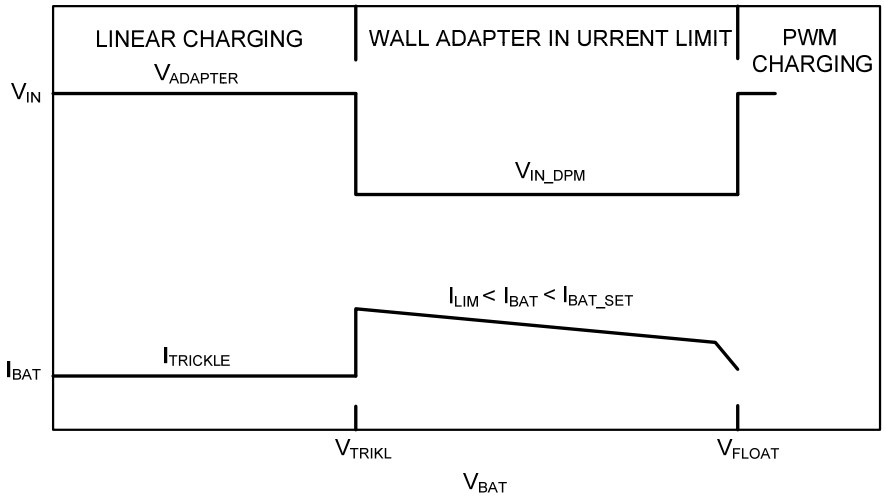


Figure 22. Charging Characteristic

To understand operation with a current limited wall adapter, assume battery voltage, V_{BAT}, is initially below V_{TRIKL}, the trickle charge threshold (Figure 22). Battery charging begins at approximately 50mA, well below the wall adapter current limit so the voltage into the CE3320 (V_{IN}) is the wall adapter's rated output voltage ($V_{ADAPTER}$). Battery voltage rises eventually reaching V_{TRIKL}. The linear charger shuts off, the PWM (high rate) charger turns on and a soft-start cycle begins. Battery charging current rises during the soft-start cycle causing a corresponding increase in wall adapter load current.

When the wall adapter reaches current limit, the wall adapter output voltage will drop to the V_{IN_DPM} threshold (the input voltage based DPM regulation loop is active then) and the CE3320 PWM charger duty cycle ramps up to 100% (the topside PMOS switch in the CE3320 buck regulator stays on continuously). When the IC enters this mode, the charge current is lower than the set value. As the battery voltage approaches V_{FLOAT}, the charge current begain drop. Furtherly, the float voltage error amplifier commands the PWM charger to deliver less than I_{LIMIT}. The wall adapter exits current limit and the V_{IN} jumps back up to $V_{ADAPTER}$.

Battery charging current continues to drop as the V_{BAT} rises, dropping to zero at V_{FLOAT}. Because the voltage drop in the CE3320 is very low when charge current is highest, power dissipation is also very low.

Thermal Calculations (PWM and Trickle Charging)

The CE3320 operates as a linear charger when conditioning (trickle) charging a battery and operates as a high rate buck battery charger at all other times. Power dissipation should be determined for both operating modes.

For preconditioning-current mode (trickle) charge - linear charger mode:

$$P_{DL} = (V_{IN} – V_{BAT}) • I_{TRIKL} + V_{IN} • I_{IN}$$

where I_{IN} is V_{IN} current consumed by the IC.

Worst-case dissipation occurs for V_{BAT} = 0, maximum V_{IN}, and maximum quiescent and trickle charge current. For example with 5.5V maximum input voltage and 65mA worst case trickle charge current, and 2mA worst-case chip quiescent current:

$$P_D = (5.5 – 0) • 65mA + 5.5 • 2mA = 368.5mW$$

For constant-current mode (fast) charge & constant-voltage mode (taper) charge - switching charge mode:

The device power dissipation of switching charge mode, P_{DS}, is a function of the charge rate and the voltage ratio of V_{BAT}/V_{IN}. It can be calculated from the following equations when a battery pack is being charged :

$$P_{DS} = \left(\frac{V_{BAT} • I_{BAT}}{\eta_S} - V_{BAT} • I_{BAT}\right) - P_{L\_winding}$$

Where:

V_{BAT} = Battery voltage

I_{BAT} = Charge current at Constant-Current Mode (Fast) Charge & Constant-Voltage Mode (Taper) Charge

η_S = Synchronous Buck Converter efficiency

$P_{L\_winding}$ = winding loss of the output inductor, it normally can be estimated as:

$$P_{L\_winding} \approx {I_{L\_RMS}}^2 \bullet R_{L\_DCR}$$

Where:

I_{L_RMS}= RMS ripple current of the output inductor, calculated as

$$I_{L\_RMS} = \sqrt{{I_{BAT}}^2 + \frac{1}{12}{\Delta I_L}^2}$$

R_{L_DCR}= DCR of the output inductor, which is temperature-dependent. It normally can be estimated as:

$$R_{L\_DCR}(T) = R_{L\_DCR}(25°C) \bullet (1+K \bullet \Delta T)$$

where K is the temperature coefficient and K ≈ 0.0039/°C.

So the IC power dissipation in switching mode, P_{DS} can be calculated from the following equations

$$P_{DS} = \left(\frac{V_{BAT} \bullet I_{BAT}}{\eta_S} - V_{BAT} \bullet I_{BAT}\right) - {I_{L\_RMS}}^2 \bullet R_{L\_DCR}(T)$$

$$P_{DS} = \left(\frac{V_{BAT} \bullet I_{BAT}}{\eta_S} - V_{BAT} \bullet I_{BAT}\right) - \left(\sqrt{{I_{BAT}}^2 + \frac{1}{12}{\Delta I_L}^2}\right)^2 \bullet R_{L\_DCR}(25°C) \bullet (1 + K \bullet \Delta T)$$

$$P_{DS} = \left(\frac{V_{BAT} \bullet I_{BAT}}{\eta_S} - V_{BAT} \bullet I_{BAT}\right) - ({I_{BAT}}^2 + \frac{1}{12}{\Delta I_L}^2) \bullet R_{L\_DCR}(25°C) \bullet (1 + K \bullet \Delta T)$$

$$P_{DS} = \left(\frac{V_{BAT} \bullet I_{BAT}}{\eta_S} - V_{BAT} \bullet I_{BAT}\right) - \left\{{I_{BAT}}^2 + \frac{1}{12} \bullet \left[\frac{V_{BAT}}{L \bullet f_{OSC}} \bullet \left(1 - \frac{V_{BAT}}{V_{IN}}\right)\right]^2\right\} \bullet R_{L\_DCR}(25°C) \bullet (1 + K \bullet \Delta T)$$

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at V_{TRIKL}. See the charging profile, Figure 3.

Power dissipation in buck battery charger mode may be estimated from the dissipation curves given in the Typical Performance Characteristics section of the data sheet. This will slightly overestimate chip power dissipation, because it assumes all loss, including loss from external components, occurs within the chip. CE3320 power dissipation is very low if a current limited wall adapter is used and allowed to enter current limit.

Insert the highest power dissipation figure into the following equation to determine maximum junction temperature:

$$T_J = T_A + (P_D \bullet 40°C/W)$$

The CE3320 includes chip overtemperature protection. If junction temperature exceeds 160°C (typical), the chip will stop battery charging until chip temperature drops below 140°C.

Thermal Considerations

The thermal path for the heat generated by the IC is from the die to the copper lead frame, through the package leads (especially the ground lead) and the Exposed Thermal Die Pad to the PC board copper. The PC board copper is the heat sink.

The CE3320 is housed in a thermally-enhanced Exposed Thermal Die Pad package that has an exposed metal pad on the backside of the package.

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA}=(T_J - T_A) / P_D$$

Where:

T_J = chip junction temperature

T_A = ambient temperature

P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The maximum power dissipation for a given situation should be calculated:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation (W)

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum junction temperature Value (ºC) [125ºC]

T_A = Ambient Temperature (°C)

Figure 23 shows the relationship of maximum power dissipation and ambient temperature of CE3320.

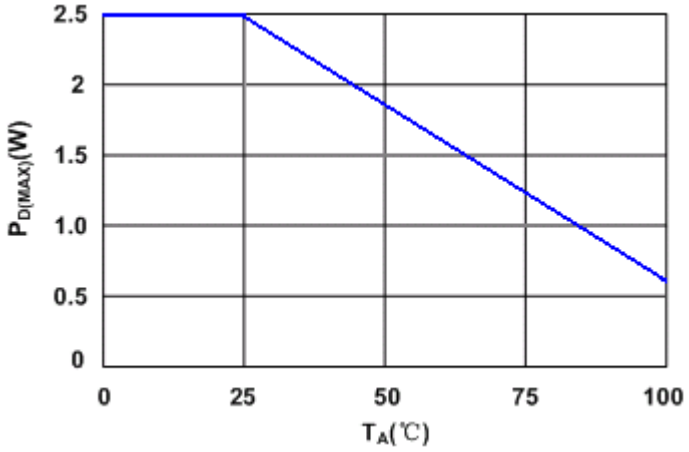


Figure 23. Maximum Power Dissipation

If the board thermal design is not adequate, the programmed fast-charge rate current may not be achieved under maximum input voltage and V_{TRIKL} battery voltage, as the thermal shutdown protection can be active effectively to avoid excessive IC junction temperature.

For improved overall thermal performance of the charger, to deliver maximum charge current under all conditions, it is critical that the exposed metal pad on the backside of the CE3320 package is properly soldered to the PC board ground via thermal land on the PCB. This ground trace acts as a both a heat sink and heat spreader. Correctly soldered to a 2500mm^2 double-sided 2oz copper board, the typical thermal resistance, θ_{JA}, of approximately 40°C/W, is achieved based on a land pattern of 2.8 mm x2.8 mm with nine vias (0.3-mm via diameter, the standard thermal via size) without air flow (see Figure 24).

As an example, a correctly soldered CE3320 can deliver 2A to a battery from a 5V supply at room temperature.

Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistances far greater than 40°C/W.

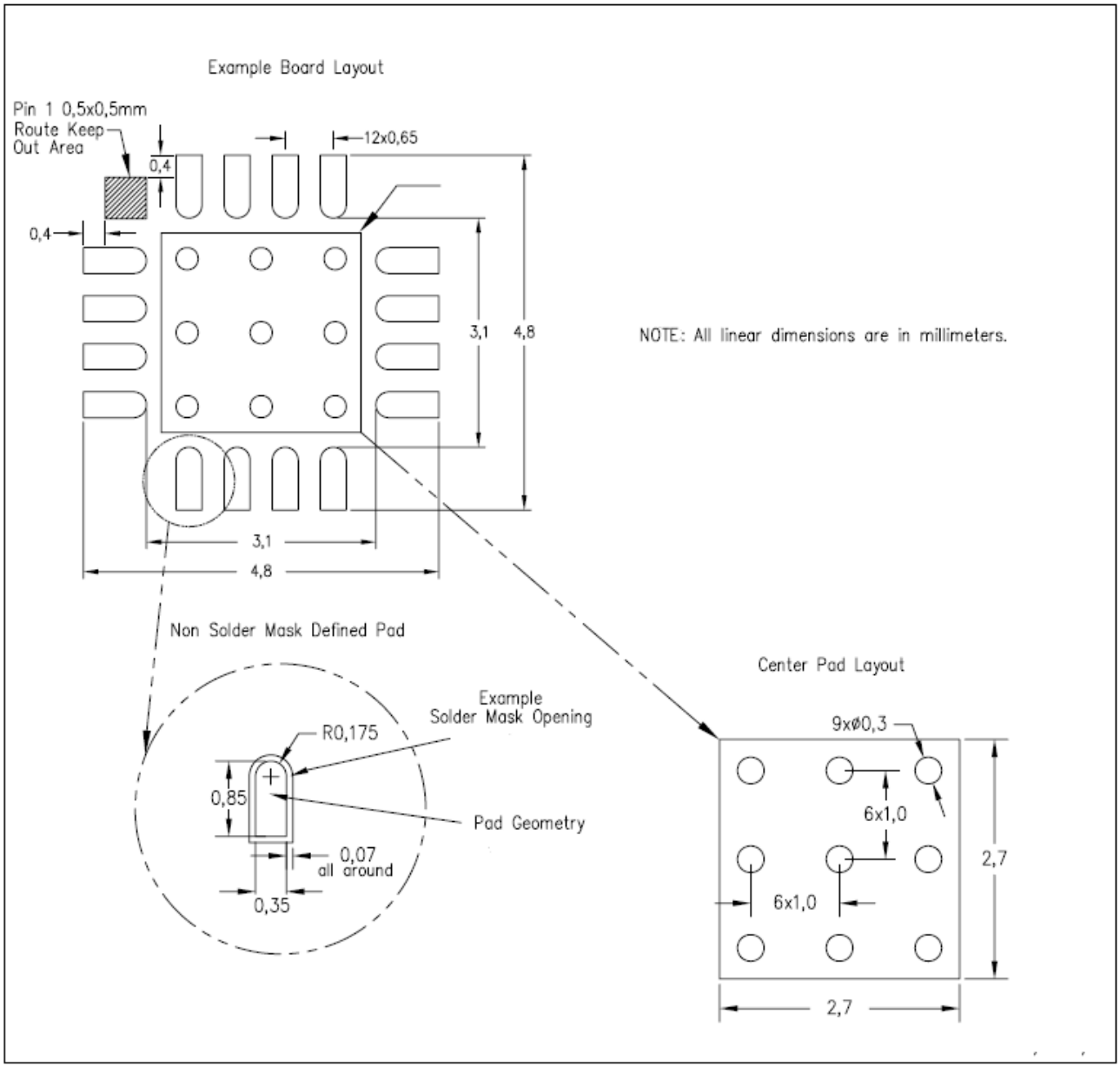


Figure 24. Recommended Land Pattern for 16-Pin QFN4x4 Exposed Thermal Die Pad

For operation at full-scale rated charge current, the power ground plane must provide adequate heat dissipating area. A 2.7mm by 2.7 mm plane of 2 ounce copper is recommended, though not mandatory, depending on ambient temperature and air flow. Most applications have larger areas of internal ground plane available, and the Exposed Thermal Die Pad should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 2A operation is desired. Connection from the exposed area of the Exposed Thermal Die Pad to the power ground plane layer should be made using 0.3 mm diameter vias to avoid solder wicking through the vias. Nine vias should be in the Exposed Thermal Die Pad area. Additional vias beyond the nine recommended that enhance thermal performance should be included in areas not under the device package.

The footprint copper pads should be as wide as possible and expand out to larger copper areas to spread and dissipate the heat to the surrounding ambient.

Other heat sources on the board, not related to the charger, must also be considered when designing a PC board layout because they will affect overall temperature rise and the maximum charge current

System Load Indefinite Operation with a powered Wall Adapter

The CE3320 is normally used in end products that only operate with the battery attached (Figure 25). Under these conditions the battery is available to supply load transient currents. For indefinite operation with a powered wall adapter there are only two requirements—that the average current drawn by the load is less than the high rate charge current, and that V_{BAT} stays above the trickle charge threshold when the load is initially turned on and during other load transients. When making this determination take into account battery impedance. If battery voltage is less than the trickle charge threshold, the system load may be turned off until V_{BAT} is high enough to meet these conditions.

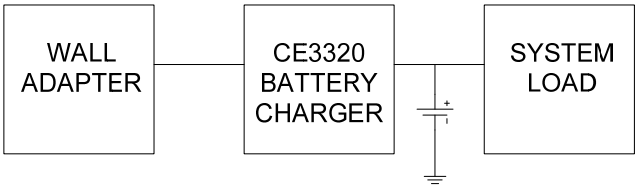


Figure 25. Typical Application

Connecting the System Load to the Battery

Some designers may simply connect the system load to the battery cell. This allows the system to be powered by Li-Ion batteries without proper regulation. It is not encouraged to attach the system load directly to Li-Ion batteries when using a stand-alone Li-Ion battery charge management with automatic termination feature.

Here are several reasons that the system load is not recommended to be connected directly to the battery terminals:

1. The charge may never end. Most Li-Ion battery chargers are based on Constant Current and Constant Voltage (CC-CV) modes. The termination is based on the ratio of charge current and preset constant current (Fast Charge). If the system draws current from the battery, the charge current will never meet the termination value. This causes the non-termination of the charge management circuit.
2. The total system current is limited by the charge current because the charger will deliver total system and battery charging current through the output pin. This solution may be feasible for some applications that run on constant current, but it is not recommended.

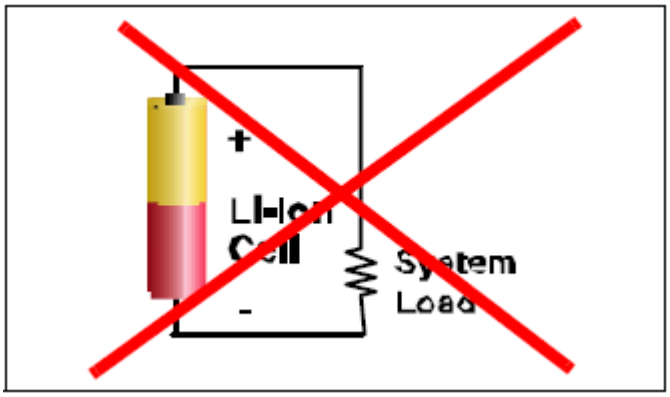


Figure 26. Do Not Connect the System Load Directly to the Battery When Charging with the Li-Ion Battery Charge Management with Automatic Termination Feature

3. A switch can be introduced to the system to turn it off before charging the batteries. This method limits the way that portable electronics operates and is only suitable for finite applications.

External Power Path Management

Some applications require that the battery be isolated from the load while charging. Figure 27 illustrates a typical charger bypass circuit. This circuit powers the load directly from the charging source via the Schottky diode D_{BYPASS}.

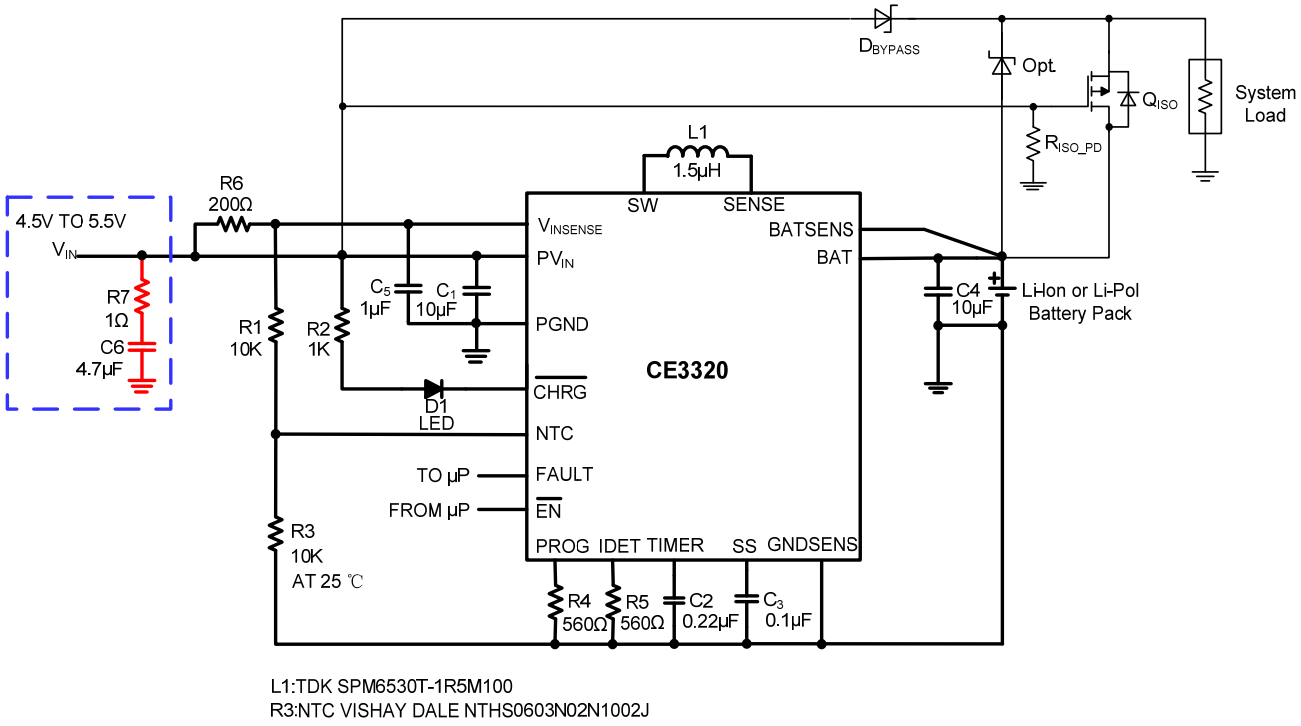


Figure 27. Battery Isolation and Power Path Bypass, Powering the Load Directly From the Charging Adapter

When the charging source is present, the p-channel MOSFET battery isolation switch Q_{ISO} source-to-gate voltage V_{SG} is equal to minus the D_{BYPASS} forward-biased voltage drop, ensuring that the switch Q_{ISO} is off (open). When the charging source is removed, the MOSFET gate is pulled down to ground by R_{ISO_PD}, closing the battery isolation switch and connecting the battery to the load.

When the charging source is removed, the turn-on of Q_{ISO} could be delayed due to its gate capacitance. If so, the substrate PN diode of Q_{ISO} will become forward biased, holding the load voltage to within 0.7V of the battery voltage until $V_{SG} > V_{TH}$, turning on Q_{ISO}. **This momentary voltage drop can be mitigated by the use of an optional Schottky diode in parallel with Q_{ISO}, as shown.**

With the load isolated from the battery, the charging adapter must supply both the load current and the charging current. If the sum of these should ever exceed the current capacity of the adapter, $V_{ADAPTER}$ will be pulled down. Current limited adapter operation of the CE3320 ensures charge cycle integrity if the device load pulls the adapter voltage down to the input voltage DPM regulation threshold V_{IN_DPM} at the CC current, or even deeper into dropout if necessary to further reduce the charge current to power the device load.

Selecting The Pull-Down Resistor

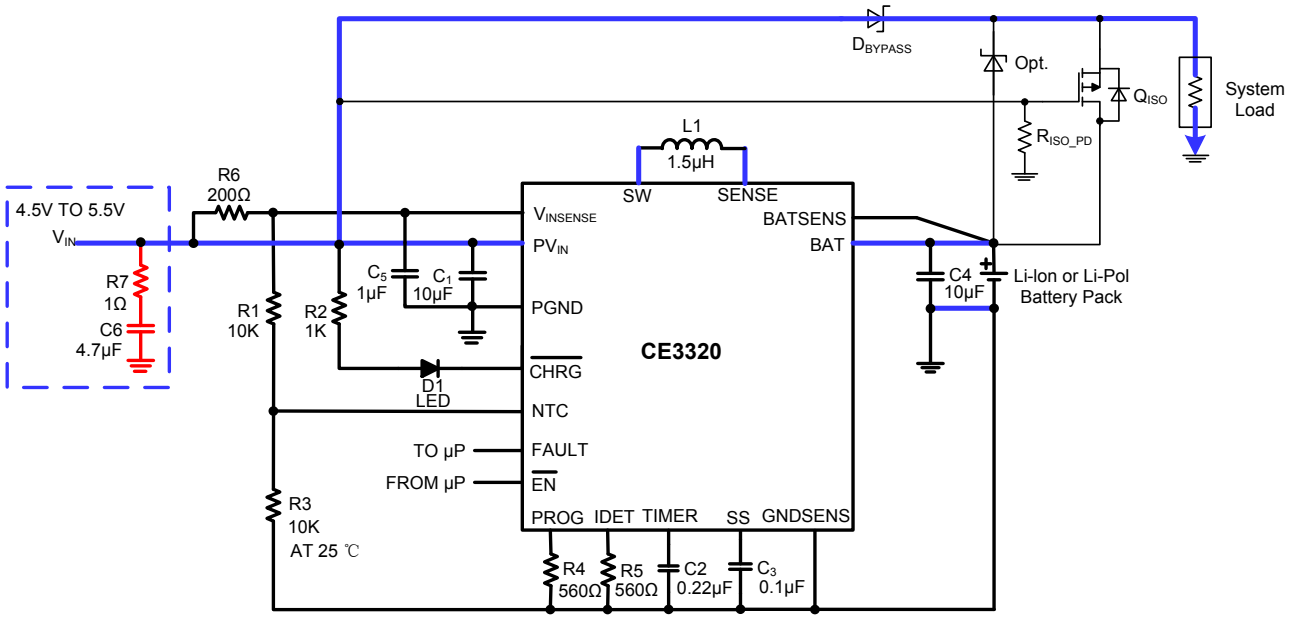
Figure 27 represents the pull-down resistor R_{ISO_PD}) to make sure that the P-Ch MOSFET (Q_{ISO}) turns on when the input sources are removed. When the input sources are absent, the R_{ISO_PD} pulls the gate to zero allowing current to flow out of the battery.

R_{ISO_PD} value can be any reasonable value resistor. However, the R_{ISO_PD} value should not be too small. A small R_{ISO_PD} value wastes unnecessary current when the input sources are present. A 100kΩ R_{ISO_PD} resistor is recommended in this design which consumes about 50μA when PV_{IN}=5V.

Selecting The MOSFET

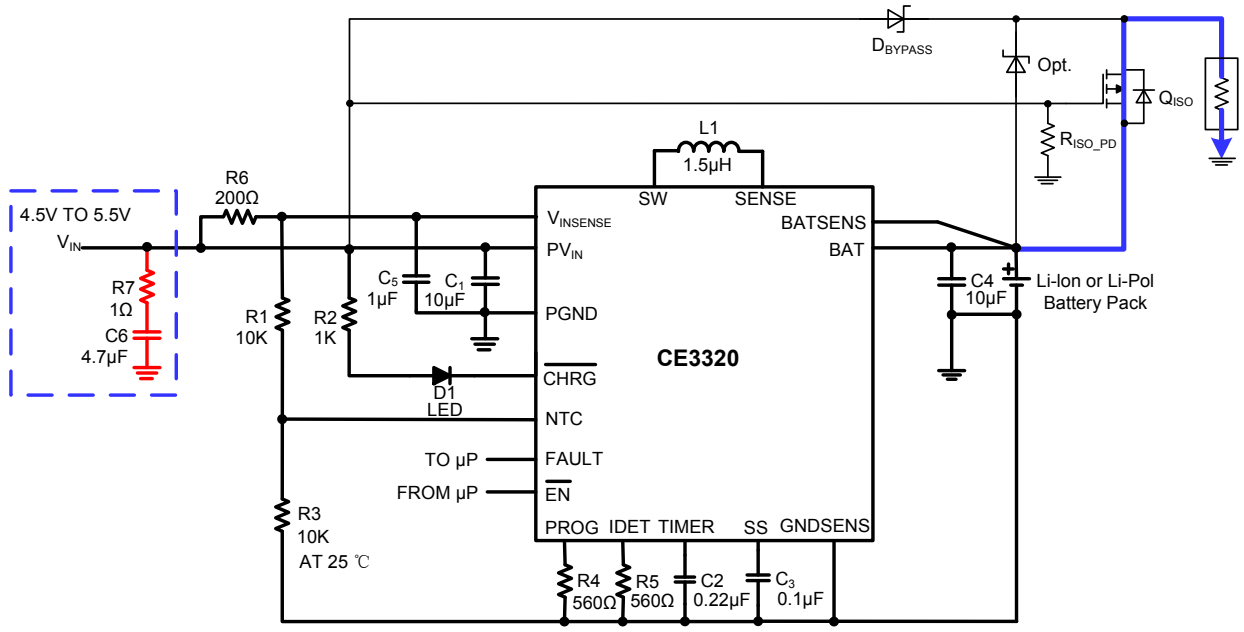
The nature of the MOSFET makes it the best candidate for current direction control. A P-Channel MOSFET is selected to complete this circuit as Figure 28 depicts, when PV_{IN} is available, the gate of Q_{ISO} is high. With Q_{ISO} off, current does not flow from the Li-Ion battery to the system load. The system load requirements are provided by the input source when the Li-Ion battery is charged at the same time. When the gate of Q_{ISO} is low, Q_{ISO} turns on and allows the Li-Ion battery to supply the system as shown in Figure 29. The CE3320 device BAT pin is also disabled when PV_{IN} is absent.

Note: It is important to select a proper gate threshold voltage range so the MOSFET will be turned on.



L1:TDK SPM6530T-1R5M100
R3:NTC VISHAY DALE NTHS0603N02N1002J

Figure 28. Q_{ISO} is Off When Gate is High and No Current Flows from the Battery Cell to the System Load.



L1:TDK SPM6530T-1R5M100
R3:NTC VISHAY DALE NTHS0603N02N1002J

Figure 29. Q_{ISO} is On When the Gate is Low and Current Flows from the Battery Cell to the System Load.

Selecting The Diode

A diode, D_{BYPASS} in Figure 29 is required to prevent reverse current from flowing to the power source. Selecting the right diode can minimize the leakage current and the forward voltage drop from the power source to the system load. A schottky diode, which has lower forward voltage drop, is recommended.

Note: The Average Forward Current has to be rated greater than the maximum system load current for the application.

Co-packaged MOSFET + Schottky Diode

Semiconductor manufacturers provide a MOSFET and Schottky diode in one small package to save board space and cost. A typical SO-8 packaged low forward voltage drop Schottky diode and power P-Ch MOSFET is used for demonstration in this section.

Using the CE3320 in Applications Without a Battery

The situation changes dramatically with the battery removed (Figure 30). Since the battery is absent, V_{BAT} begins at zero when a powered wall adapter is first connected to the battery charger. With a maximum load less than the CE3320 trickle charge current, battery voltage will ramp up until V_{BAT} crosses the trickle charge threshold. When this occurs, the CE3320 switches over from trickle charge to high rate (PWM) charge mode but initially delivers zero current (because the soft-start pin is at zero). Battery voltage drops as a result of the system load, crossing below the trickle charge threshold. The charger re-enters trickle charge mode and the battery voltage ramps up again until the battery charger re-enters high rate mode.

The soft-start voltage is slightly higher this time around (than in the previous PWM cycle). Every successive time that the charger enters high rate (PWM) charge mode, the soft-start pin is at a slightly higher voltage. Eventually high rate charge mode begins with a soft-start voltage that causes the PWM charger to provide more current than the system load demands, and V_{BAT} rapidly rises until the float voltage is reached.

For battery-less operation, system load current should be restricted to less than the worst case trickle charge current (preferably less than 30mA) when V_{BAT} is less than 3.15V (through an undervoltage lockout or other means). Above V_{BAT} =3.0V, system load current less than or equal to the high rate charge current is allowed. If operation without a battery is required, additional low-ESR output filtering improves start-up and other load transients. Battery-less start-up is also improved if a 10k resistor is placed in

series with the soft-start capacitor.

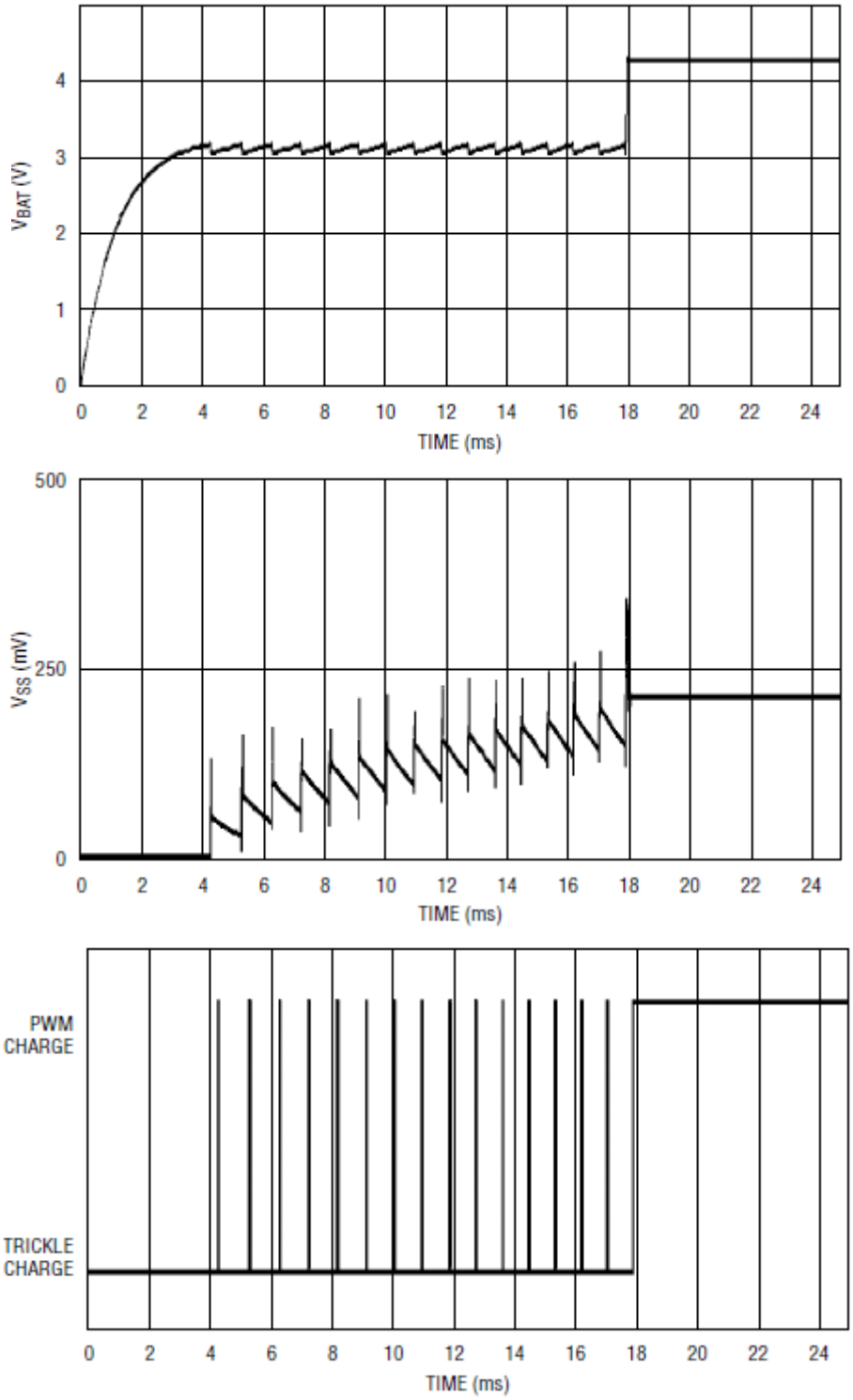


Figure 30. Battery-Less Start-Up

Reverse Polarity Input Voltage Protection

In some applications, protection from reverse polarity voltage on PV_{IN} and $V_{INSENSE}$ is desired. Where the voltage drop must be kept low, a P-channel MOSFET can be used (as shown in Figure 31).

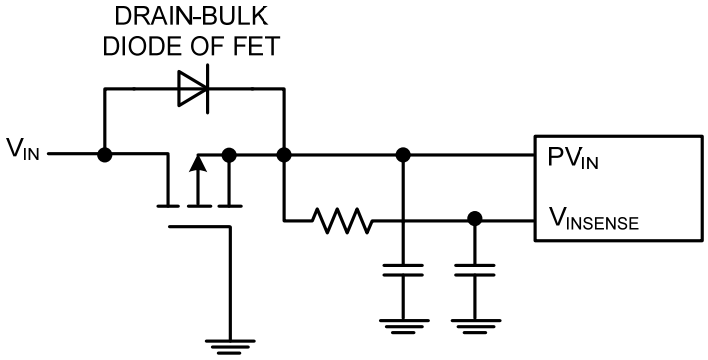


Figure 31. Low Loss Input Reverse Polarity Protection

Dynamically Selectable Charge Current

The PROG resistance can be altered dynamically under processor control by switching a second PROG pin resistor. When the higher current is required, the switch is turned on, making the effective programming resistance equal to the parallel combination of the two resistors. The external circuit is illustrated in Figure 32.

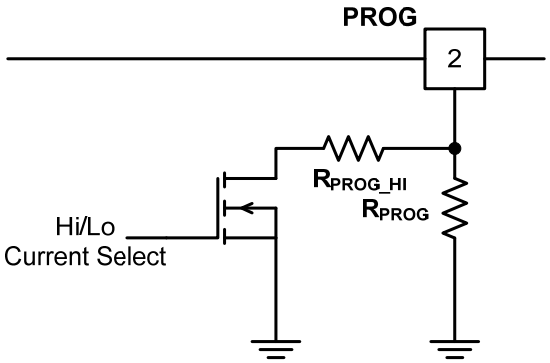


Figure 32. Dynamic selection of low and high charge currents

Note that the PROG pin resistor just only programs the fast-charge, so preconditioning (trickle)-charge, and termination currents will not be modified by a change in the PROG pin resistor.

An open-drain GPIO can be used directly to engage the parallel resistor R_{PROG_HI}. Care must be taken to ensure that the $R_{DS\text{-}ON}$ of the GPIO is considered in the selection of R_{PROG_HI}. Also important is the part-to-part and temperature variation of the GPIO $R_{DS\text{-}ON}$, and their contribution to the High Current charge current tolerance. Note also that PROG will be pulled up briefly to as high as 1.2V during startup to check for a PROG static pinshort to ground. A small amount of current could, potentially, flow from PROG into the GPIO ESD structure through R_{PROG_HI} during this event. While unlikely to do any harm, this effect must also be considered.

USB Dedicated Charger Compatibility

The CE3320 is well suited to the USB Charging Specification, Revision 1.0, Dedicated Charger, Sections 3.5 and 4.1, due to its thermal shutdown protection and current-limited-supply charging behavior.

The USB Dedicated Charger is required to limit its output current to more than 0.5A and less than 1.5A. A dedicated charger identifies itself by shorting together the USB D+ and D- lines. Once the dedicated charger is detected, the CE3320, with its 2A maximum programmed fast-charge current, permits the

fast-charge current to be set higher than the 500mA USB High Power Mode specified limit to permit faster charging of a large battery. **(See the section Dynamically Selectable Charge Current.)**

If the USB Dedicated Charger's current limit exceeds the CE3320 programmed fast-charge current, then its output will regulate to its specified output voltage, and the fast-charge current will be determined by the CE3320 PROG pin resistance to ground. If the resulting power dissipation in the CE3320 causes an excessive rise in temperature, T_J up to T_{TSD} , then thermal shutdown protection will be active to ensure safe charging.

But if the USB Dedicated charger's current limit is less than the CE3320 programmed fast-charge current, then its output voltage will be pulled down to the input voltage DPM regulation threshold of CE3320, V_{IN_DPM}. The USB Dedicated Charger is required to maintain its current limit down to 2V. This behavior is recognized in the USB Battery Charging Specification, Section 3.5, as an accepted means to reduce power dissipation in the charging circuit while charging at high current.

The CE3320 thermal shutdown protection and current-limited-adapter charging capability together ensure reliable charging at any programmed charge current, using any USB Battery Charging Specification compliant Dedicated Charger, regardless of its current limit.

USB Inrush Limiting

When a USB cable is plugged into a portable product, the inductance of the cable and the high-Q ceramic input capacitor form an L-C resonant circuit. If the cable does not have adequate mutual coupling or if there is not much impedance in the cable, it is possible for the voltage at the input of the product to reach as high as twice the USB voltage (~10V) before it settles out. In fact, due to the high voltage coefficient of many ceramic capacitors (a nonlinearity), the voltage may even exceed twice the USB voltage. To prevent excessive voltage from damaging the CE3320 during a hot insertion, it is best to have a low voltage coefficient capacitor at the PV_{IN} and $V_{INSENSE}$ pins to the CE3320 family. This is achievable by selecting an MLCC capacitor that has a higher voltage rating than that required for the application. For example, a 16V, X5R, 10µF capacitor in a 1206 case would be a better choice than a 6.3V, X5R, 10µF capacitor in a smaller 0805 case.

Alternatively, the following soft connect circuit in Figure 33 can be employed. In this circuit, capacitor C1 holds MP1 off when the cable is first connected. Eventually C1 begins to charge up to the USB input voltage applying increasing gate support to MP1. The long time constant of R1 and C1 prevent the current from building up in the cable too fast thus dampening out any resonant overshoot.

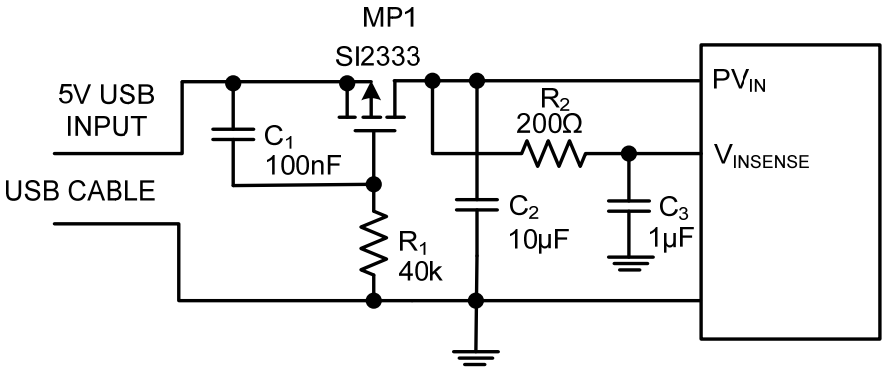


Figure 33. USB Soft Connect Circuit

PCB Layout Considerations

The switching node rise and fall times should be minimized(kept under 5ns) for minimum switching loss and maximum efficiency. Proper layout of the components to minimize high frequency current path loop (see Figure 35) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. To minimize radiation, the SW pin and input bypass capacitor leads (between PV_{IN} and PGND) should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling. The Exposed Pad must be connected to the ground plane for proper power dissipation. The other paths contain only DC and/or 1.5MHz tri-wave ripple current and are less critical.
With the exception of the input and output filter capacitors (which should be connected to PGND), all other components that return to ground should be connected to GNDSENS.
The important thing to remember about the cell connections is that high current flows through the top and bottom connection, therefore, the sense leads at these points must be made with a Kelvin connection to avoid any errors due to drop in the high current copper trace. Some designs have even extended the PACK+ and PACK– sense connections all the way to the cells themselves with additional wires or a flex circuit. So the GNDSENS and BATSENS pins of the CE3320 should be respectively connected in a kelvin fashion at the Battery negative terminal and Battery positive terminal to eliminate voltage drops in the return path which reduce the regulated battery voltage.

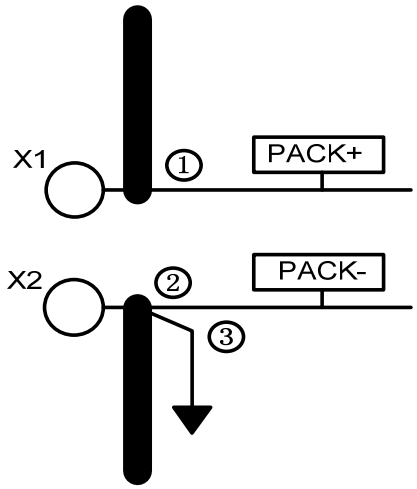


Figure 34. Lithium-Ion Cell Connections

The circled location 1 in Figure 34 indicates the Kelvin connection of the most positive battery node. Circled locations 2 and 3 are equally important. Note that the ground symbol at location 3 is only associated with UI.
Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.
1.Place the power input capacitors as close as possible to PV_{IN} pin and PGND pin connections and use shortest copper trace connection or ground plane, to make high frequency current loop area as small as possible.
2.Place 1μF input bypass capacitor GNDSENS as close to the respective $V_{INSENSE}$ cap GNDSENS and PGND pins as possible to minimize the ground difference between the input and $V_{INSENSE}$.
3.The traces from the input connector to the inputs of the CE3320 should be as wide as possible to minimize the impedance in the line. Although the V_{IN_DPM} feature will allow operation from input sources having high resistances(impedances), the CE3320 input PV_{IN} pin has been optimized to connect to input sources with no more than 250mohm of input resistance, including cables and PCB traces.
4.The output inductor should be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high frequency oscillation problems, proper layout to minimize high frequency current path loop is critical (see Figure 35). Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

5.The local output bypass capacitor from BAT to PGND should be connected between the BAT pin and PGND of the IC. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
6.Minimize the amount of inductance between BAT and the postive connection of the battery terminal. If a large parasitic board inductance on BAT is expected, increase the bypass capacitance on BAT.
7.Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
8.The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
9.The high-current charge paths into PV_{IN}, BAT, SENSE and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pin is power ground connection for high-current power converter node. Internally, PGND is connected to the source of the internal n-channel low-side FET. On PCB layout, connected directly to ground connection of input and output capacitors of the charger and should be connected to the ground plane to return current through the internal low-side FET.
10.GNDSENS provides a Kelvin connection for PGND and must be connected to PGND schematically.
11.Route analog ground separately from power ground. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
12.Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
13.It is critical that the exposed power pad on the backside of the IC package must be soldered to the PCB ground plane for proper power dissipation and should be connected to as much copper in the PCB as possible. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers. This allows better thermal performance as the board pulls heat away from the IC.
14.The via size and number should be enough for a given current path.
15. The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. It is important that the NTC thermistor not be in close thermal contact with the CE3320. Furthermore, it is essential that the $V_{INSENSE}$ connection to R_{NOM} is made according to standard Kelvin sense techniques.
16.The constant current provided to charge the timer capacitor is very small, and the TIMER pin is susceptible to noise and changes in capacitance value. Therefore, the timer capacitor should be physically located on the printed circuit board layout as close as possible to the TIMER pin.

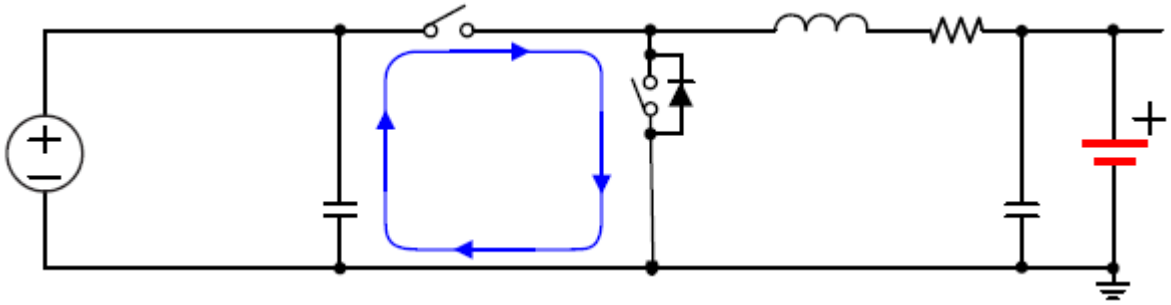
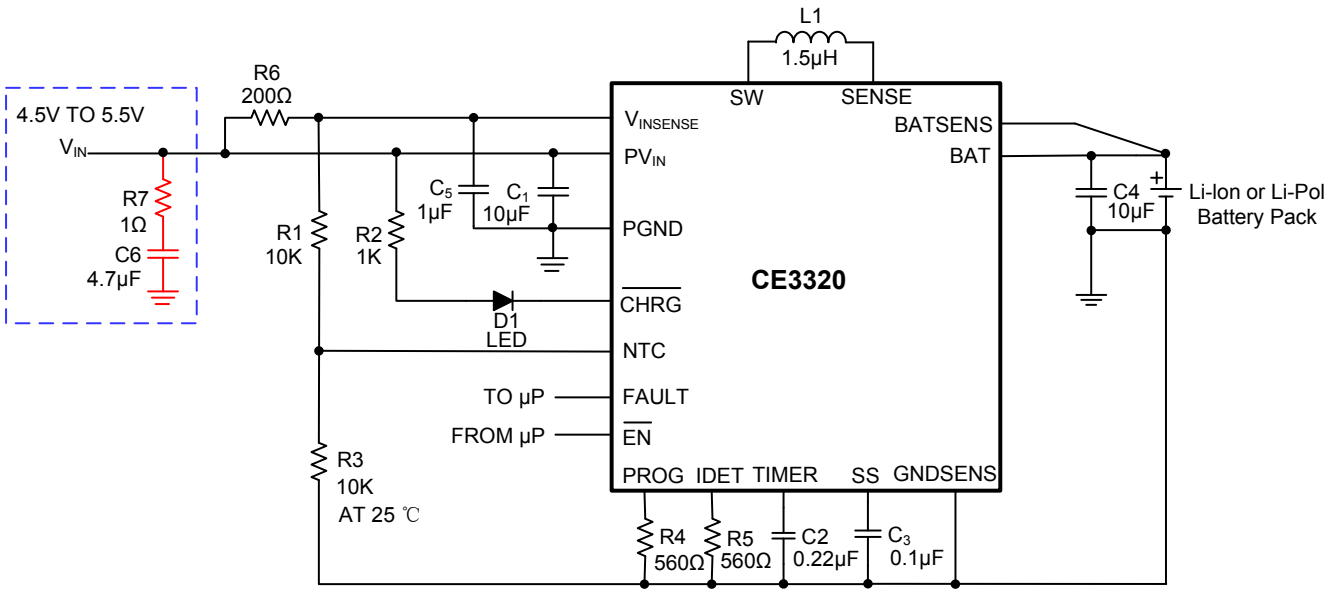


Figure35. High Frequency Current Path

Recommended Components Manufacturers

For a list of recommend component manufacturers, contact the Chipower application department.



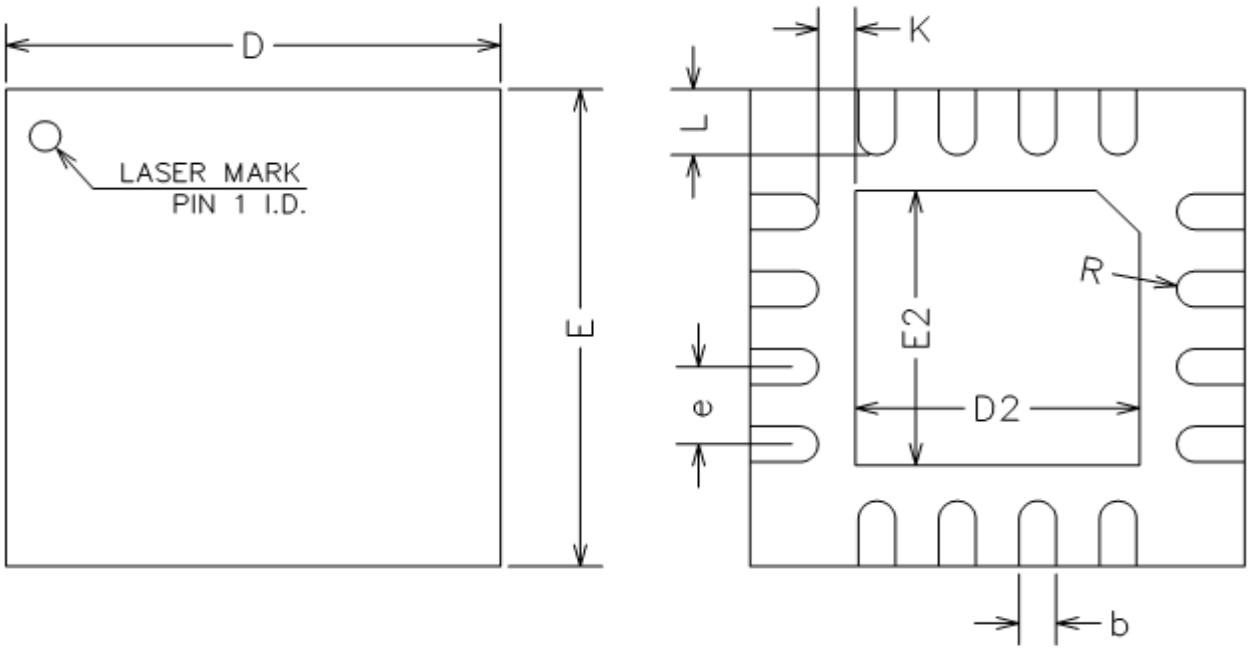
L1:TDK SPM6530T-1R5M100

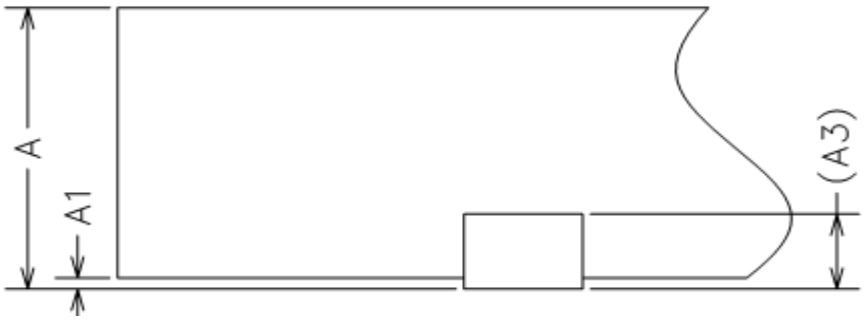
R3:NTC VISHAY DALE NTHS0603N02N1002J

Figure 36. 2A Li-Ion Battery Charger with 2.5Hr Timer, Temperature Qualification, Soft-Start, Remote Sensing and C/10 Indication

■ PACKAGING INFORMATION

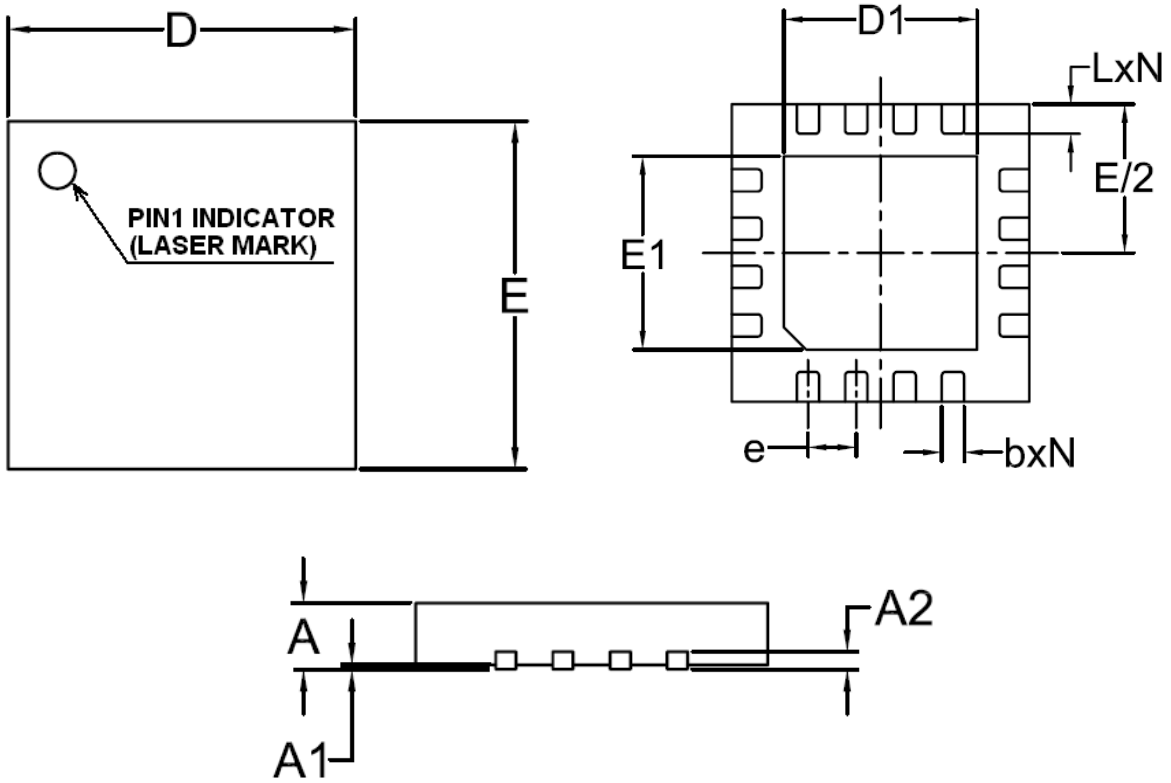
● QFN4×4-16 PACKAGE OUTLINE DIMENSIONS





Dimensions In Millimeters			
Symbol	Min	NOM	Max
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A3		0.20REF	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.20	2.30	2.40
E2	2.20	2.30	2.40
e	0.55	0.65	0.75
K	0.20	-	-
L	0.50	0.55	0.60
R	0.09	-	-

- **QFN4×4-16B PACKAGE OUTLINE DIMENSIONS**



Dimensions In Millimeters			
Symbol	Min	NOM	Max
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2		0.20BSC	
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D1	2.50	2.60	2.80
E	3.90	4.00	4.10
E1	2.50	2.60	2.80
e		0.65BSC	
L	0.30	0.40	0.50
N		16	