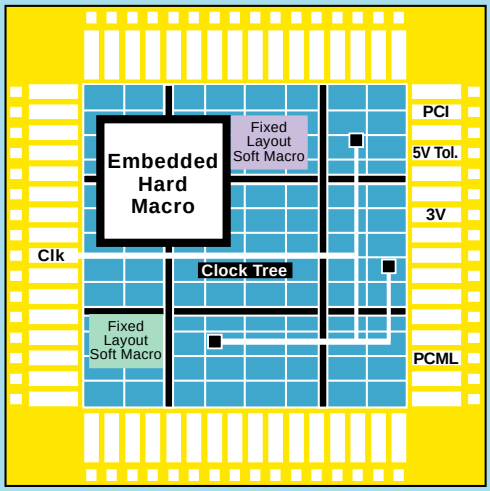
CE71 Series Embedded Array

0.25µm CMOS Technology

Features

- 0.18µm L_{eff} (0.24µm drawn)
- Propagation delay of 61 ps
- Separate core and I/O supply voltages
- Mixed-signal macros–A/D and D/A converters
- I/Os: 2.5V, 3.3V, 5V tolerant
- Core power supply voltage: 2.5V, 1.8V, 1.5V
- Junction temperature: -40ºC~125ºC
- High performance and special I/Os–PCML, LVDS, PCI, SSTL, GTL+, AGP, USB
- Analog and digital PLLs
- Packaging options: QFP, HQFP, BGA, TBGA
- Support for major third-party EDA tools



Description

Fujitsu's CE71 is a series of high-performance, 0.18µm L_{eff} CMOS embedded arrays that include full support of diffused high-speed RAMs, ROMs, mixed-signal macros, and a variety of other embedded functions.

The CE71 series offers density and performance similar to those of standard cells, yet provides the time-to-market advantage of gate arrays. The CE71 series devices include 44µm, 66µm, or 88µm pad pitch for a cost-effective solution for both pad-limited and core-limited designs.

With a nominal 1.5V to 2.5V core operation and with 2.5V and 3.3V/5V tolerant I/Os, the CE71 series features a very low-power consumption of 0.06µW/gate/MHz. Potential applications for the CE71 series include computing, graphics, communications, networking, wireless, and consumer designs.

J-Series with 66µm Stagger Pad Pitch and Wire Bonding

Frame	Total Gates	Total Pads	Signals
CE71J1	216K	192	152
CE71J2	312K	224	152
CE71J3	488K	272	178
CE71J4	703K	320	206
CE71J5	911K	360	264
CE71J6	1,098K	392	304
CE71J7	1,302K	424	360
CE71J8	1,524K	456	360
CE71J9	2.020K	520	360
CE71JA	2,586K	584	472
CE71JB	3,055K	632	472
CE71JC	3,564K	680	506
CE71JD	4,113K	728	506
CE71JE	5,114K	808	506
CE71JF	6,698K	920	506
CE71JG	8,096K	1,008	506

K-Series with 88µm Inline Pad Pitch and Wire Bonding

Frame	Total Gates	Total Pads	Signals
CE71K1	167K	100	88
CE71K2	237K	120	102
CE71K3	348K	144	126
CE71K4	524K	176	152
CE71K5	734K	208	178
CE71K6	963K	240	206
CE71K7	1,110K	256	220
CE71K8	1,559K	304	264

CE71 Series Embedded Array

L-Series with 44µm Inline Pad Pitch and Au Bump			
Frame	**Total Gates**	**Total Pads**	**Signals**
CE71L4	356K	304	264
CE71L5	476K	352	304
CE71L6	677K	420	360
CE71L7	1,034K	520	428
CE71L8	1,469K	620	504
CE71L9	1,976K	720	504
CE71LA	2,513K	812	504
CE71LB	3,001K	888	504
CE71LC	3,506K	960	504
CE71LD	4,050K	1,032	504
CE71LE	5,043K	1,152	504

T-Series with 88µm Inline Pad Pitch and Wire Bonding			
Frame	**Total Gates**	**Total Pads**	**Signals**
CE71T2	347K	144	128
CE71T3	524K	176	156
CE71T4	734K	208	178
CE71T5	845K	224	192
CE71T6	963K	240	206
CE71T7	1.110K	256	220
CE71T8	1.407K	288	248
CE71T9	1.559K	304	264
CE71TA	1.827K	328	264
CE71TB	2.088K	352	312
CE71TC	2.398K	376	312
CE71TD	3.040K	424	360
CE71TE	3.645K	464	360
CE71TG	5.152K	552	264

Mixed-Signal Macros

D/A Converters

- 10-bit: 1 MS/s, 1.5 MS/s, 30 MS/s, 50 MS/s, 100 MS/s, 220 MS/s
- 8-bit: 200 KS/s, 1 MS/s, 50 MS/s

A/D Converters

- 12-bit: 1 MS/s
- 10-bit: 1 MS/s, 20 MS/s, 40 MS/s
- 8-bit: 1 MS/s, 30 MS/s, 50 MS/s
- 6-bit: 100 MS/s, 500 MS/s

Multiplier Compiler

- Multiplicand (m): $4 \leq m \leq 32$
- Multiplier (n): $4 \leq n \leq 32$ (even number only)

Memory Macros

- SRAM Compiler: single and dual port (1 R/W, 1R), up to 72K bits per block, both BUS and Partial Write
- ROM Compiler: up to 512K bits per block
- High-density single-port RAM 288K bits
- Register file (2R/W, 2R/2W), up to 4,608 bits

Phase-Locked Loops

- Analog: up to 250 MHz (622 MHz under development)

I/Os

- 2.5V, 3.3V, and 5V tolerant
- Slew-rate controlled
- CMOS, TTL, PCML, T-LVTTL, LVDS, PCI, SSTL, GTL+, AGP, USB

SOC IP Cores

ARM 7TDMI Hard Macro
ARC 32-bit RISC
834/836 SPARClite Hard Macros
Oak DSP Hard Macro
10/100 MAC
64/256 QAM
MPEG2 Decoder/Demultiplexer
8VSB TV Demodulator
AC-3 Dolby Voice Decoder
JPEG Encoder and Decoder
PCI–33/66 MHz, 32/64-bit cores
USB Host Controller/Device
I^2C
IDE (ATA3) Host Controller
Smart Card I/F
IRDA I/R Interface
More IPs are being added

ASIC Design Kit and EDA Support	
Verilog Logic Simulators from Cadence, Synopsys, and Mentor	Verilog-XL, NC-Verilog, VCS, Model-sim (Verilog)
VHDL/VITAL Logic Simulators from Synopsys, Cadence, and Mentor	VSS, Model-sim (VHDL), V-System, Leapfrog
Synthesis, power, DFT, and STA tools from Synopsys	Design Compiler, Design Power, Test Compiler, PrimeTime, MOTIVE, and Sunrise TestGen
Other EDA tools	Chrysalis Design Verifyer and Sente Watt Watcher

PACKAGE AVAILABILITY	
No. of Pins	**Frame Size**
Thin and Low Profile QFP Packages (0.4, 0.5 mm lead pitch)	
100	K1, K2
120	K2, K3
144	K3, K4, K8, T2, T3
176	K4, K5, T3, T4
208	T4, T5, T6, T7, T8, T9
256	T8, T9, TA, TB, TC
Shrink QFP Package (0.5 mm lead pitch)	
176	J1, J2, K4, K5
208	J3, J4, J5, K5, K6, K7, K8
240	J4, J5, J6, K6, K7, K8
Heatspreader QFP Package (0.4, 0.5 mm lead pitch)	
208	J3, J4, J5, J6, J7, J8, J9, K5, K6, K7, K8
	T4, T5, T6, T7, T8, T9
240	J4, J5, J6, J7, J8, J9, JA, K6, K7, K8, T6, T7, T8, T9, TA
256	J5, J6, J7, J8, J9, T7, T8, T9, TA, TB, TC
304	J7, J8, J9, JA, JB, JC, JD, JE, JF, JG, TB, TC, TD, TE, TG
Ball Grid Array (1.27 mm ball pitch)	
256	J3, J4, T7, T8, T9, TA, TB
352	J6, J7, J8, TB, TC, TD
420	J8, J9, TD, TE
576	JA, JB
672	JC, JD
Fine-Pitch Ball Grid Array (0.75, 0.8 mm ball pitch)	
144	T3
176	T3, T4
224	T5, T6, T7, T8, T9
288	T8, T9, TA, TB, TC
Tab Ball Grid Array (0.8, 1.0 mm ball pitch)	
304	L4, L5
352	L5, L6, L7
480	L6, L7
560	L7, L8, LB, LC
660	L8, L9
720	L9, LA, LB, LC, LD, LE

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